MS Thesis

Design and Implementation of Energy-Efficient Analog Front-End Circuit for a Sub-1V Digital Hearing Aid Chip

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Korea Advanced Institute of Science and Technology

Outline

- Motivation
- Proposed Analog Front-End Circuit
- Building Blocks
  - Preamplifier with combined gain control
  - Σ-Δ Modulator with adaptive-SNR
- Implementation Results
- Conclusions and Further Works

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Motivation

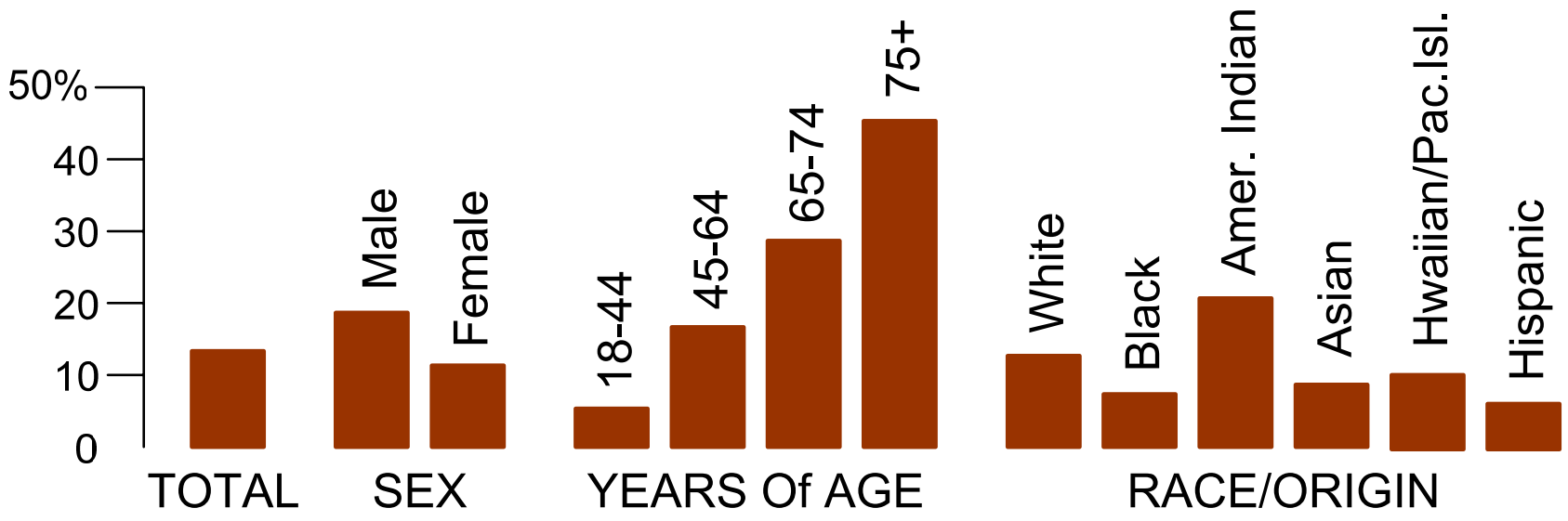
- More and More Needs on Digital Hearing Aid
- More Design Requirements
  - Low-power consumption
  - Small size
  - Programmability
  - Low cost CMOS process

[Newsweek. June 6, 2005]

"…more than 28 million Americans have some degree of hearing loss, a number that could reach 78 million by 2030…"

Motivation (Cont'd)

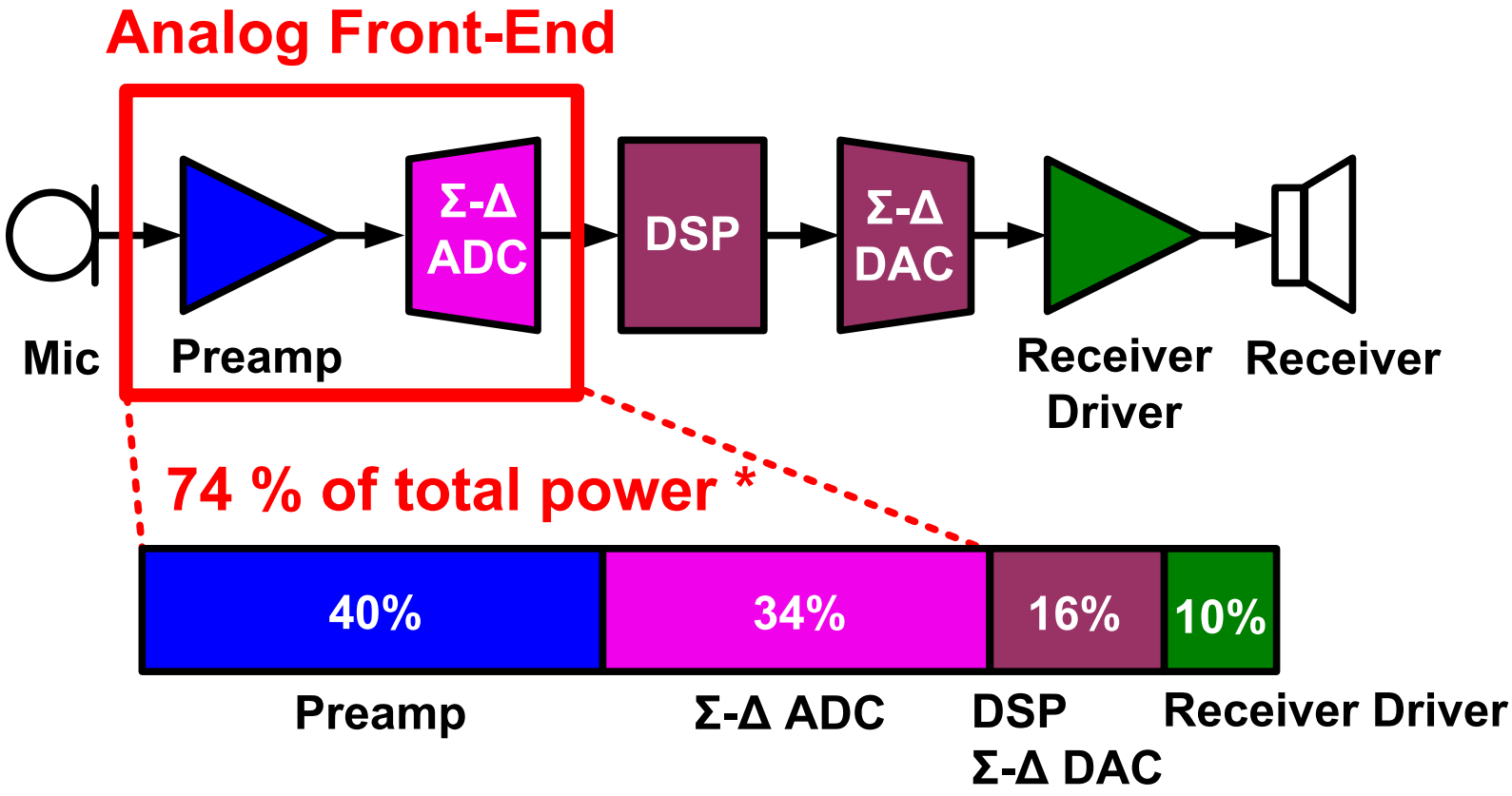
- **Americans with hearing trouble***



***Mild to severe hearing loss,2002.**

Sources:NATL. Health interview survey, CDC

Overview of the Digital Hearing Aid



*[ISSCC2002. John W. Fattaruso et.al.]

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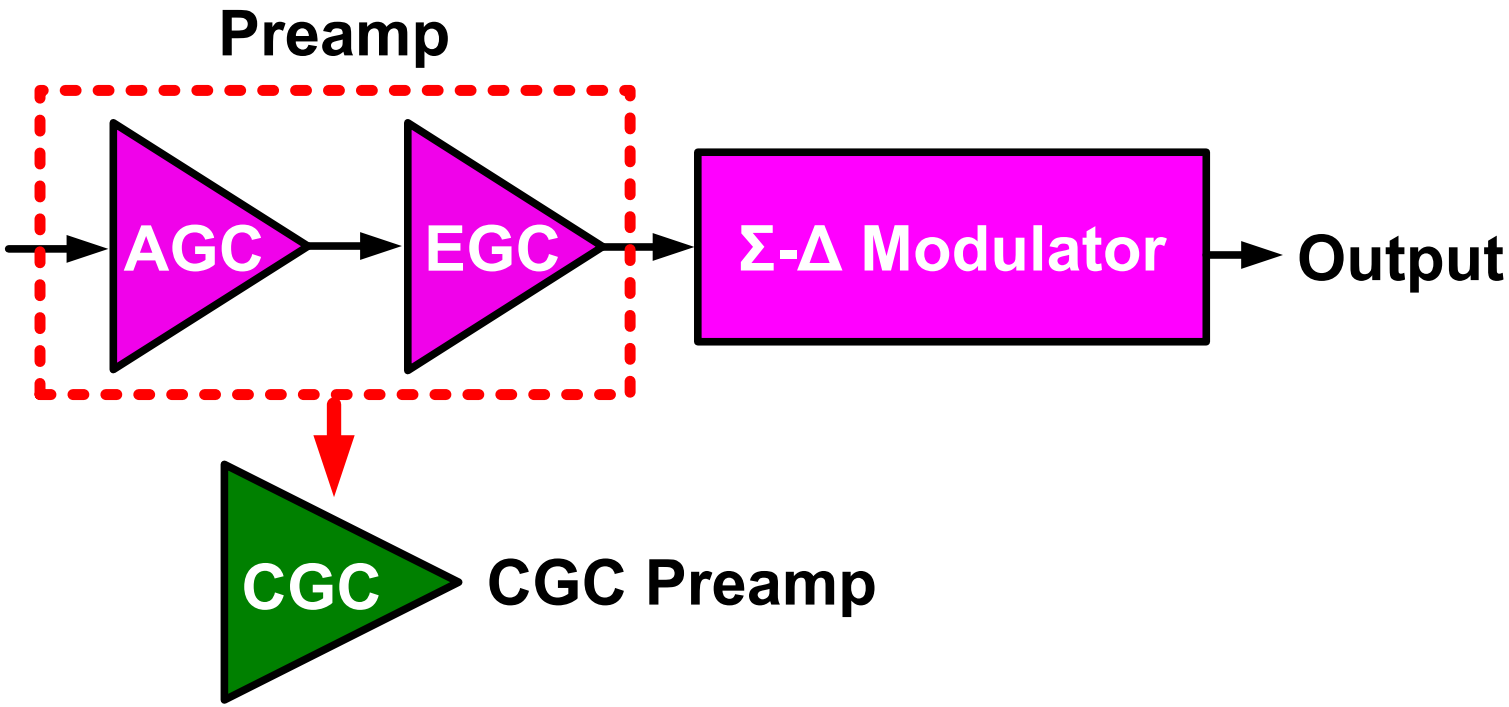
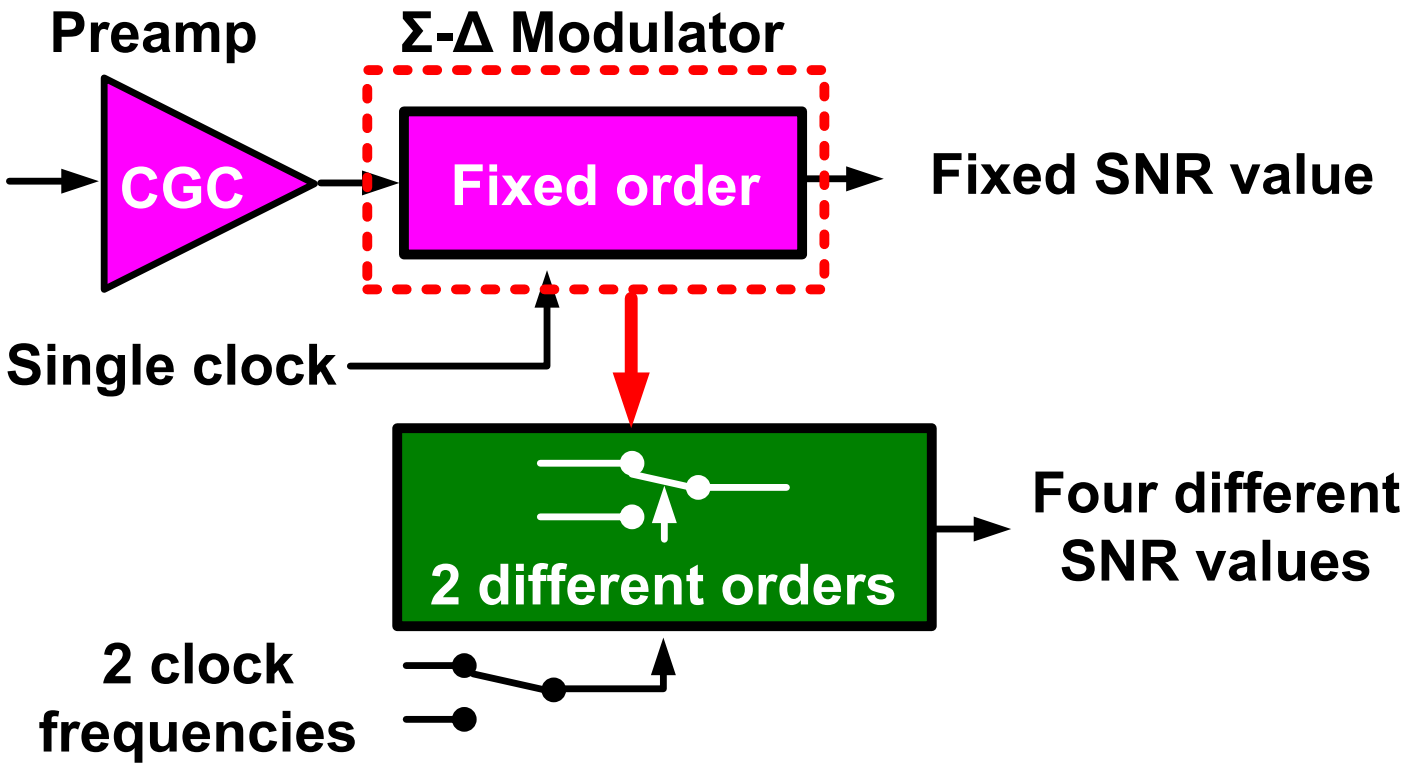
CGC Preamplifier



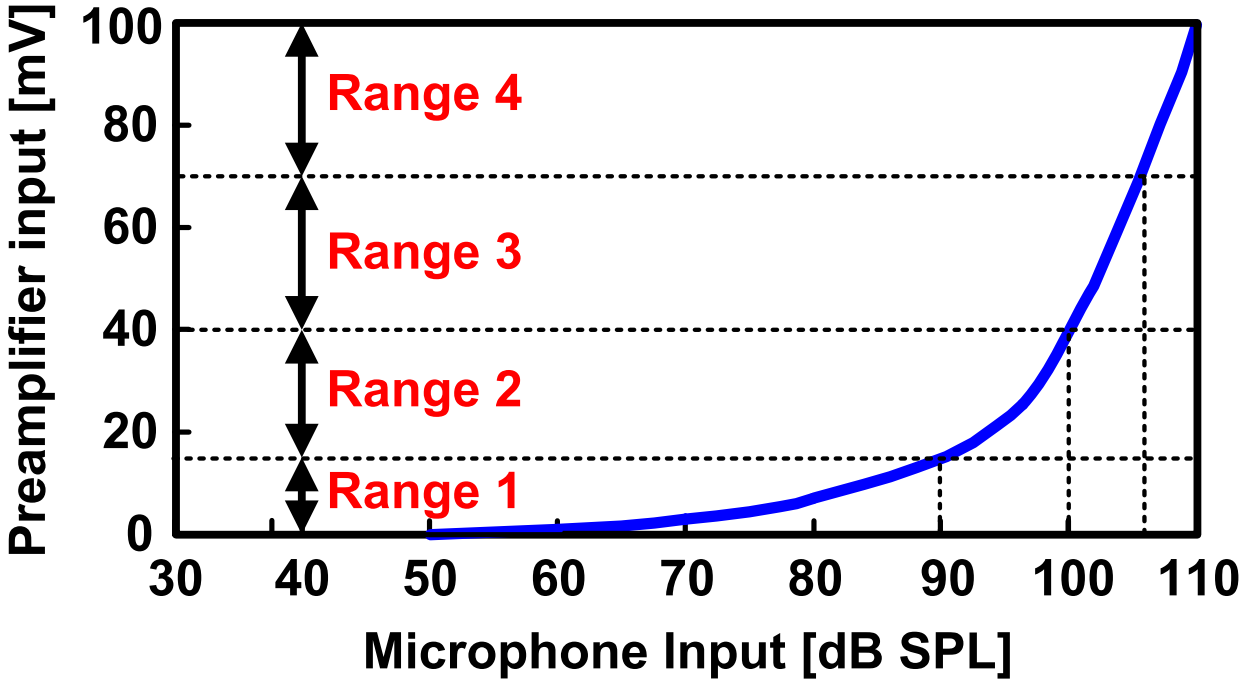
- Low Power Consumption
- Controllability with combined gain control

Adaptive SNR Σ-Δ Modulator



- **Multiple SNR values with adaptive SNR**

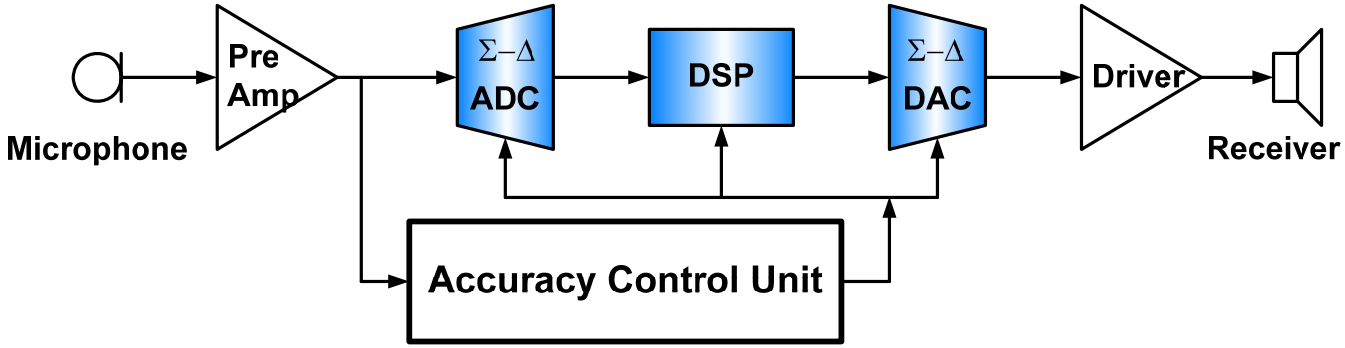
Needs of Adaptive-SNR Values

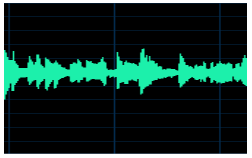


- **Normal sound level from 30 to 90-dB SPL**
  - **High performance Σ-Δ Modulator**
- **Sufficiently large sound above 90-dB SPL**
  - **Medium performance Σ-Δ Modulator**

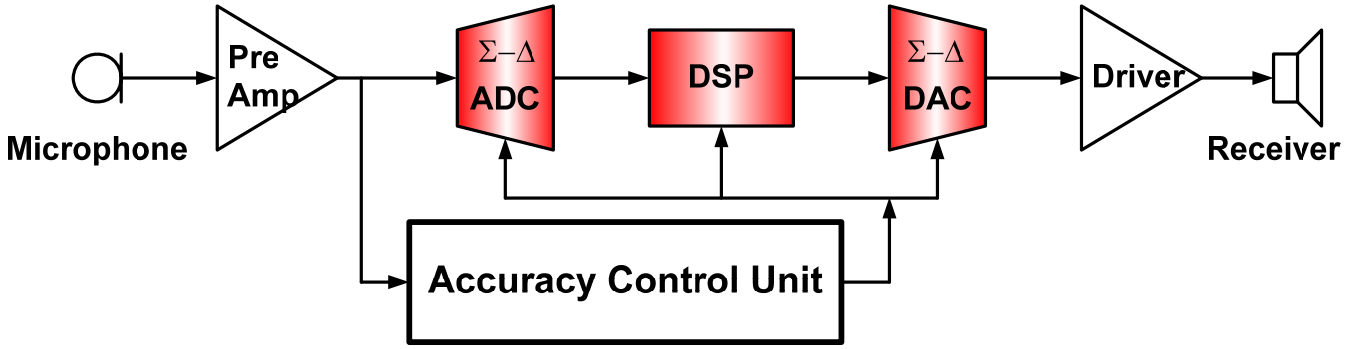
Environment-Aware Operation

low-resolution operation with normal SNR
(power-reduction)

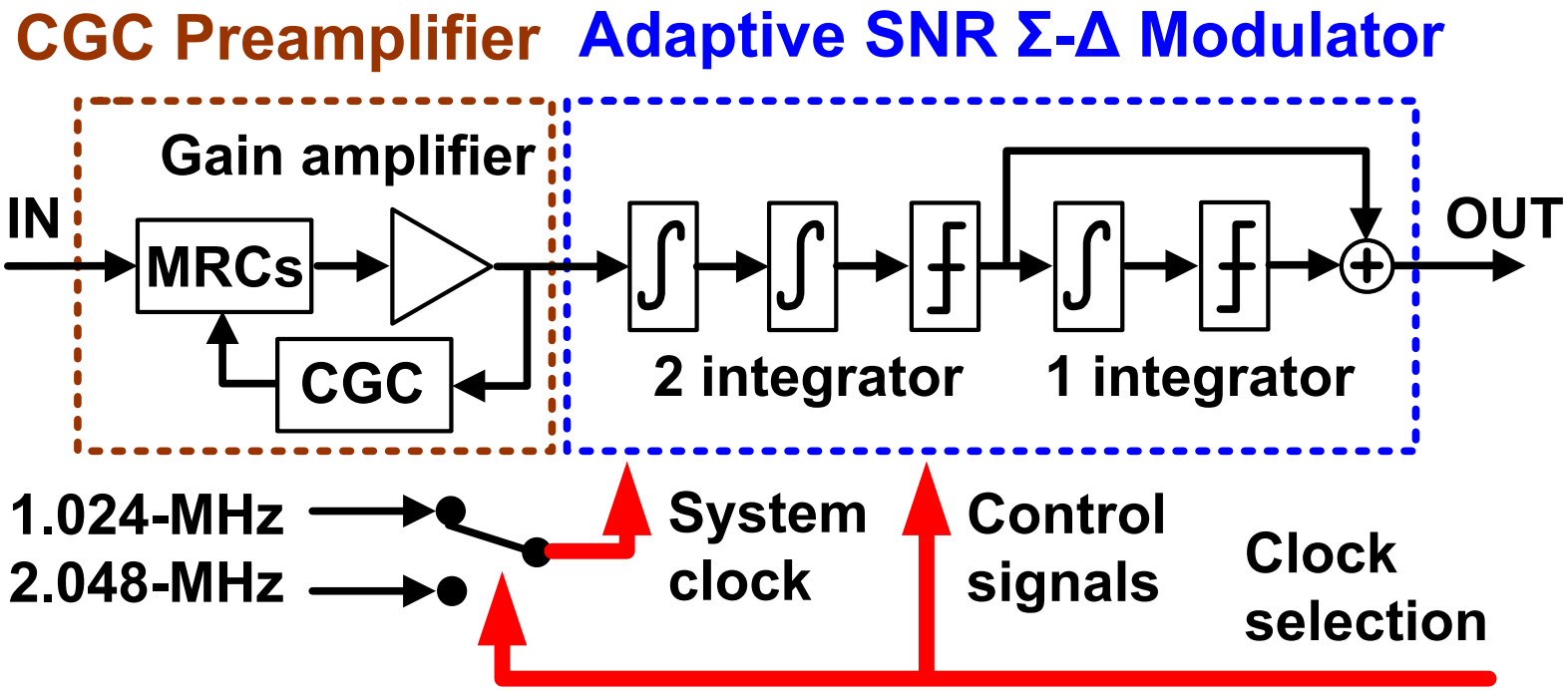




high-resolution operation with enhanced SNR



Proposed Analog Front-End



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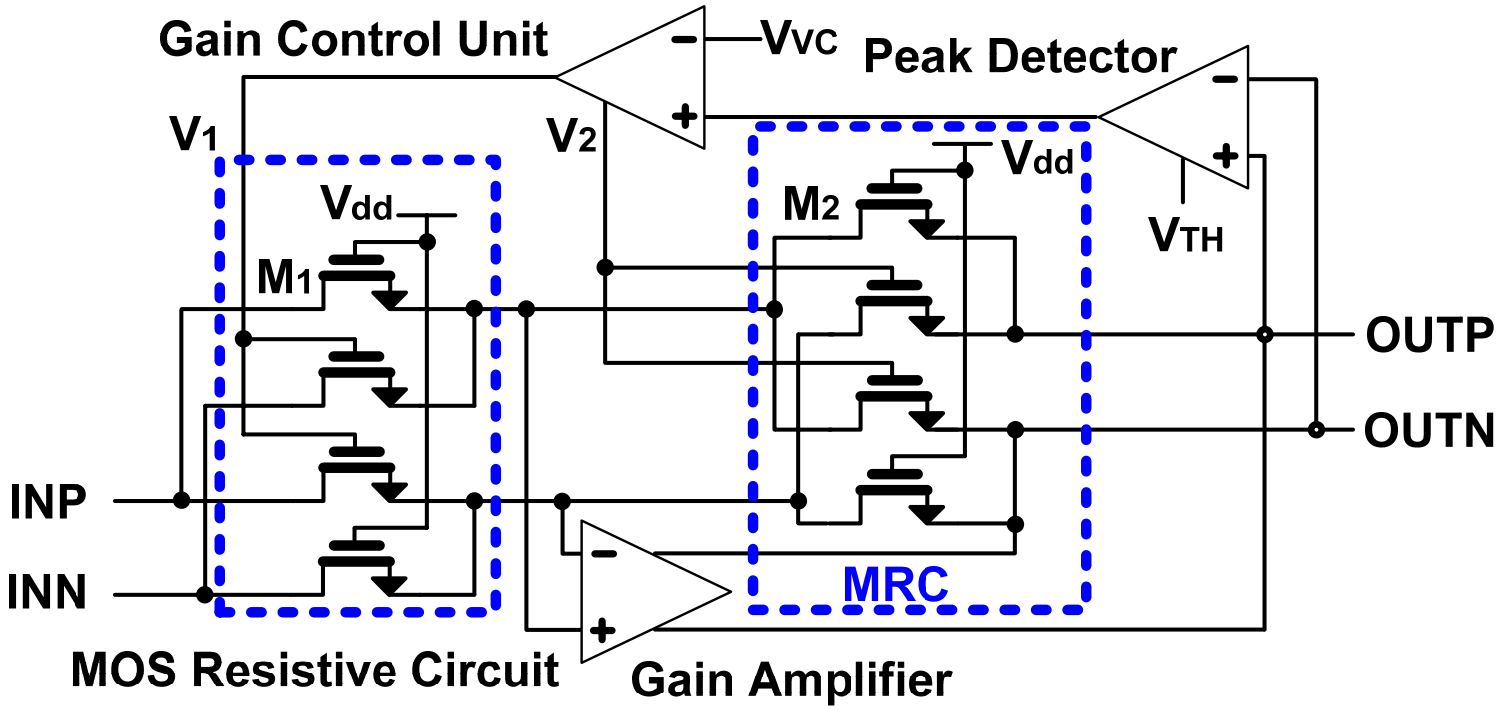
CGC Preamplifier



$$Av = \frac{OUT}{IN} = W_1 L_2 \left(1 + \frac{V_x}{V_{dd} - V_{VC}}\right) / W_2 L_1 \left(1 - \frac{V_x}{V_{dd} - V_{VC}}\right) \qquad \begin{aligned} V_1 &= V_{VC} - V_x \\ V_2 &= V_{VC} + V_x \end{aligned}$$

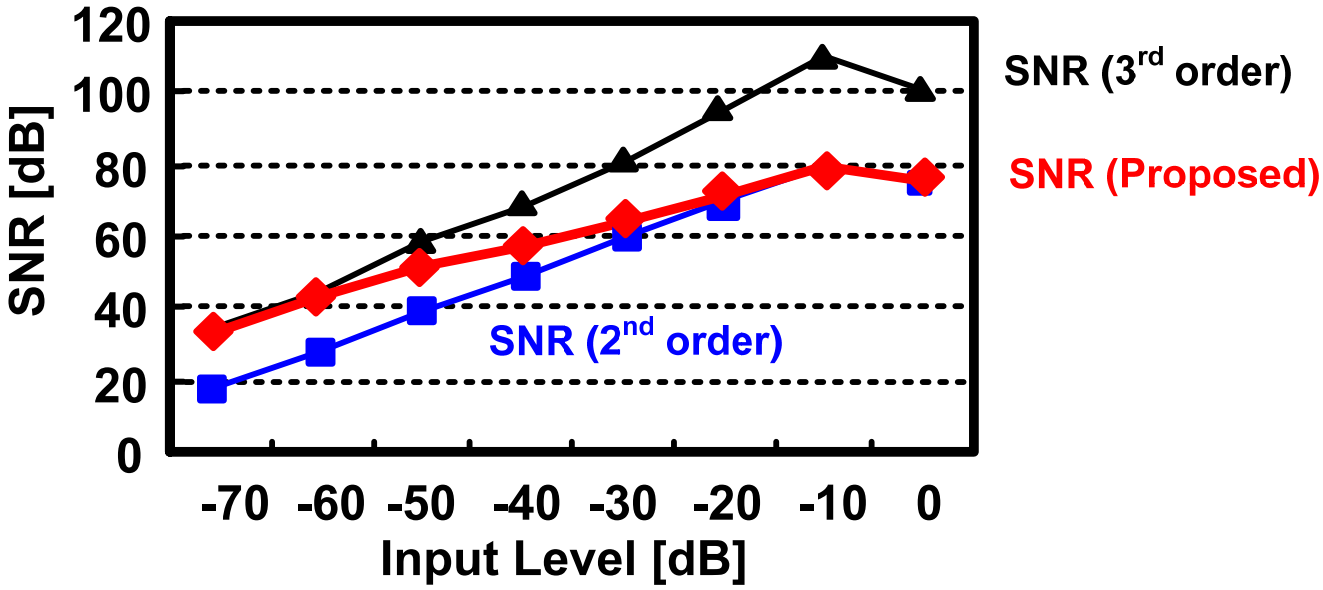
How to obtain multiple SNR values

- **Multiple Clock Frequencies**
  - ☺ **Various SNR values with small power consumption**
  - ☹ **Difficult to design by analog circuit**

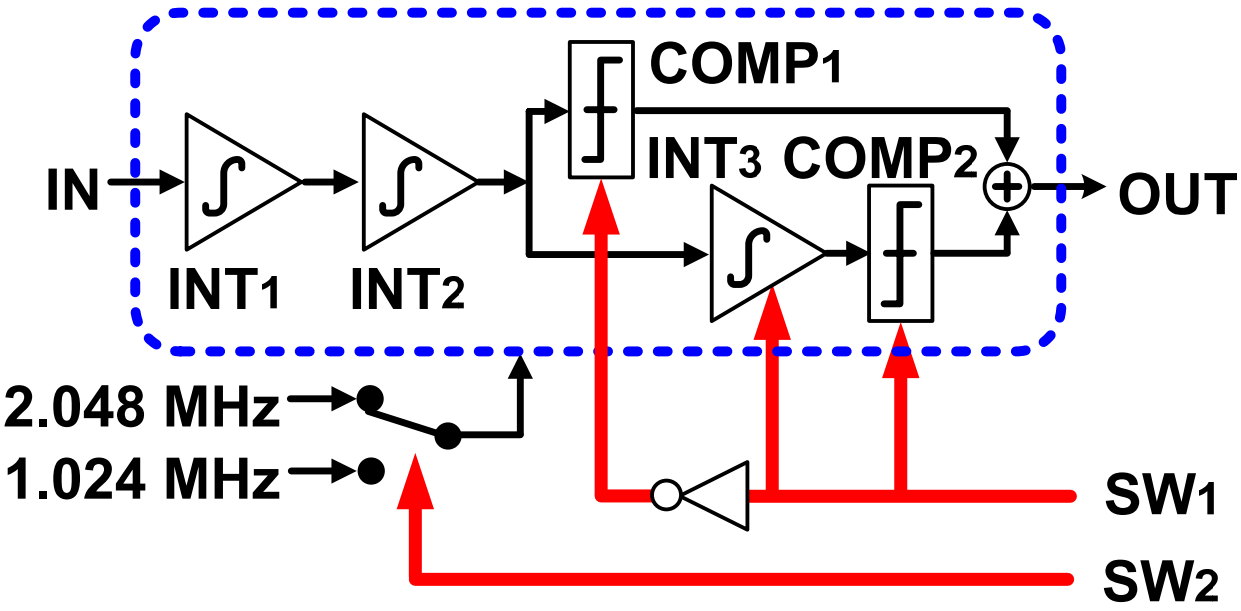
- **Multiple Orders of the Σ-Δ Modulator**
  - ☺ **Large SNR variations**
  - ☹ **High power consumption due to additional OTA**
  - ☹ **Unstable @ > 3rd order Σ-Δ modulator**

Adaptive SNR Σ-Δ Modulator

- **Combine only the strong points of the two methods**
  - ☺ **Variable clocking : 1.024-MHz or 2.048-MHz**
  - ☺ **Various order : 2nd or 3rd order**

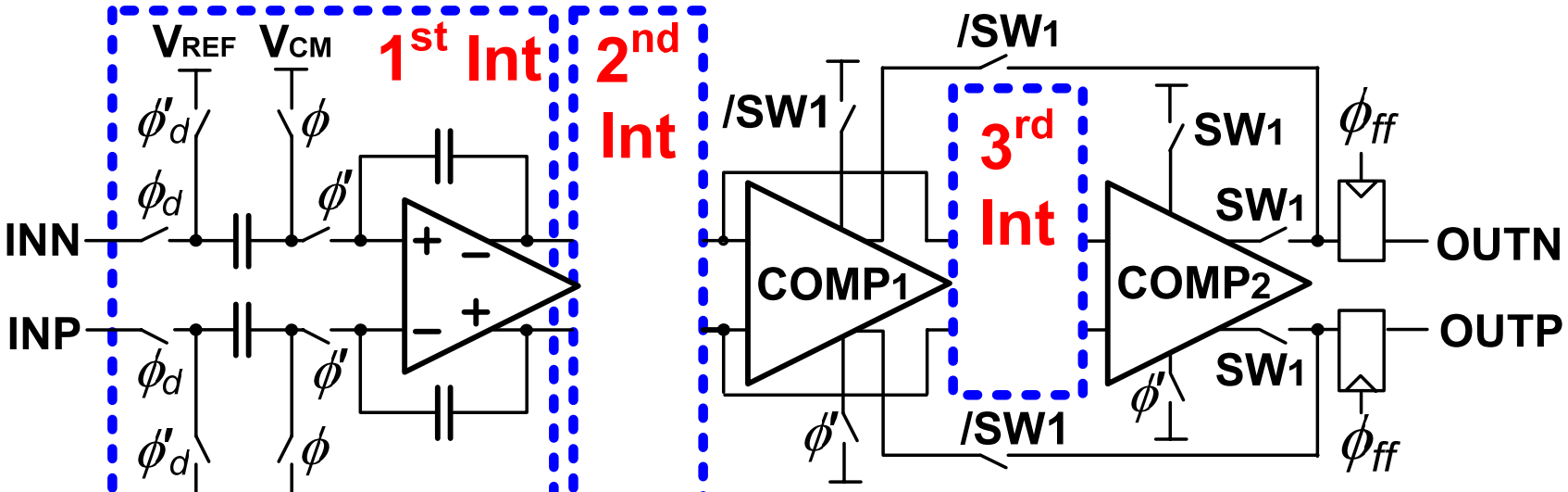


Adaptive SNR



- SW_1 determines the number of integrators
- SW_2 decides the clock frequency

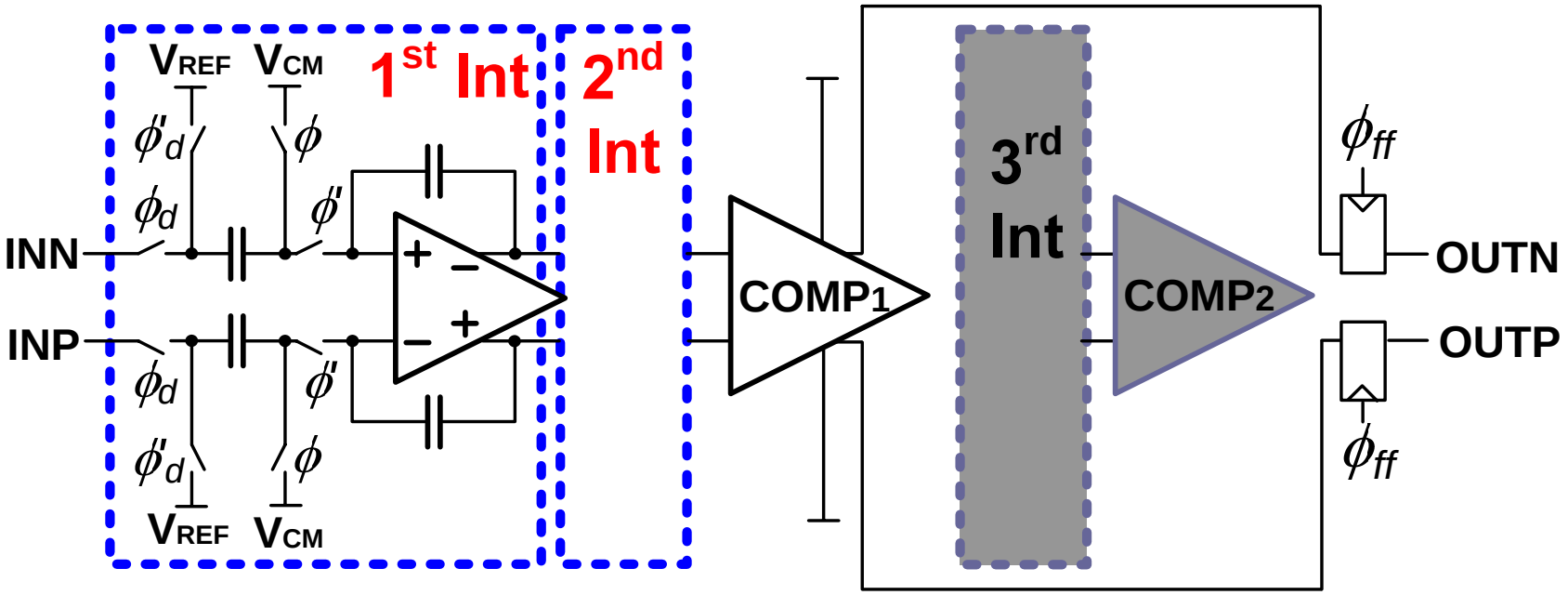
Details of Adaptive SNR Σ-Δ Modulator



	Type1	Type2	Type3	Type4
SW1	off	off	on	on
SW2	off	on	off	on

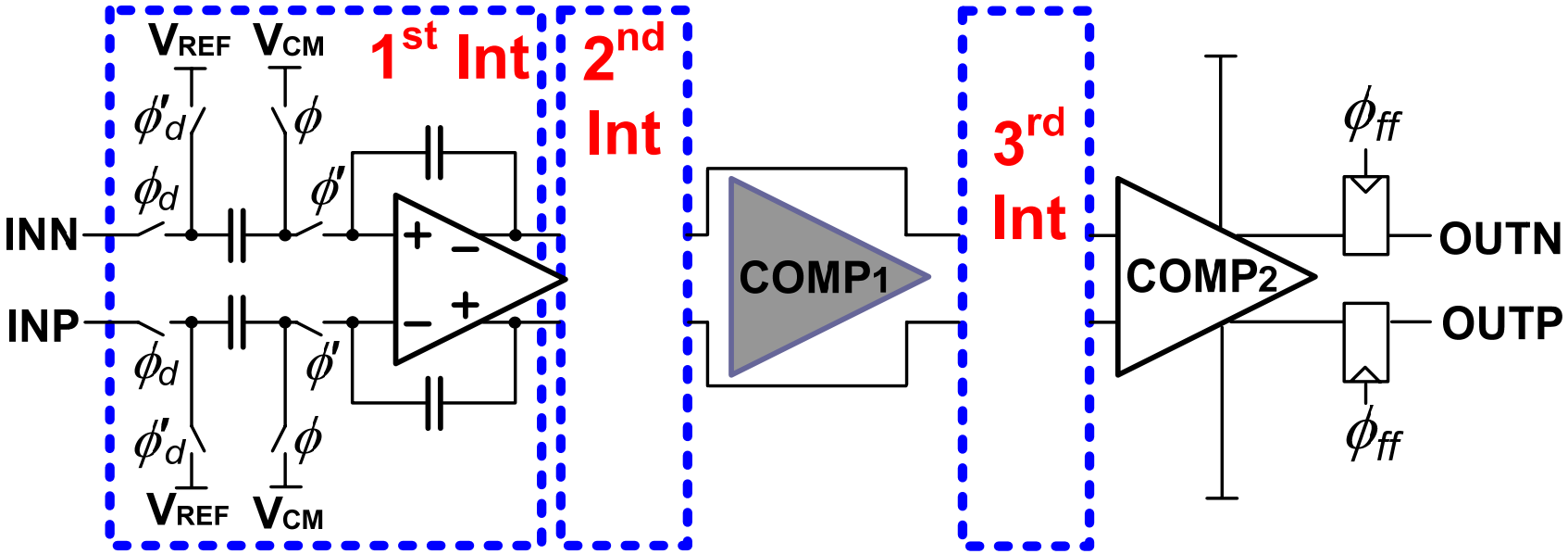
- The combination of SW_1 and SW_2 allows the Σ-Δ modulator to obtain four kinds of SNR

2nd order Σ-Δ Modulator



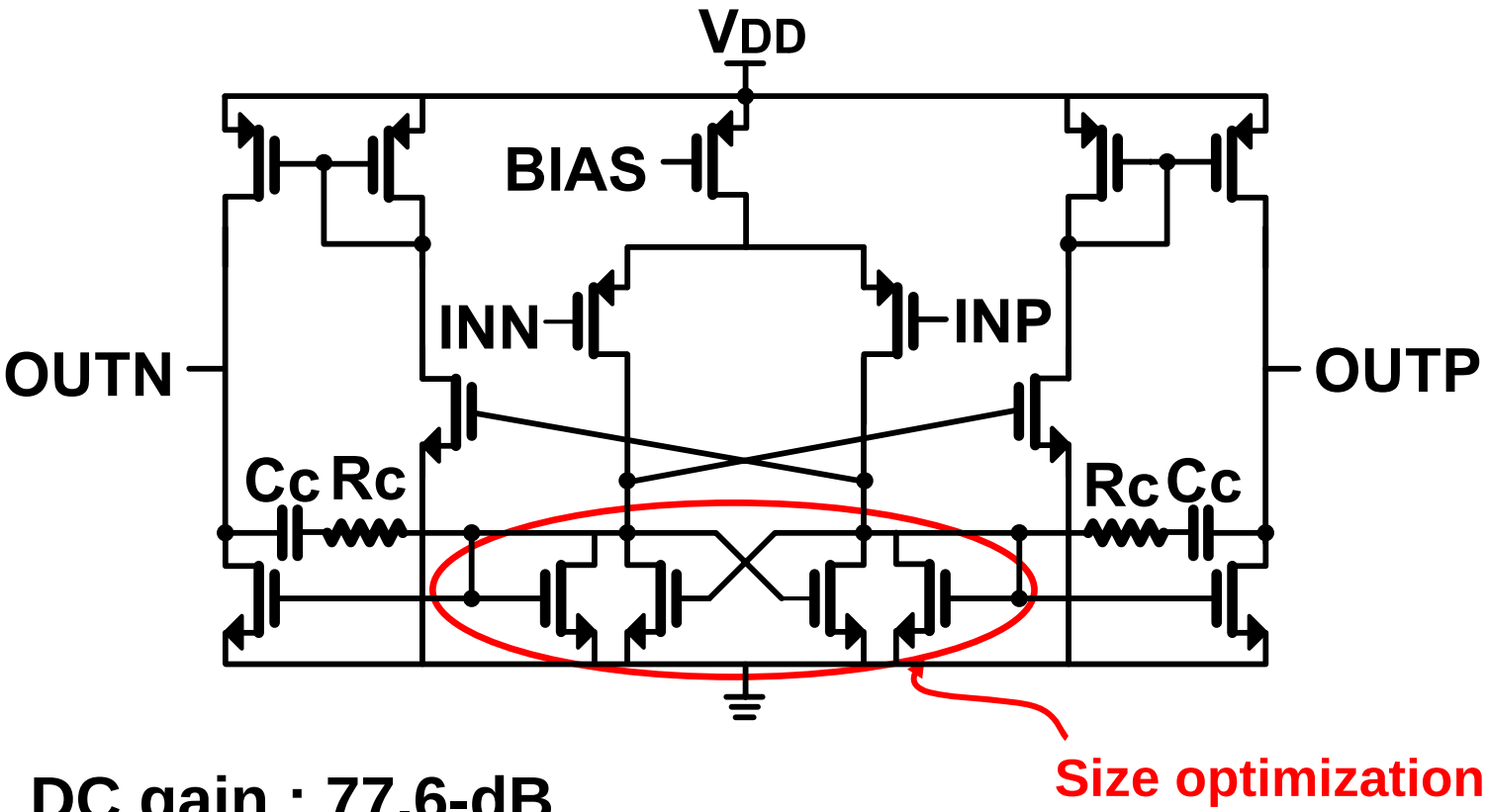
- 2nd order Σ-Δ modulator when the /SW$_1$ is closed

3rd order Σ-Δ Modulator



- 3rd order Σ-Δ modulator when the /SW$_1$ is opened

Low Power OTA



- DC gain : 77.6-dB
- Unity gain bandwidth : 7.07-MHz
- Phase margin : 55° @ 3-pF load
- Power Consumption : 15-μW

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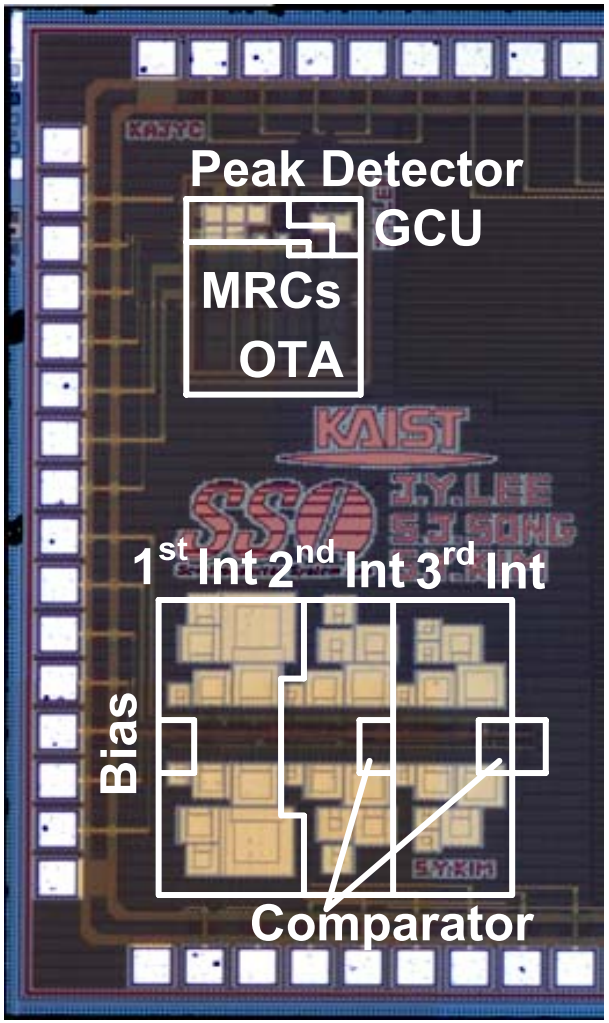
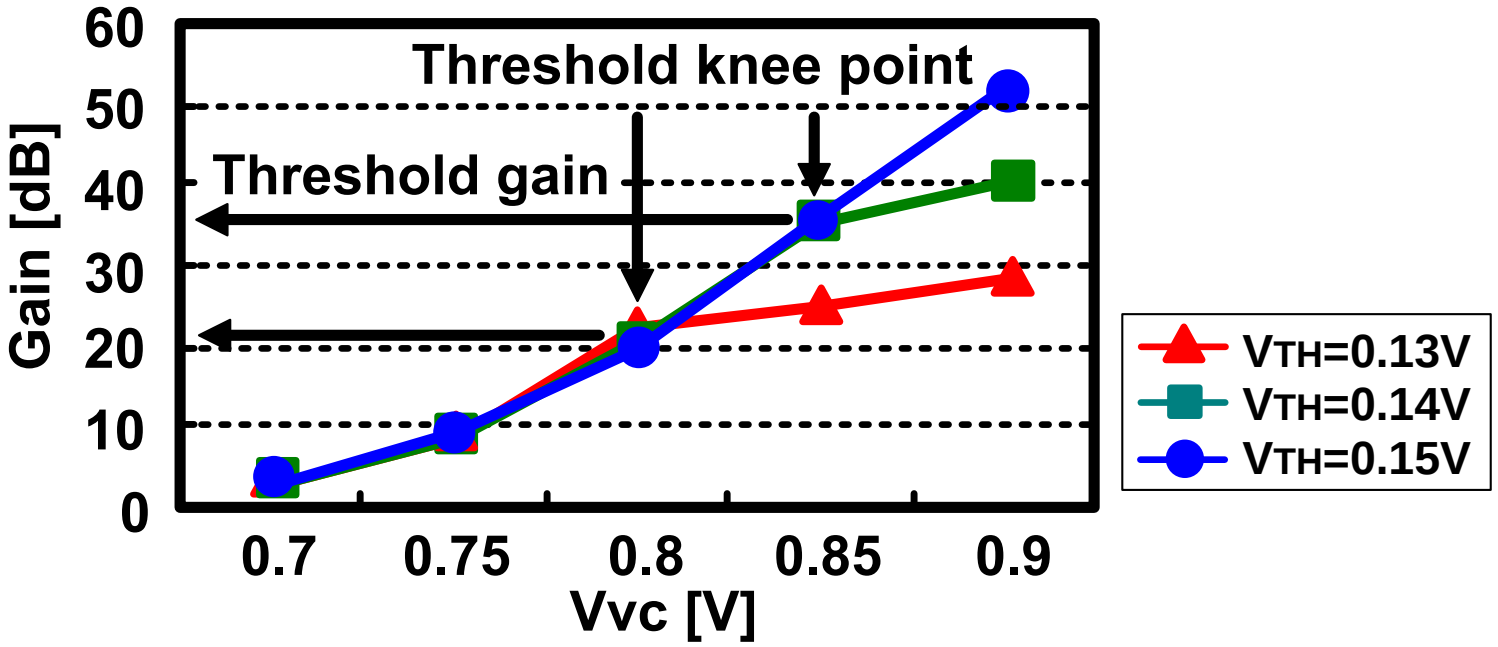
Chip Microphotograph



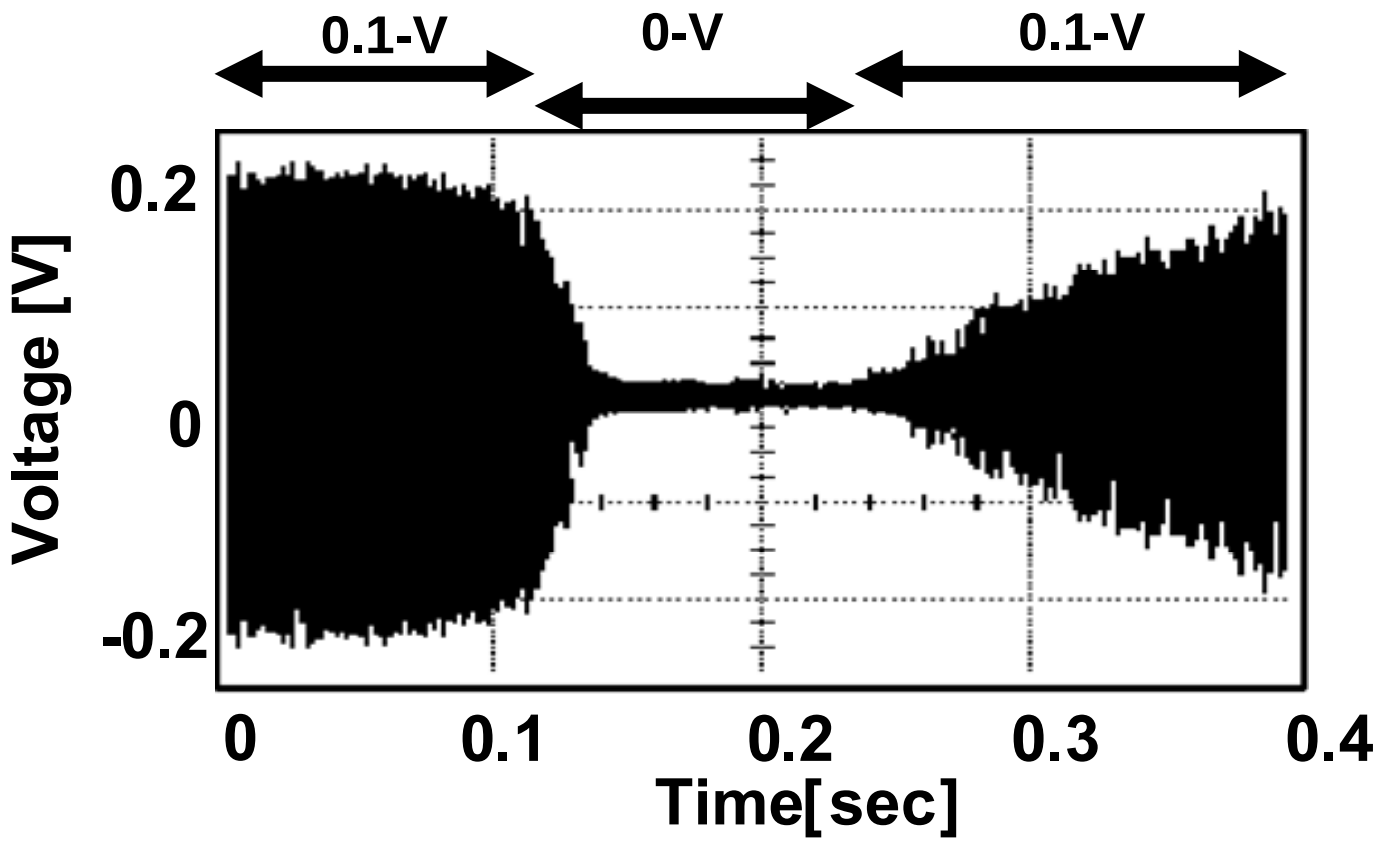
- 0.25-μm CMOS Process
- 0.9-V supply voltage
- 0.5-mm² active area
  - Preamplifier : 0.1-mm²
  - Σ-Δ Modulator : 0.4-mm²
- Power consumption
  - < 74.7-μW
- Peak SNR
  - 72-dB(2nd), 86-dB(3rd)

Measured Performance - CGC Preamplifier



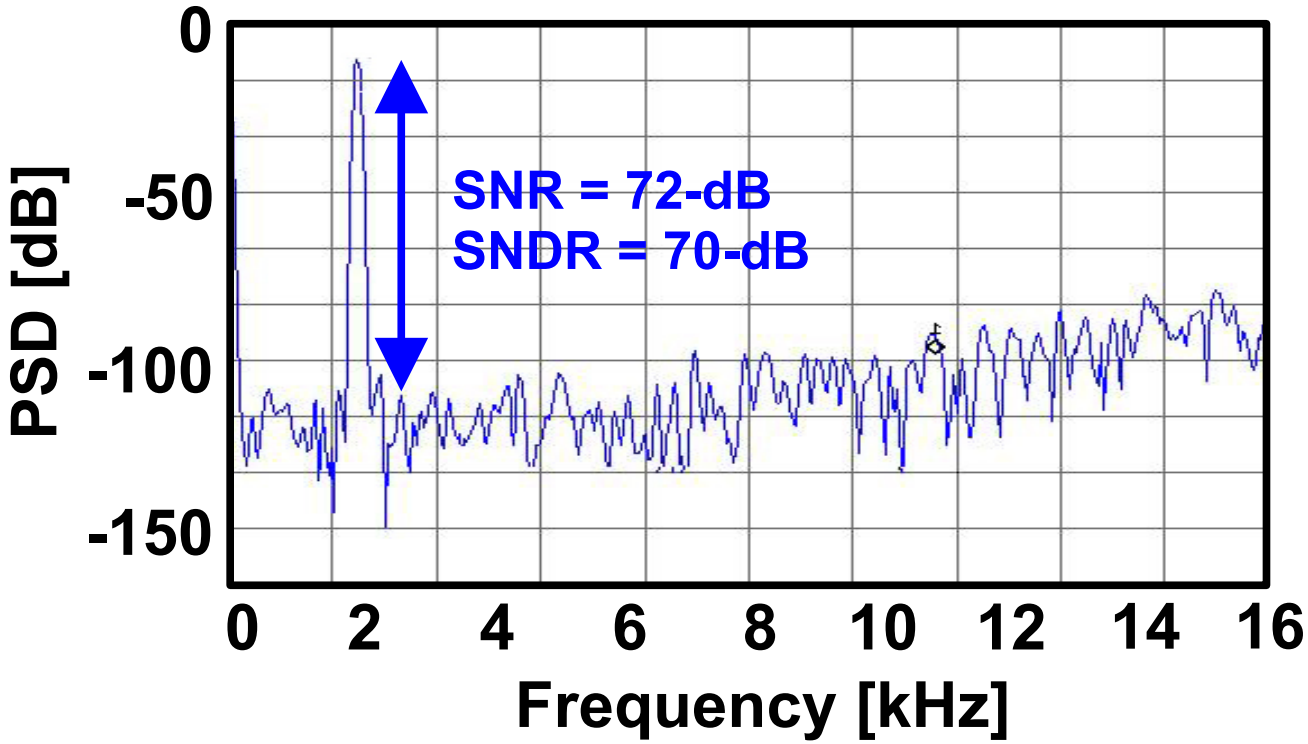
- By reducing V_{TH}, the threshold knee point is decreased simultaneously

Attack and Release time - CGC Preamplifier



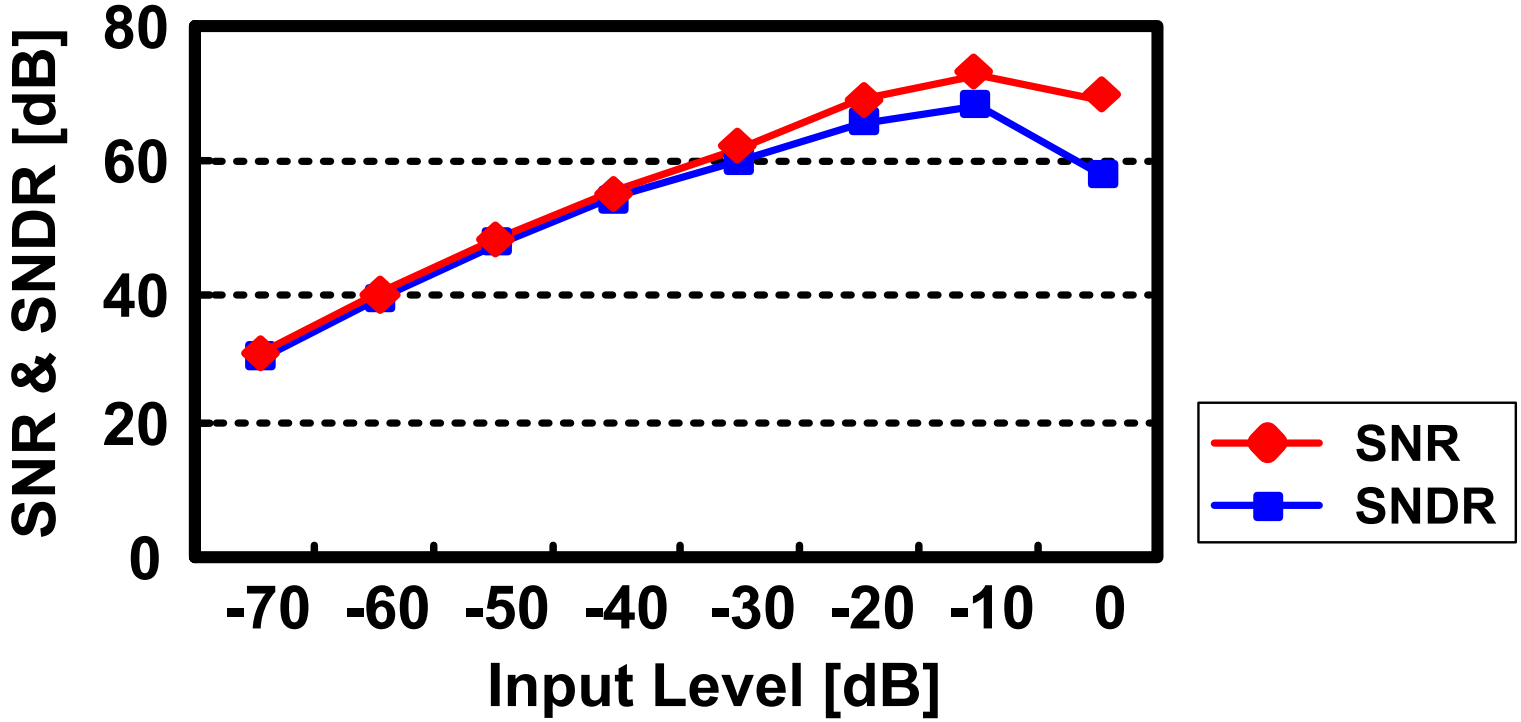
Measured attack and release response

Measured SNR
- Adaptive SNR Σ-Δ Modulator



Measured output spectrum

SNR variation
- Adaptive SNR Σ-Δ Modulator



Measured SNR/SNDR versus input amplitude

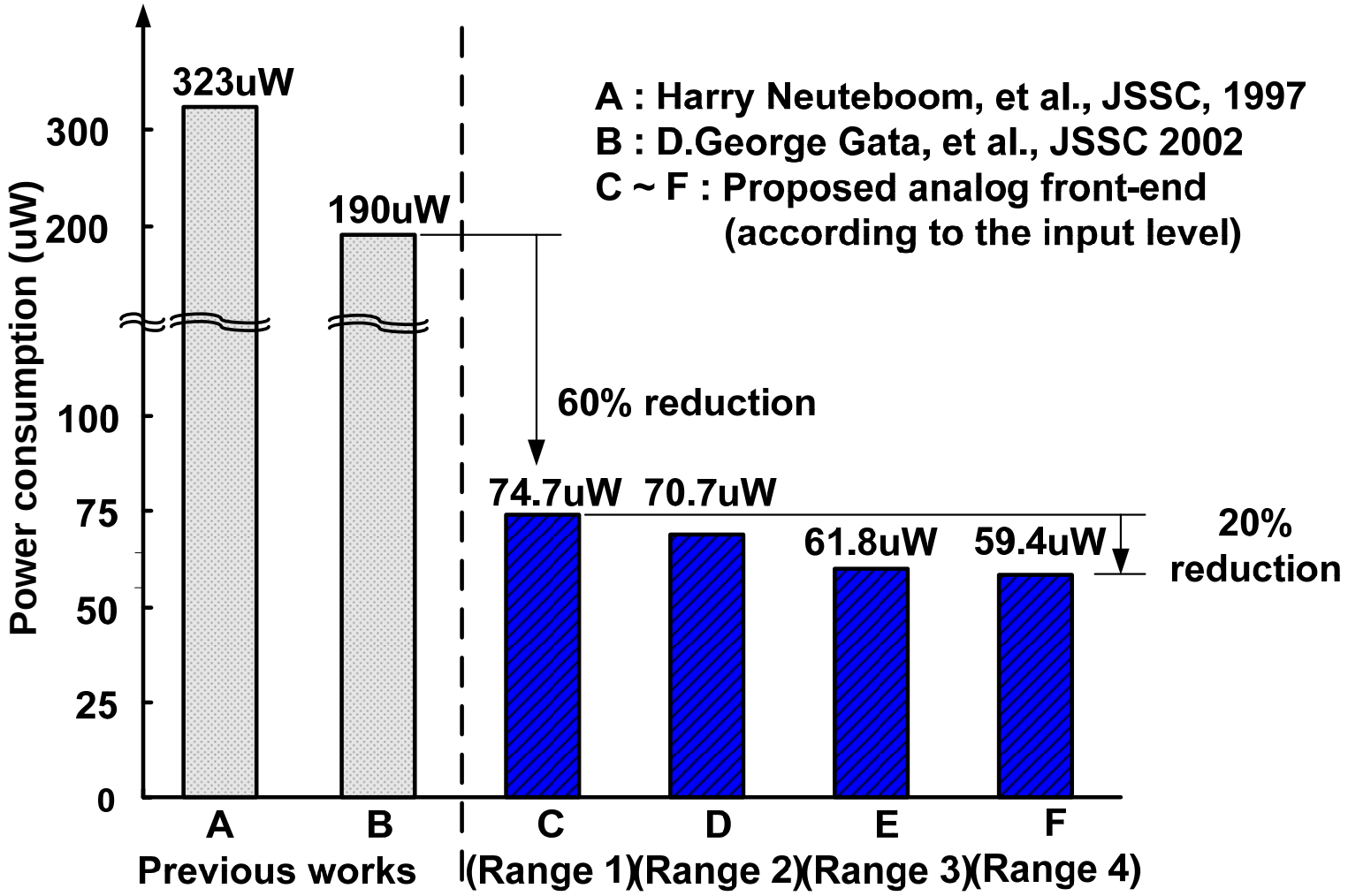
Performance Summary

Supply voltage	0.9-V			
Order	2nd order		3rd order	
Type	1	2	3	4
Clock frequency (MHz)	1.024	2.048	1.024	2.048
Peak SNR	72-dB	81-dB	78-dB	86-dB
Power dissipation (Σ-Δ Modulator)	26.4-μW	26.8-μW	35.7-μW	36.7-μW
Power dissipation (Preamplifier)	Vvc=0.75	Vvc=0.8	Vvc=0.85	
	33-μW	35-μW	38-μW	
Total power dissipation (Analog front-end)	59.4-μW ~ 74.7-μW (According to the parameter value)			
Signal bandwidth	8-kHz			

Performance Comparison

	Supply Voltage	Power Consumption	Peak SNR	Process (CMOS)
JSSC 1997 [Harry Neuteboom]	2.15-V	323-μW	77-dB	0.8-μm
JSSC 2002 [D. George Gata]	1.1-V	190-μW	92-dB	0.6-μm
This work	0.9-V	59.4-μW	86-dB	0.25-μm

Power Consumption Comparison



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Conclusions

- **Digital Hearing Aid Preamplifier with Combined Gain Control**
  - **Controllability and Wide dynamic range**
  - **Low power consumption**
- **Σ-Δ Modulator with Adaptive-SNR**
  - **Optimized Power consumption wrt input condition**
- **Average power consumption of the proposed Hearing Aid Front End**

  < 74.7-μW @ 0.9-V Supply

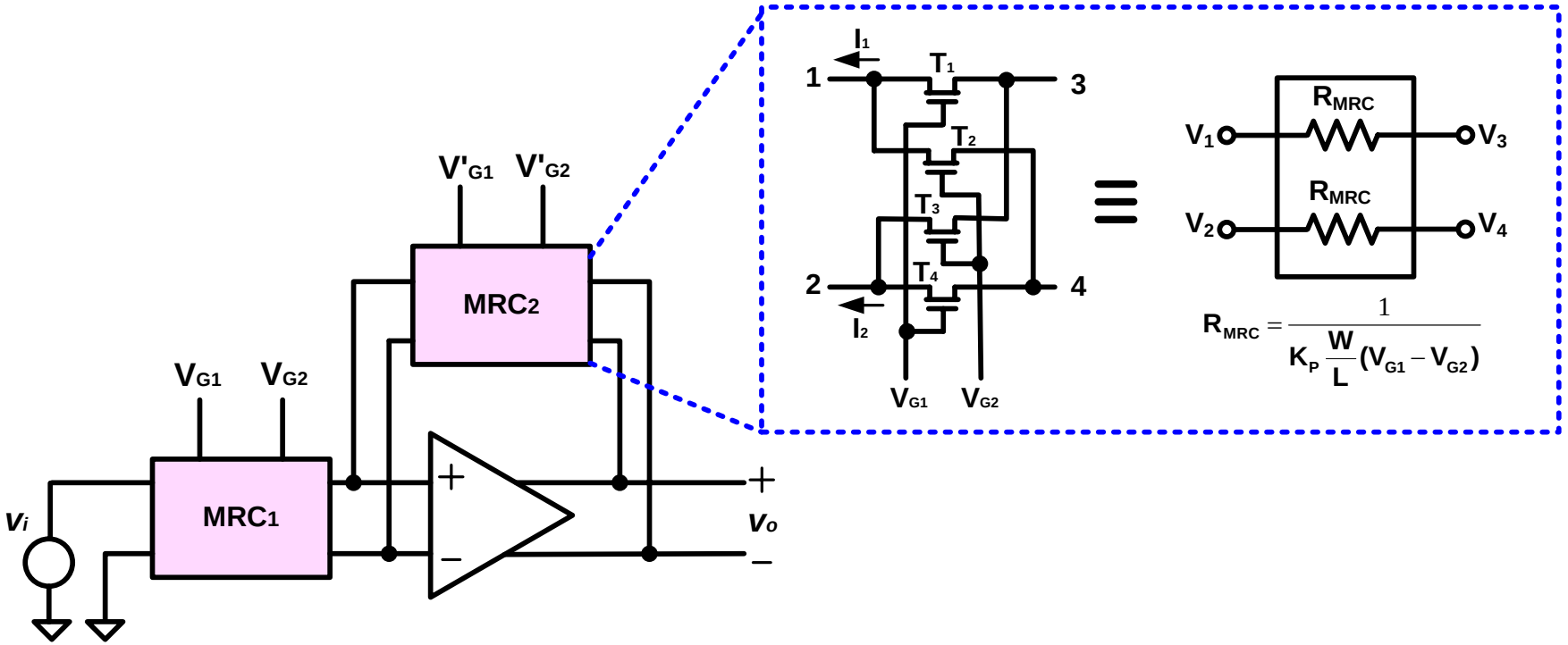
Further Works

- **Design and Implementation of Digital Hearing Aid with Combined Gain Control and Adaptive-SNR**

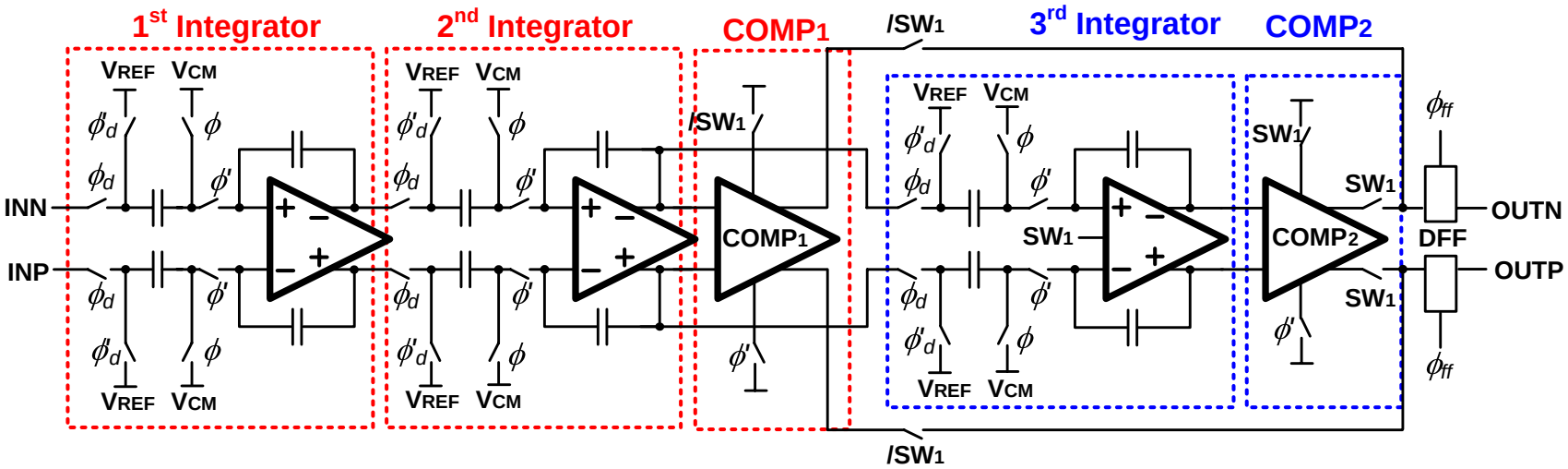
Supplementary

CGC Preamplifier

- **Opamp. with MOS Resistive Circuit (MRC)**
  - **Small Area**
  - **Ease of Tunability for Future AGC**



Details of Adaptive SNR Σ-Δ Modulator



(a) Schematic of the Adaptive SNR Σ-Δ Modulator

(b) Timing diagram of the clock