USB-OTG용 고정밀 Regulated Charge Pump의 설계 및 구현

Design and Implementation of Regulated Charge Pump with High Precision for USB-OTG Application

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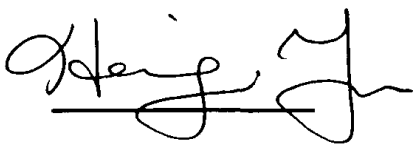
Approved by



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USB-OTG용 고정밀 Regulated Charge Pump의 설계 및 구현

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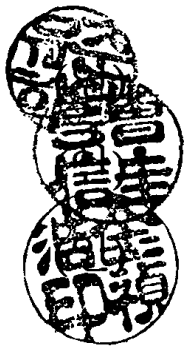

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Abstract

A regulated charge pump circuit is realized in a 3.3V 0.13-um CMOS I/O technology. The regulated charge pump exploits 'Automatic Driving Buffer' scheme to generate 5V constant output voltage which is independent of load current and to lower output ripple voltage under 40mV with 2uF load capacitor.

To make stable output voltage, the regulated charge pump detects the variation of output boosted voltage which is higher than power supply voltage. As the variation of detected output voltage, 6-bit control signal is obtained and controls the 'Automatic Driving Buffer' which is composed of four parallel buffers. The 'Automatic Driving Buffer' operates selectively by 'Driving Buffer Size Control Unit' and controls pumping current with 6-bit control signals. Therefore, by controlling of pumping current as the variation of boosted output voltage, the regulated charge pump generates stable boosted output voltage.

At simulation, the operation with the variation of process,

voltage, temperature is checked and the performance of proposed charge pump is compared with that of conventional charge pump. Test chips demonstrate the boosted output voltage to be 5V and 30mA load current with 500KHz input clock signal. The output ripple voltage is less than 40mV with 2uF load capacitor.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Most of today's portable devices are moving towards the Universal Serial Bus (USB) electrical interface as a way of connecting to a PC. Although USB works well as desktop interface, it is not well suited for portable devices. The PC should act as host (or master), and all other devices are peripherals (or slaves). Hosts cannot connect to hosts, and peripherals cannot connect to peripherals. But in December 2001, the USB On-The-Go (OTG) was announced. USB-OTG supports point-to-point connectivity for data exchange without PC. In other words, portable devices can act as hosts in USB-OTG and communication between portable devices has become possible. But hosts are required to supply large current. Because to function as a host, a device must include adequate storage for a large number of device drivers, and be capable of sourcing a large current. Therefore transceiver of USB-OTG, the USB physical layer, should be capable of supplying large current. In addition to the capacity of supplying large

current, hosts should provide stable output voltage which has constant value and small ripple. If a host provides unstable output voltage, a peripheral which uses the power host provides will not act correctly. Especially, the unstable voltage may affect the performance of analog blocks such as gain, sensitivity, bandwidth and so on in peripherals. Hence, in order to be a host, it needs to have a transceiver which is able to supply large current with stable output voltage. This paper proposes a 5V 30mA regulated charge pump circuit which is employed in the transceiver of USB-OTG. And it is implemented in a 3.3V 0.13um I/O CMOS technology. The proposed charge pump architecture generates 5V output voltage from 3.3V power voltage. As process technology of semiconductor develops, power voltage lowers. On the other hand, communication specification of USB is fixed. So voltage boosting from power voltage considering transistor voltage tolerance problem is essential. And by adapting 'Automatic Driving Buffer', the proposed charge pump generates stable output voltage which has constant output voltage independent of load current and small ripple voltage with supplying large current. Therefore the proposed charge pump enhances output voltage precision supplying large current for USB-OTG application.

1.2 Thesis Organization

Chapter 2 will introduce the concept and architecture of USB-OTG. Chapter 3 will analyze basic charge pump and show contribution of proposed charge pump. It has reduced output voltage rising time which shows tolerance for variation of output current and lowers output ripple voltage. The proposed regulated charge pump which is designed and implemented for USB-OTG will be explained in chapter 4. Its building blocks such as main charge pump, output stage detect unit, driving buffer size control unit, automatic driving buffer, warming-up stage will be described. Measurement results of test chips will be presented in chapter 5. Finally, I conclude this thesis in chapter 6.

CHAPTER 2

OVERALL ARCHITECTURE OF USB-OTG

2.1 Concept of USB-OTG

Today, an increasing number of mobile consumer electronics products such as portable digital assistants (PDA), mobile phones, digital cameras, portable storage devices, etc use the USB interface to exchange data with host PCs. Yet as these devices increase in number , sophistication, and portability, there is a growing need to connect them with each other when a PC is not available. For example, many USB digital cameras can download data to a PC-based application, but cannot connect directly to a USB printer or CD burner to print or store the photos. To meet the requirement, the popular USB standard was recently enhanced to include 'On-The-Go' (OTG) functionality enabling point-to-point data exchange between mobile products. USB-OTG supports both traditional host-based (PC) and device-to-device connectivity. The changes in OTG aim primarily to extend usage of

USB by including more practical specifications and user-friendly features for mobile device. By enabling point-to-point connectivity between and formerly peripheral-only devices, OTG opens up a range of new applications in the mobile/portable space from battery-powered handheld products to non-portable peripherals. Table 2.1.1. shows a list of some of the many data exchange tasks made possible by OTG capabilities.

OTG HOST	PERIPHERAL	TASK
PDA	PDA	Exchange files
	Mobile phone	Surf Web, Send e-mail
	Digital Camera	Exchange pictures
	Keyboard	User Interface
	Printer	Print pictures
	GPS	Get direction
Mobile phone	Digital Camera	Upload pictures
	MP3 Player	Up/Download music
Digital Camera	Printer	Print pictures
	Mass storage	Store pictures
Digital audio	CD player	Upload songs
	Speaker	Play songs
	Storage	Retrieve songs

Table 2.1.1. List of data exchange by USB-OTG

2.2 Architecture of Transceiver in USB-OTG

USB-OTG transceiver enables USB ASICs, FPGAs, or any system chipset with built-in USB host/device functionality (but without a USB transceiver) to interface with the USB physical layer. It transmits and receives serial data at both full speed (12Mbit/s) and low speed (1.5Mbit/s). It is composed of charge pump, bandgap reference, comparators, ID-pin detector, and level shifter. Overall architecture of transceiver is Fig. 2.2.1.

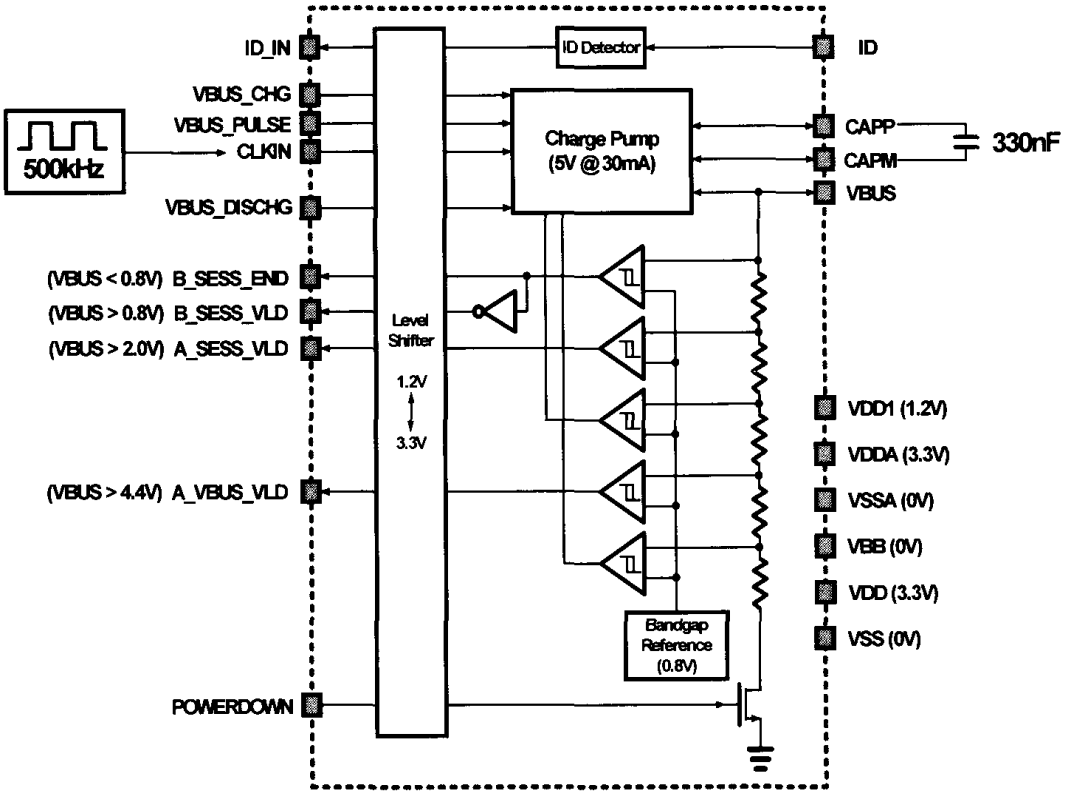


Fig. 2.2.1. Overall architecture of transceiver

Key features of transceiver is like this

1. Fully Compliant with USB Specification Rev. 2.0., and the OTG Supplement to the USB Specification Rev. 1.0.

2. Ideal for systems ASICs, FPGAs, or chipsets with a built-in USB-OTG dual-role core

3. Supports both full-speed (12Mbit/s) and low-speed (1.5Mbit/s) data transfer rates

4. Flexible general-purpose buffer mode supports serial communication interfaces used with UARTs

5. Global power down mode reduces power consumption to bare minimum

6. Supports mini USB audio interface

7. Supports data line VBUS pulsing session request

8. Contain HNP command and status registers

2.3 Specification of Transceiver in USB-OTG

2.3.1 Charge pump

- Voltage conversion : 3.3V input, 4.4~5V output
- Current requirement : 8mA~30mA
- Efficiency should be better than 70%
- Rising time (from 0V to 4.4V) < 100msec
- Disable mode : VBUS < 0.2V
- External Cmax : ~500nF
- Input clock : 500KHz
- Worst case ripple : 50mV
- 5V input tolerance

2.3.2 Bandgap Reference

- Accurate 0.7V reference voltage for comparators

2.3.3 Comparator

- 4 comparators needed : threshold voltage (0.7V, 1.5V, 3V, 4.55V)
- Hysteresis 50mV
- 5.5V input tolerance

2.3.4 ID-pin Detector

- 2 level detectors are needed. (GND, floating)

2.3.5 Level Shifter

- 2 types of voltage level shifters are needed
- From 1.2V to 3.3V
- From 3.3V to 1.2V

CHAPTER 3

CONVENTIONAL CHARGE PUMP

In principle, charge pump is a circuit which generates higher voltage than that of power supply. As it is used as a power supply unit, the performance of charge pump affects the whole operation of powered-circuit. Especially, in case of analog blocks which is very sensitive to power noise, the performance of charge pump greatly affects operation of analog blocks such as gain, sensitivity, bandwidth, and etc. Therefore charge pump should provide stable power voltage with minimum noise.

Main features of charge pump can be classified into three categories. These categories are not actually distinct, but they need to be illustrated as a design approach. The three categories encompass the large current, small ripple, and high voltage. The goal of this chapter is to analysis of these three features in a conventional charge pump and to show the performance enhancement of proposed charge pump.

3.1 Operation of Conventional Charge Pump

To generate higher voltage than that of power supply, charge pump is essential, which uses bootstrapping scheme. Bootstrapping scheme is to boost voltage at floating node. Schematic of conventional charge pump is shown in Fig. 3.1.1.

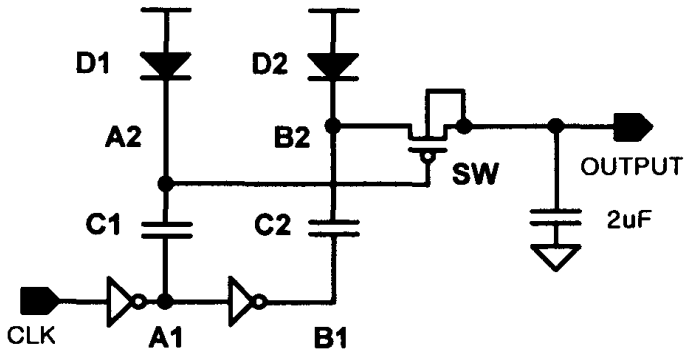


Fig. 3.1.1. Schematic of conventional charge pump

When A1, B1 node voltages are low and high separately, capacitor, C1, is charged from power through diode, D1. A2 node voltage charges up to power supply voltage and SW transistor turns on. Then bootstrapped B2 node voltage is delivered to the output stage through SW transistor. As A1 node voltage rises, A2 node voltage becomes higher and diode, D1, turns off to make A2 node float. Floating node, A2, is bootstrapped by A1, totally turning off SW. A2 node is used for

blocking leakage current by perfectly turning off SW. C2 capacitor is charged from power through diode, D2. Next time A1, B1 node voltages goes low and high again. Then A2 node voltage charges up to power supply voltage and SW transistor turns on. And bootstrapped B2 node voltage is delivered to the output stage through SW transistor. The electrical charge at C2 is used to supply output current when B2 node voltage is bootstrapped. By repeating this operation, output voltage which is higher than power supply can be generated.

3.2 Analysis of Conventional Charge Pump

The typical waveform of the circuit which is shown in Fig 3.1.1 will be shown in Fig. 3.2.1.

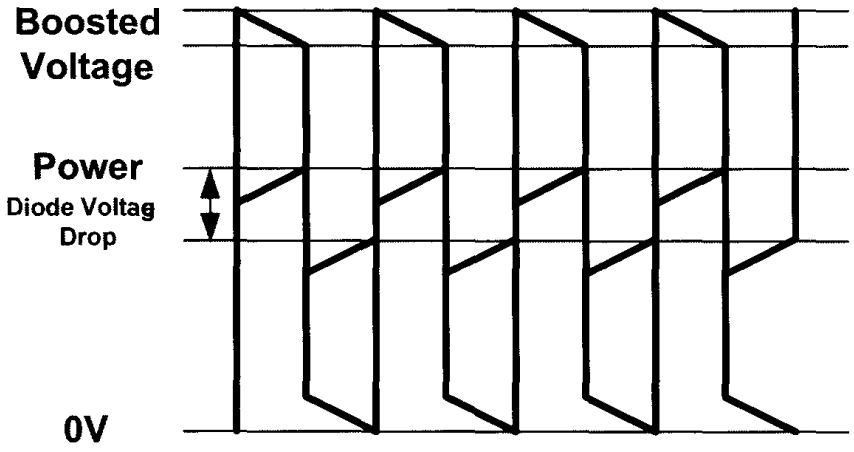


Fig. 3.2.1. Node B1, B2 waveform of conventional charge pump

As can be seen, node B1 voltage swing is from 0V to power voltage. and B2 node voltage is bootstrapped. The difference of between the voltages of B1 and B2 nodes is given by

$$Q = CV \quad (1)$$

where B_2 is the boosted voltage, B_1 is the voltage swing due to capacitive coupling form the clock, V_{POWER} is the voltage of power supply, V_D is the forward bias diode voltage, and V_L is the voltage by

which the capacitor is charged and discharged when charge pump is supplying an output current, I_{OUT}.

The current supplied by the charge pump at a clock frequency, f, is given by

$$I_{OUT} = 2fC_2V_L \tag{2}$$

where C_2 is pumping capacitor which supplies output current.

Substituting for V_L in (1), we get

$$B_2 - B_1 = V_{POWER} - V_D - \frac{I_{OUT}}{2fC_2} \tag{3}$$

Rearranging, we get

$$B_2(V_{OUT}) = B_1 + V_{POWER} - V_D - \frac{I_{OUT}}{2fC_2} \tag{4}$$

There is also a ripple voltage, V_R, at the charge pump output due to the load resistance, R_L, discharging the load capacitance, C_{LOAD}. Usually, C_{LOAD} is sufficiently large for V_R to be small compared to V_{OUT}, so that

$$V_R = \frac{I_{OUT}}{fC_{LOAD}} \tag{5}$$

As can be seen in (4), (5), output voltage is proportional to

frequency and pumping capacitor and inverse proportional to output current, and ripple voltage is also inverse proportional to output current, and proportional to frequency and load capacitor. Therefore, it is hard to make high voltage and small ripple voltage with large output current.

3.3 Contribution to Charge Pump

The proposed charge pump can contribute to conventional charge pump with two aspects. The first enhancement of proposed charge pump is to reduce rising time. In case of conventional charge pump, rising time from 3V to 5V is about 150us, but in case of proposed charge pump, rising time is reduced to 40us. This performance enhancement means that output voltage is insensitive and fast recovery from variation of load stage.

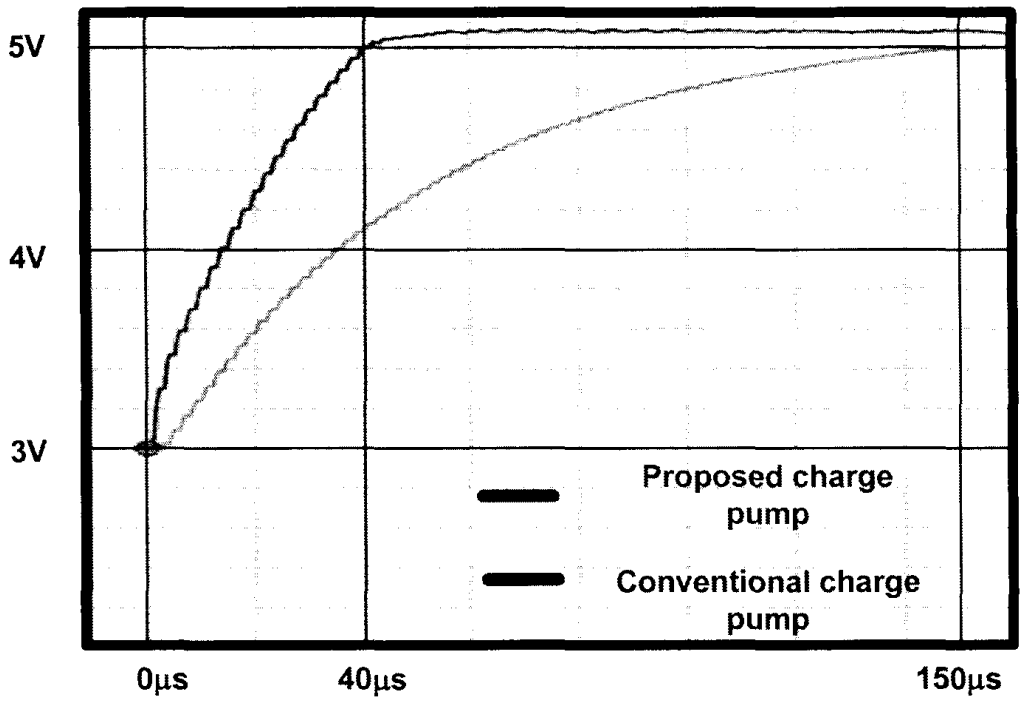


Fig.3.3.1. Performance enhancement of proposed charge pump in rising time

The second performance of proposed charge pump is to reduce output ripple voltage. In case of conventional charge pump, output ripple voltage with 10mA output current is 35mV. On the other hand, output ripple voltage of proposed charge pump is 12mV with supplying 10mA output current. This means that in stable state of output voltage, proposed charge pump can provide stable output voltage with small ripple.

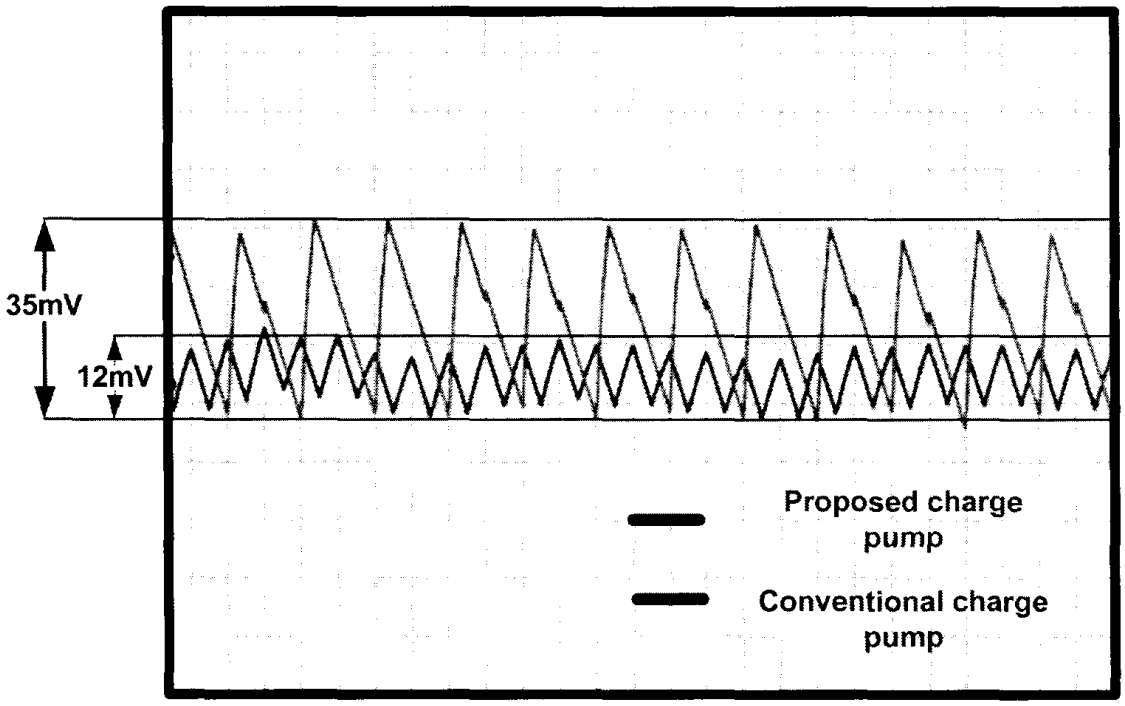


Fig.3.3.2. Performance enhancement of proposed charge pump in ripple voltage

CHAPTER 4

DESIGN AND IMPLEMENTATION OF PROPOSED CHARGE PUMP

Charge pump is used to boost from 3.3V, power voltage, to 5V, VBUS. And it supplies current up to 30mA. Fig 4.1 shows the position of charge pump in USB-OTG. Charge pump is used at output stage of USB-OTG and supply 5V boosted voltage. It uses 330nF external pumping capacitance. Main feature of charge pump in this circuit is that it has small output ripple voltage with large load current. To accomplish this feature, proposed charge pump has five main blocks. The functions of blocks are listed at Table 4.1 and the block diagram of charge pump is shown in Fig. 4.2. The first block of Charge pump is 'Main Charge Pump'. It boosts voltage by using general boot strapping scheme. The boosted voltage is detected by 'Output Stage Detect Unit'. And it informs the voltage level to 'Driving Buffer Size Control Unit'. It controls pumping current to pumping capacitor in 'Main Charge Pump' by sizing the "Automatic Driving Buffer'.

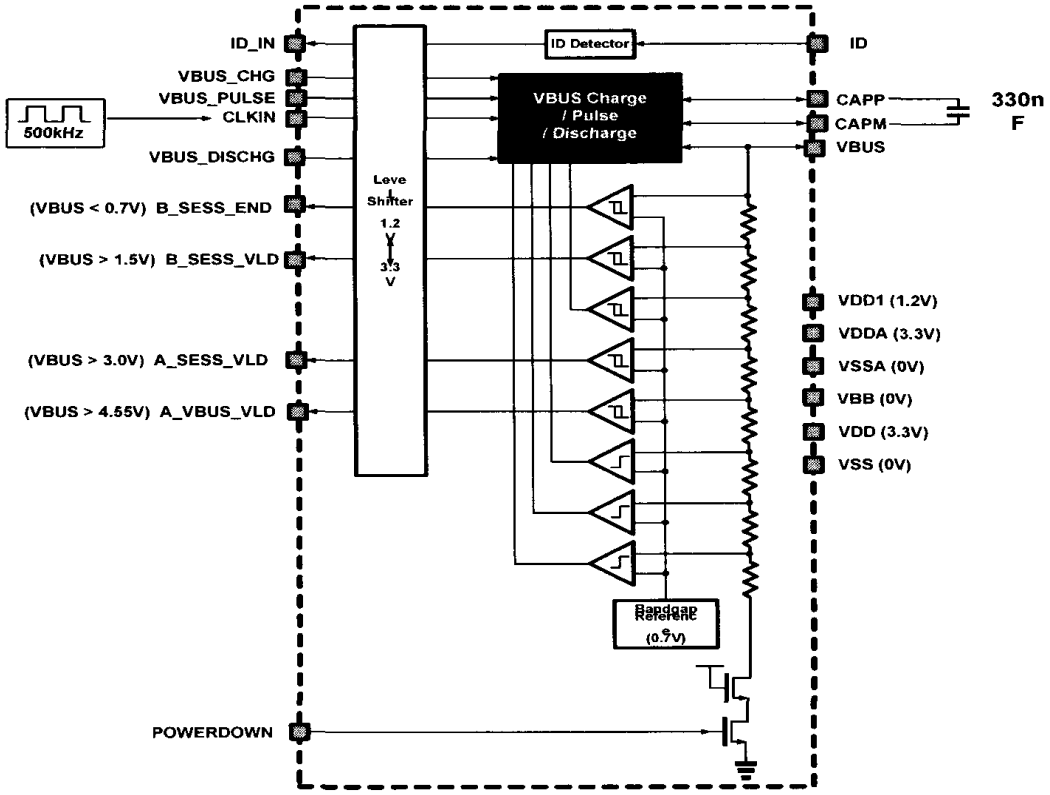


Fig. 4.1. Charge pump in transceiver

Main Charge Pump	To boost power voltage
Output Stage Detect Unit	To detect output voltage level
Driving Buffer Size Control Unit	To control the size of 'Automatic Driving Buffer'
Automatic Driving Buffer	To reduce output ripple voltage
Warming-Up Stage	To prevent breakdown of transistor in charge pump

Table 4.1. Function description of proposed charge pump

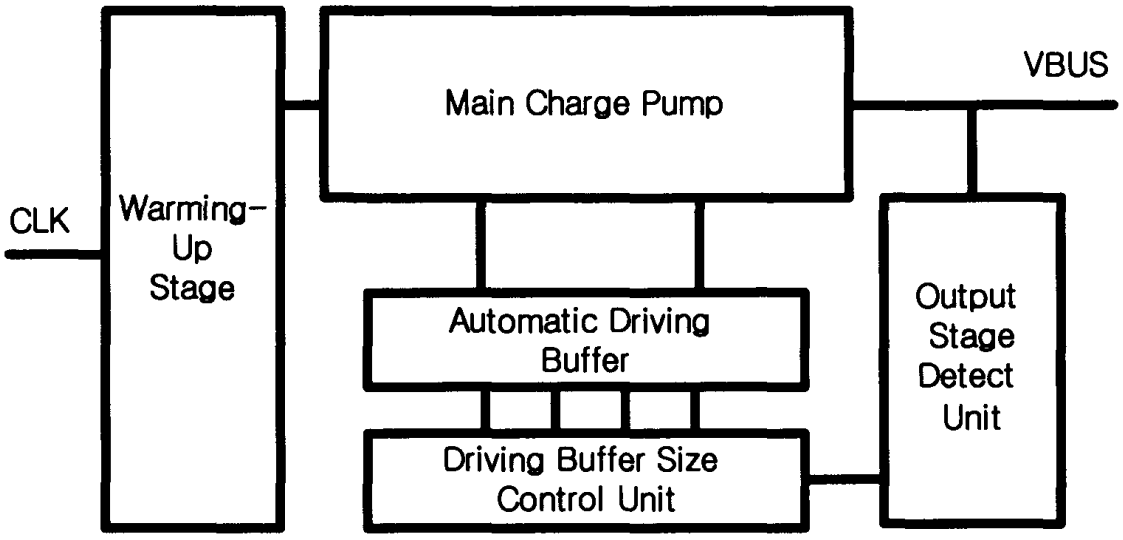


Fig. 4.2. Block diagram of proposed charge pump

4.1 Design of Regulated Charge pump for USB-OTG

4.1.1. Main Charge Pump

'Main charge pump' is the basic charge pump which uses the scheme of boot strapping. It uses 330nF external pumping capacitor to boost voltage with supplying up to 30mA output current. The size of external capacitor is determined by the output load current. To supply large output current, at least 330nF capacitor is needed. Fig 4.1.1.1 shows the position of "Main Charge Pump' in proposed charge pump.

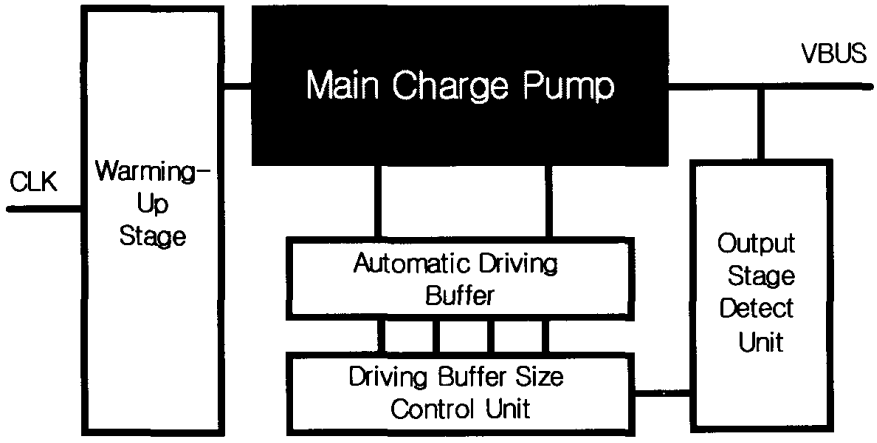


Fig. 4.1.1.1. Main charge pump of proposed charge pump in USB-OTG

Fig 4.1.1.2 shows the schematic of 'Main Charge Pump'. The operation of main charge pump is similar to the operation of conventional charge pump. In the charging cycle, the pumping capacitor is charged by power through diode. and in the pumping cycle, the stored charge in the pumping capacitor

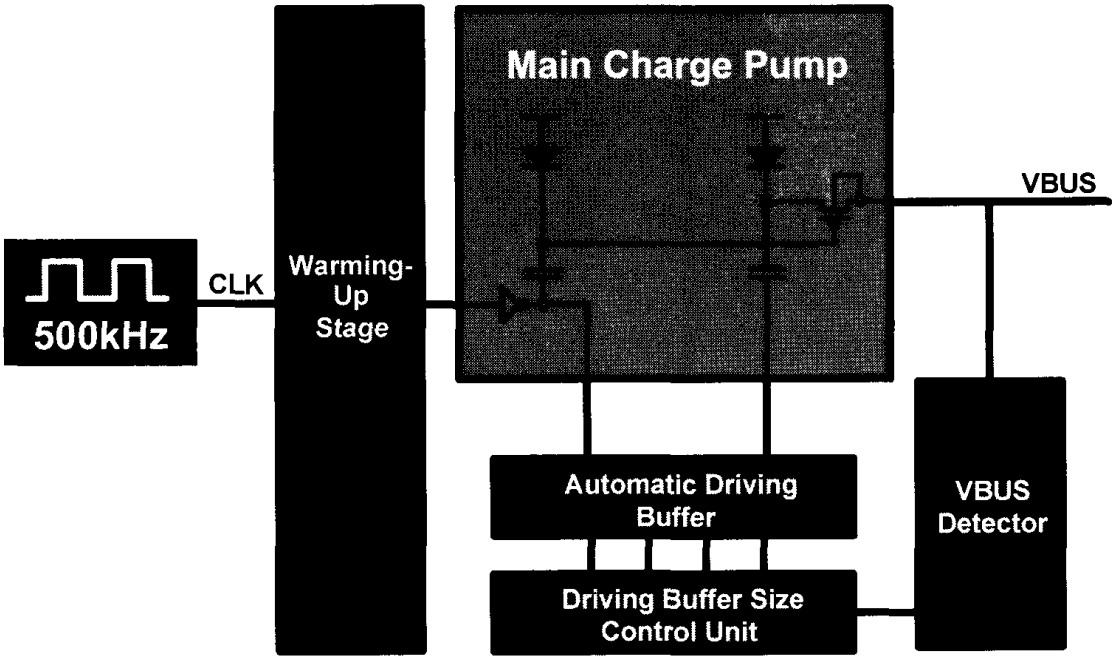


Fig. 4.1.1.2. Schematic of main charge pump

is pumped to the output stage by pumping current. The strength of pumping current is controlled by 'Automatic Driving Buffer'. Therefore the boosted output voltage level is determined by the magnitude of pumping current by this equation.

$$Q = CV \tag{6}$$

$$\frac{dV}{dt} = \frac{dQ}{dt}C \tag{7}$$

The diodes is made by PMOS transistor for preventing the use of triple-well technology.

4.1.2. Output Stage Detect Unit

Main function of output stage detect unit is to detect output voltage level and inform the detected voltage level to driving buffer size control unit. Fig 4.1.2.1. shows the position of 'Output Stage Detect Unit'. Four comparators are used to detect output voltage level. Each comparator detects 2V, 5.0V, 5.05V and 5.1V separately.

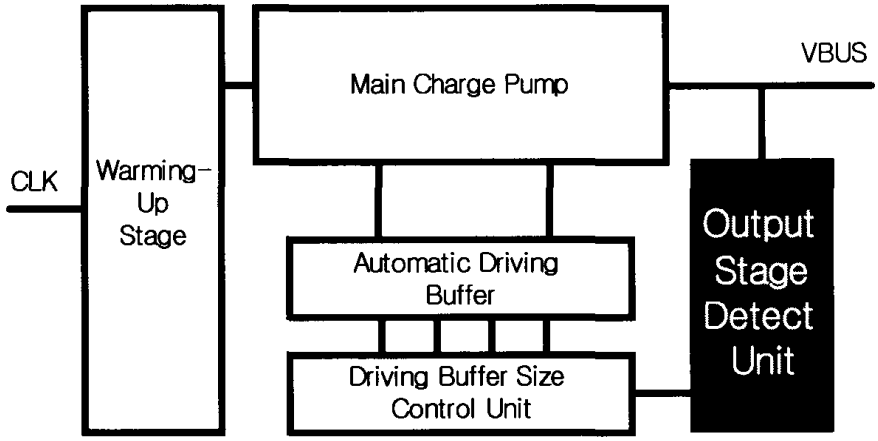


Fig. 4.1.2.1. Output stage detect unit of proposed charge pump in USB-OTG

Fig 4.1.2.2 is the block diagram of 'output stage detect unit'. 2V comparator has 100mV hysteresis and used to prevent breakdown of transistor of 'Main Charge Pump'. Output of 2V detecting comparator is connected to 'Warming-Up Stage'. 'Warming-Up Stage' operates until VBUS is higher than 2V. When VBUS is higher than 2V and output of 2V detecting comparator is '1', 'Warming-Up Stage' stops its operation. 5.0V, 5.05V and 5.1V detecting comparators have no hysteresis and connected to 'Driving

Buffer Size Control Unit'. From these comparators, 'Driving Buffer Size Control Unit' detect VBUS voltage level and controls 'Automatic Driving Buffer'.

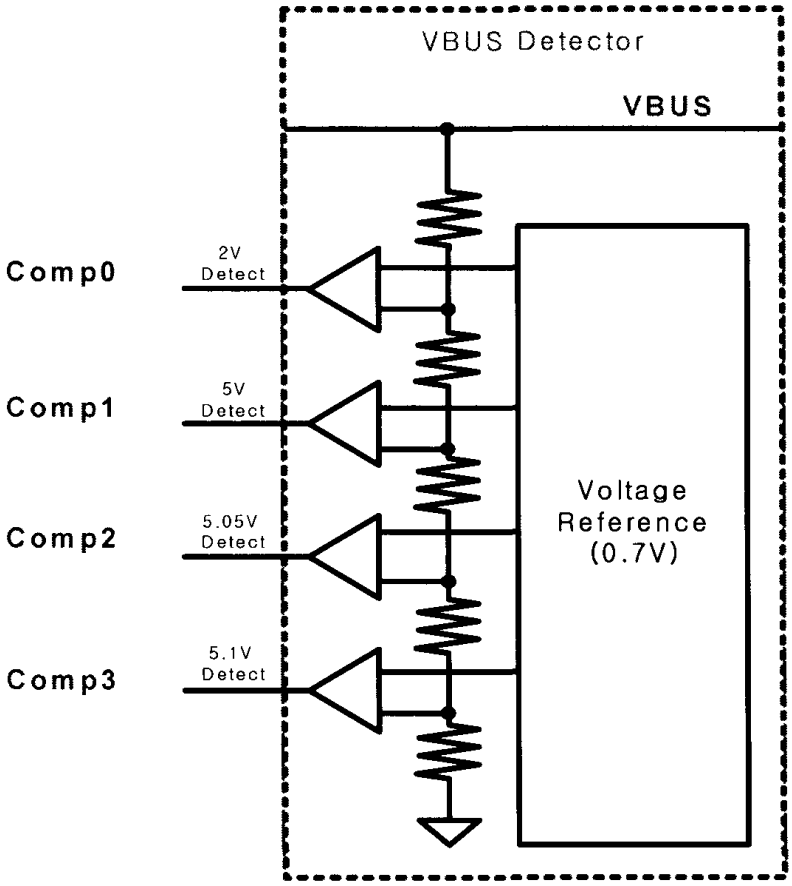


Fig. 4.1.2.2 Block diagram of output stage detect unit

4.1.3. Driving Buffer Size Control Unit

Main function of driving buffer size control unit is to control the size of 'Automatic Driving Buffer'. By controlling the size of automatic driving buffer, VBUS ripple voltage can be reduced because pumping current to pumping capacitor is controlled. Fig 4.1.3.1 shows the position of 'Driving Buffer Size Control Unit' in the proposed charge pump. With the outputs of 5.0V, 5.05 and 5.1V detecting comparators in 'Output Stage Detecting Unit', 'Driving Buffer Size Control Unit' controls driving buffer sizes. In case the VBUS is lower than 5V, 'Driving Buffer Size Control Unit' increases pumping current by controlling "Automatic Driving Buffer'. Meanwhile, in case that VBUS is higher than 5.1V, 'Driving Buffer Size Control Unit' reduces the magnitude of pumping current.

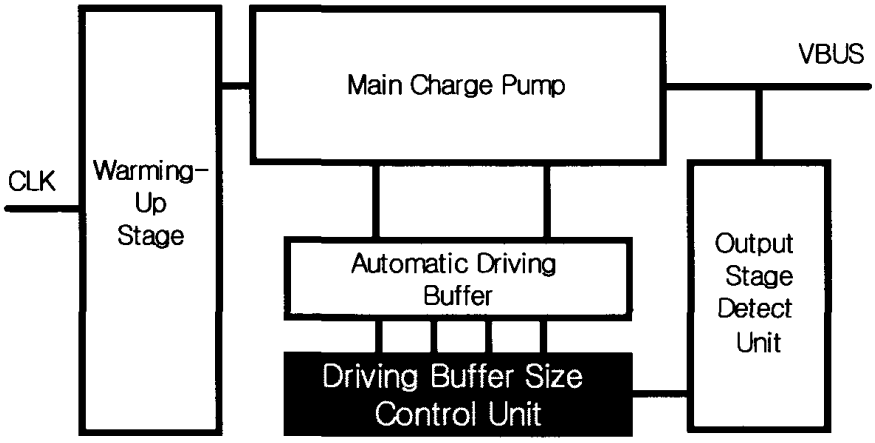


Fig. 4.1.3.1. Driving buffer size control unit of proposed charge pump in USB-OTG

Fig 4.1.3.2. is the schematic of 'Driving Buffer Size Control Unit'. CPM1~3 are connected to the PMOS gate and CNM1~3 connected to NMOS gate in 'Automatic Driving Buffer'. If comp1 is '0', CNM1 and CPM1 are in synchronous with buffered clock. If comp1 is '1', buffer stage in 'Automatic Driving Buffer' connected to CPM1 and CNM1 does not operate. Because CPM which is connected to gate of PMOS is '1' and CNM connected to gate of NMOS is '0'. By using this technique, buffer size of 'Automatic Driving Buffer' is controlled.

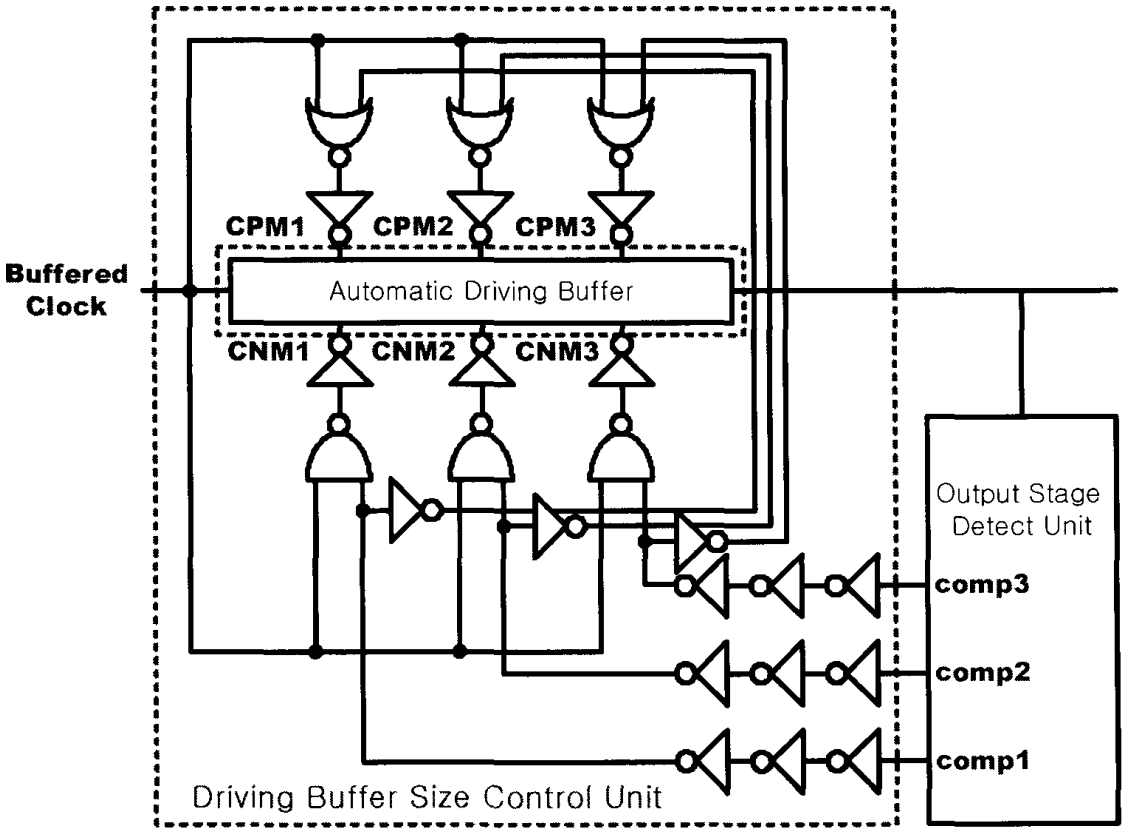


Fig. 4.1.3.2. Schematic of driving buffer size control unit

4.1.4. Automatic Driving Buffer

Main function of automatic driving buffer is to reduce output ripple voltage. The position of 'Automatic Driving Buffer' is shown in Fig 4.1.4.1. It is controlled by 'Driving Buffer Size Control Unit'. Fig 4.1.4.2. shows the schematic of 'Automatic Driving Buffer'. It consists of four buffer stages. The first buffer stage is always in synchronous with buffered clock. The second, third and forth buffer stage may operate or not according to the signal of 'Driving Buffer Size Control Unit'. If all of buffer stage operate, boosting power is the strongest. If only one buffer stage is on, boosting power is the weakest.

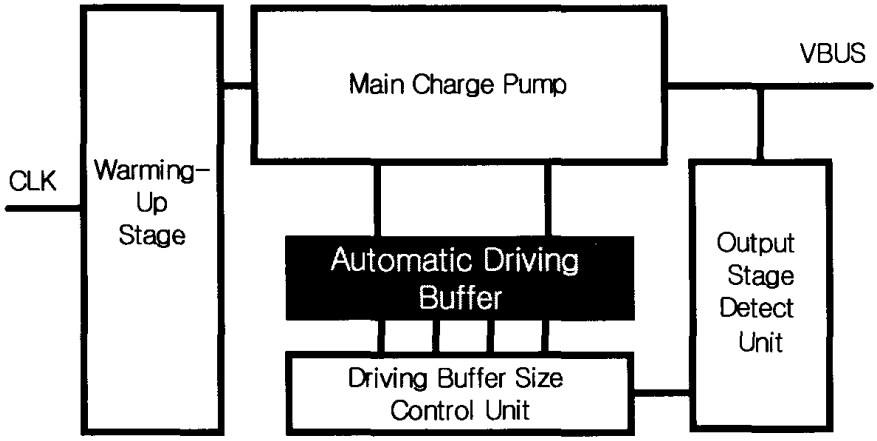


Fig. 4.1.4.1. Automatic driving buffer of proposed charge pump in USB-OTG

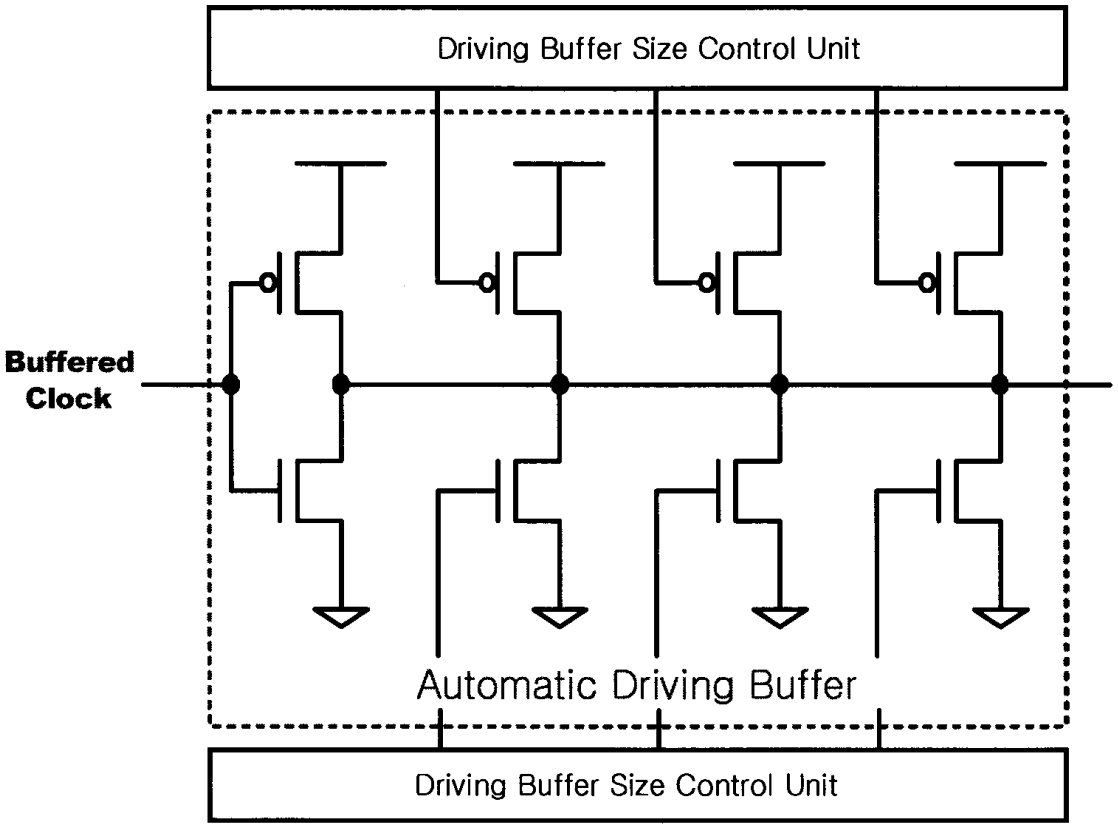


Fig. 4.1.4.2. Schematic of automatic driving buffer

4.1.5. Warming-Up Stage

Warming-up stage is to prevent breakdown of transistor in charge pump. To prevent sudden voltage difference to transistor, warming-up stage is introduced. Warming-up stage is to raise voltage level at drain to specific level before sudden voltage difference is applied to between gate and source of transistor.

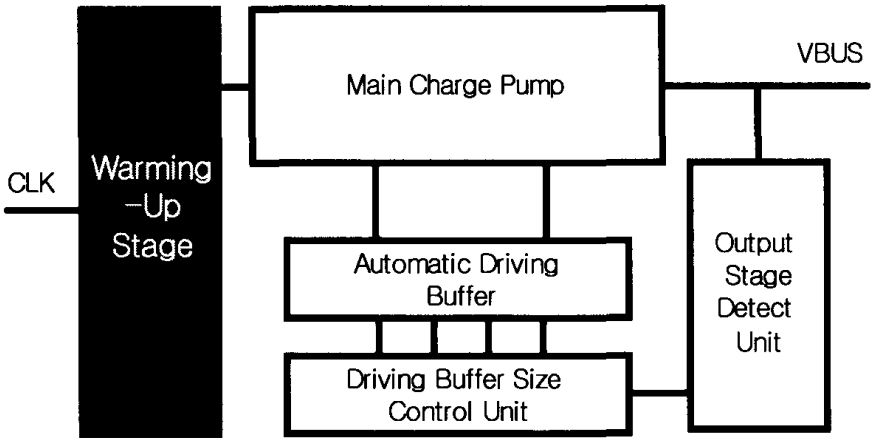


Fig. 4.1.5.1 Warming-up stage of proposed charge pump in USB-OTG

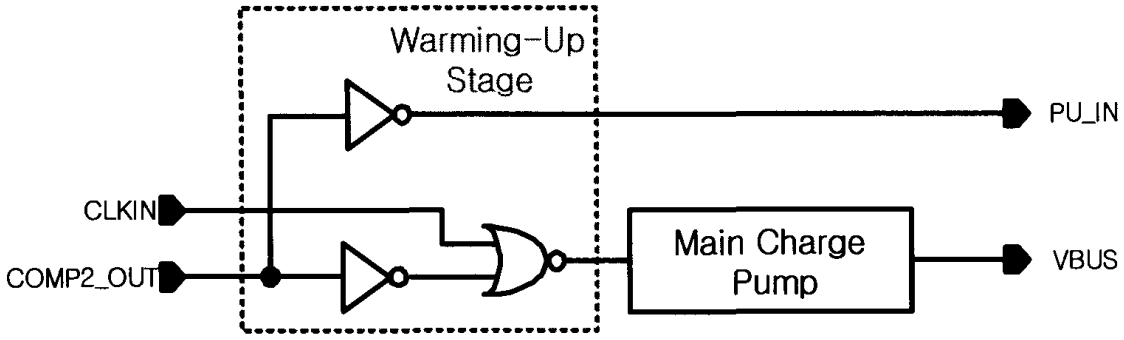


Fig. 4.1.5.2. Schematic of warming-up stage

4.2. Simulation Results

Fig 4.2.1 shows simulation results of proposed charge pump with the variation of process, supply voltage and temperature. Output voltage of charge pump is independent of variations in condition. Output voltage ranges from 4.8V to 5.1V and output ripple voltage is lower than 50mV.

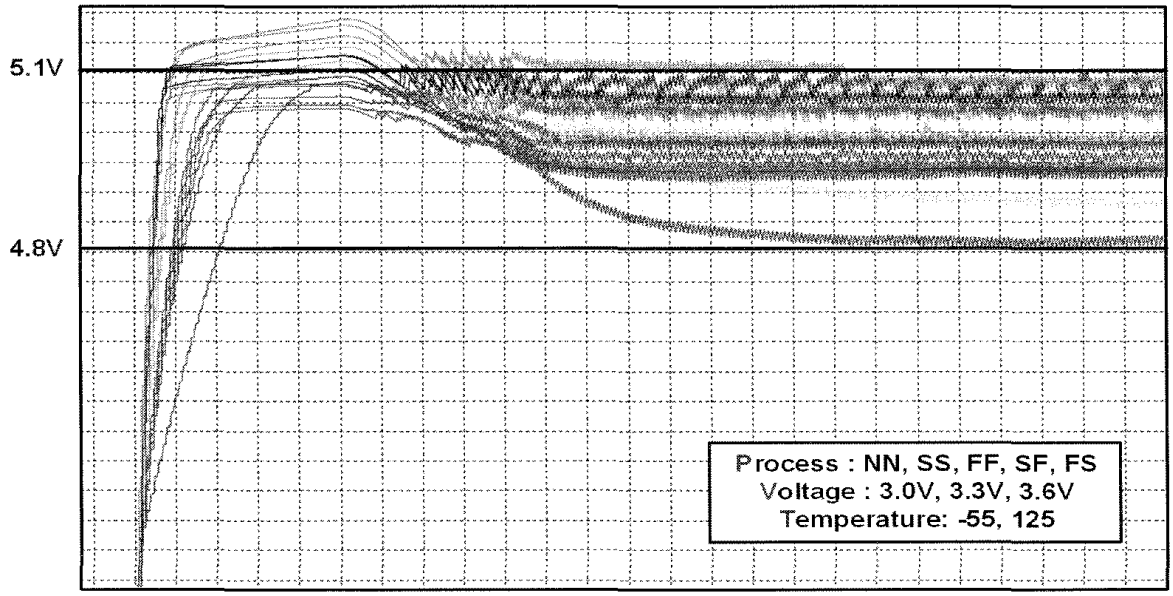


Fig. 4.2.1. Simulation results with 30mA output current in PVT variation

4.3. Chip Layout and Fabrication

The proposed charge pump is implemented using 3.3V 0.13um I/O CMOS process. Core size is 500um x 500um. To supply sufficient output current, transistor size at output stage should be large enough. Fig. 4.3.1. shows the layout structure of regulated charge pump with high precision which generate stable output voltage.

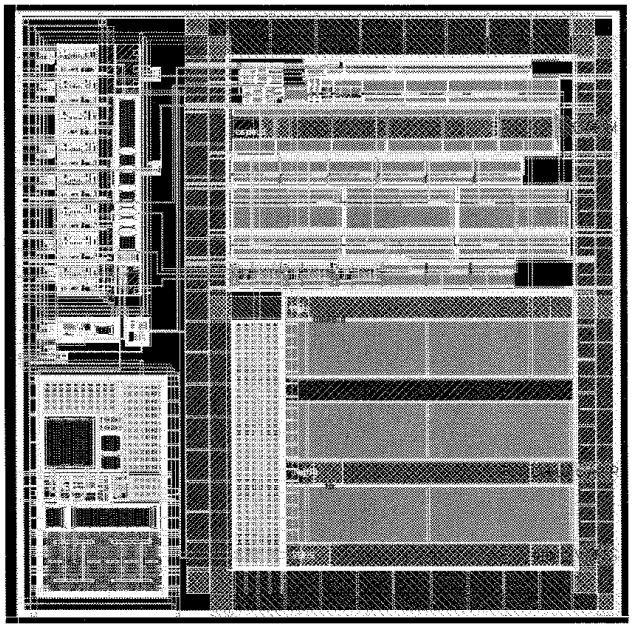


Fig. 4.3.1. Layout structure of proposed charge pump

CHAPTER 5

MEASUREMENT RESULTS

5.1 Chip Micrograph

Fig 5.1.1. shows the microphotograph of front-end in USB-OTG. Charge pump, voltage reference, comparators, ID detector and level shifter is fully implemented in 3.3V 0.13um I/O CMOS technology. Pumping capacitor of charge pump is externally attached.

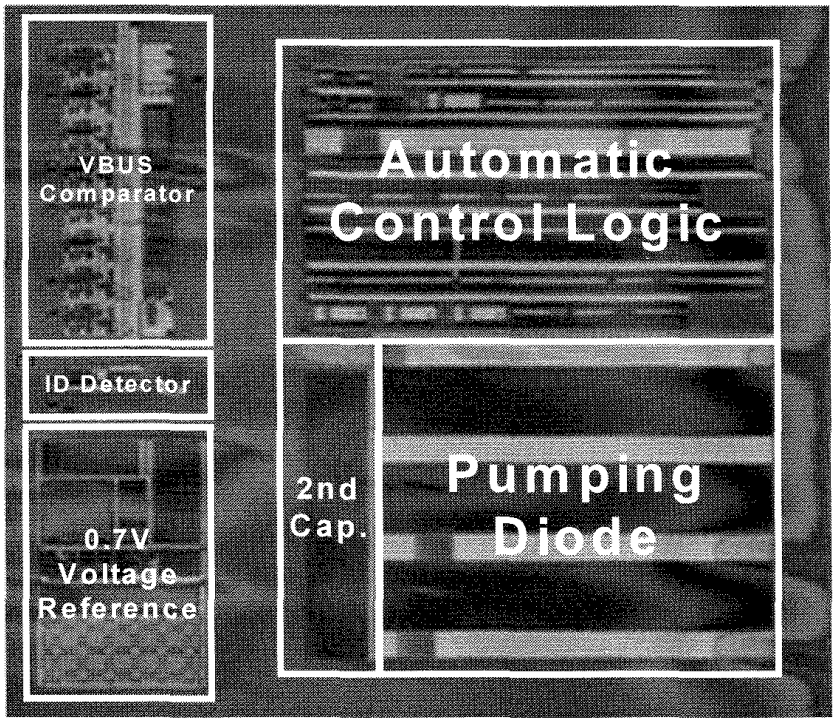


Fig 5.1.1. Microphotograph of proposed charge pump

5.2 PCB Design

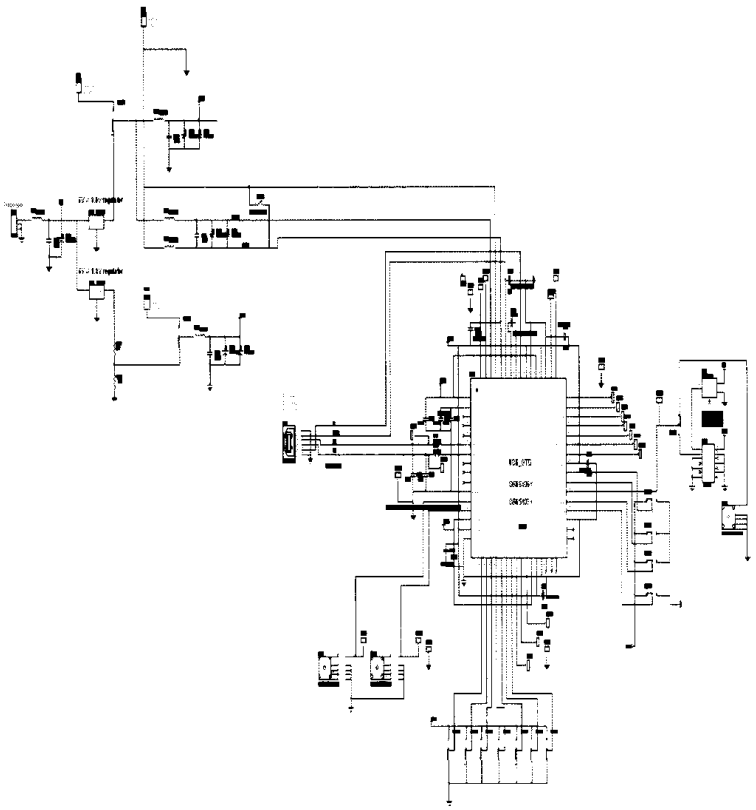


Fig 5.2.1. PCB board Schematic

Fig 5.2.1. shows schematic of PCB board for charge pump. Power is provided by either external regulators or power supply. Input clock signal is given by 500KHz crystal oscillator and can be given by external function generator. And output current can be measured by variable load resistor. By varying the value of load resistor, output current can be calculated from output voltage.

5.3 Measurement Set-up

Fig 5.3.1. shows PCB board of charge pump for measurement. Operational mode can be selected by mode switches and can be debugged by debugging pins. Output of charge pump is connected to load resistor through USB-cable. The magnitude of load resistor can be selected by switches.

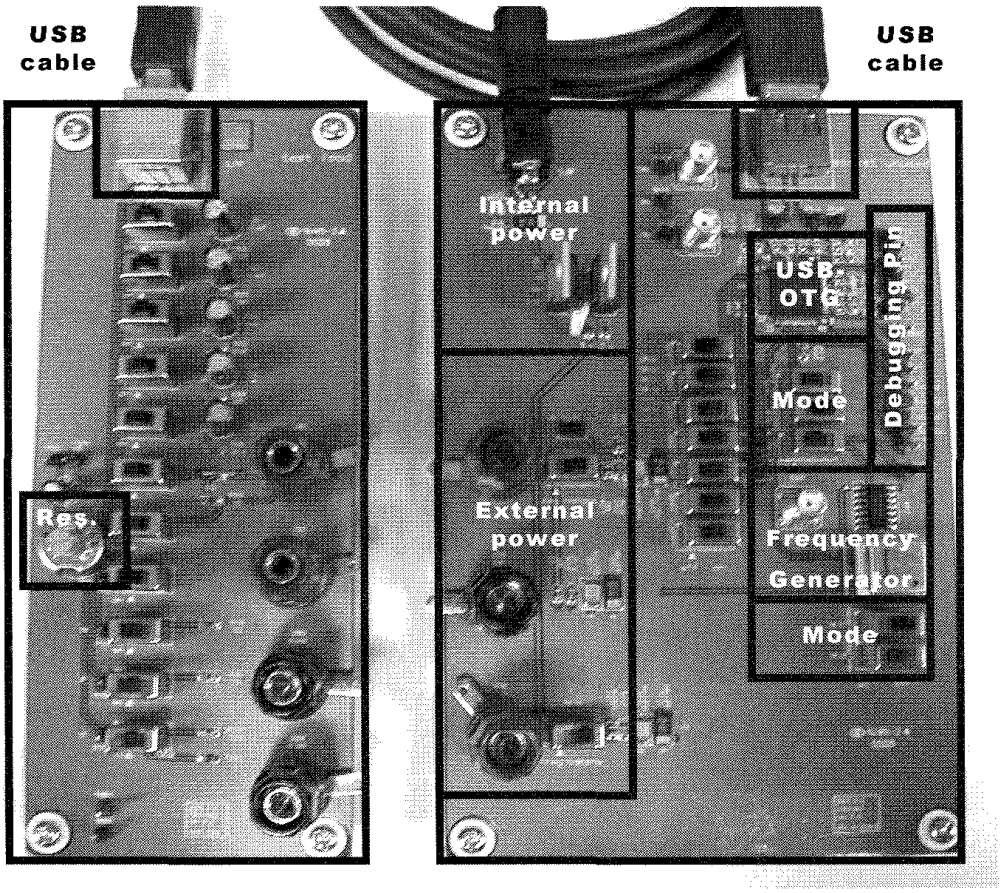
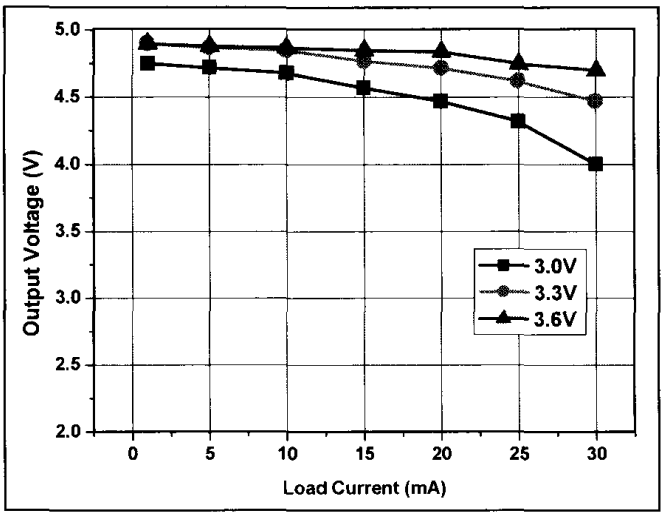
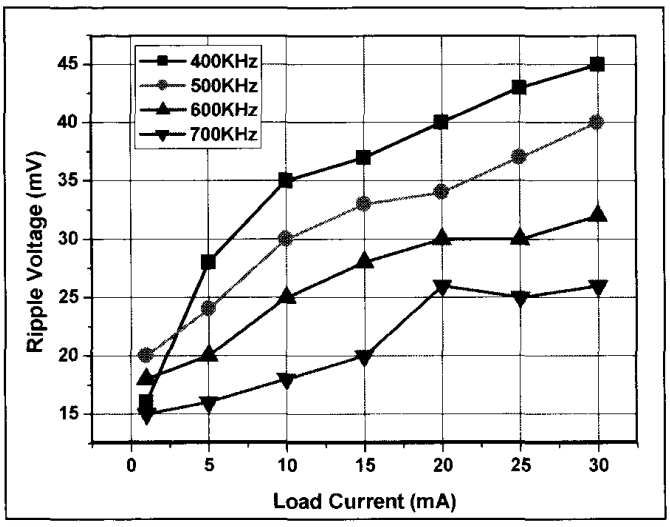


Fig 5.3.1. PCB board Set-up

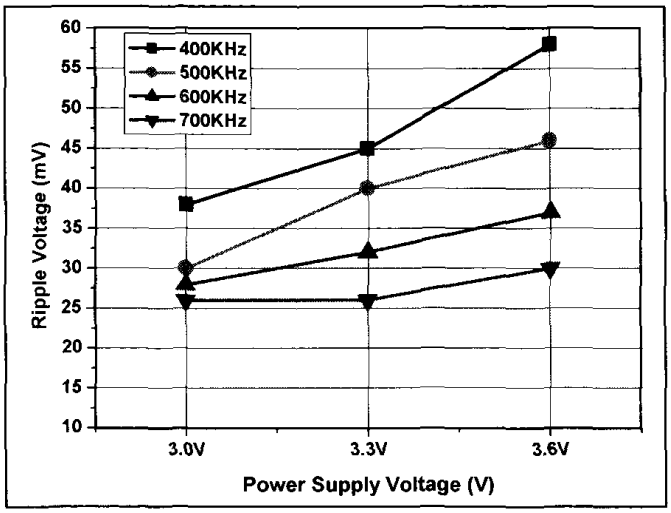
5.4 Measurement Results



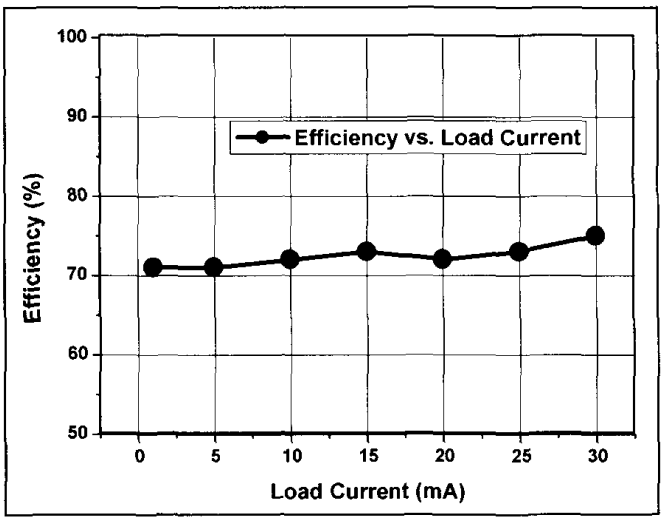
Measurement Result 1. Output Voltage vs. Load Current



Measurement Result 2. Ripple Voltage vs. Load Current



Measurement Result 3. Ripple Voltage vs. Supply Voltage



Measurement Result 4. Efficiency vs. Load Current

CHAPTER 6

CONCLUSION

6.1 Summary of the performance

5V 30mA regulated charge pump with high precision is designed and implemented using 3.3V 0.13-um I/O CMOS technology. The core size is 500um x 500um. Table 6.1.1 lists main features of proposed charge pump. Fig. 7.1.1 and Fig. 7.1.2. shows the waveform of output voltage and output ripple voltage with 30mA output current.

Performance Factors	Performance
Supply Voltage	3.3V
Output Voltage	4.5V ~ 4.9V
Output Current	< 30mA
Output Ripple Voltage	< 40mV
Efficiency	> 70%
Disable Mode	< 0.1V
External Cap. (Pumping Cap.)	330nF
Core Size	500um x 500um
Technology	3.3V 0.13um CMOS technology

Table 6.1.1. Performance summary

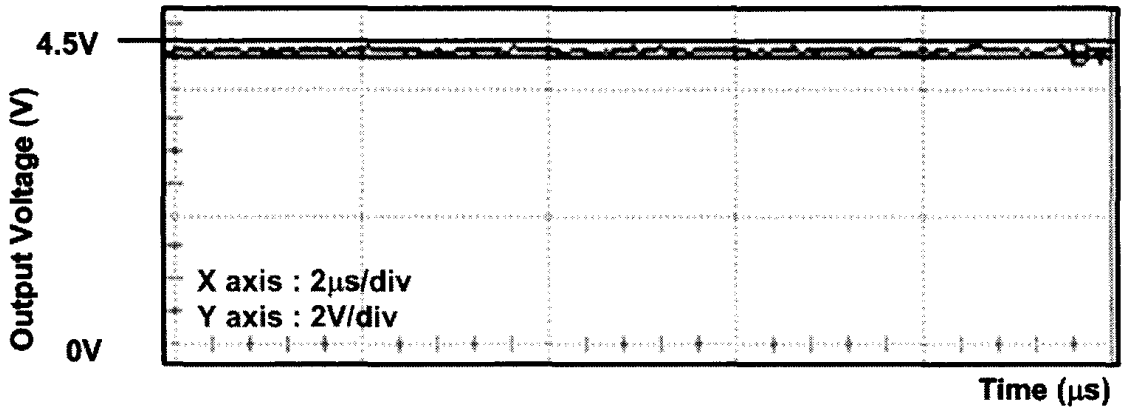


Fig 6.1.1. Output voltage with 30mA output current

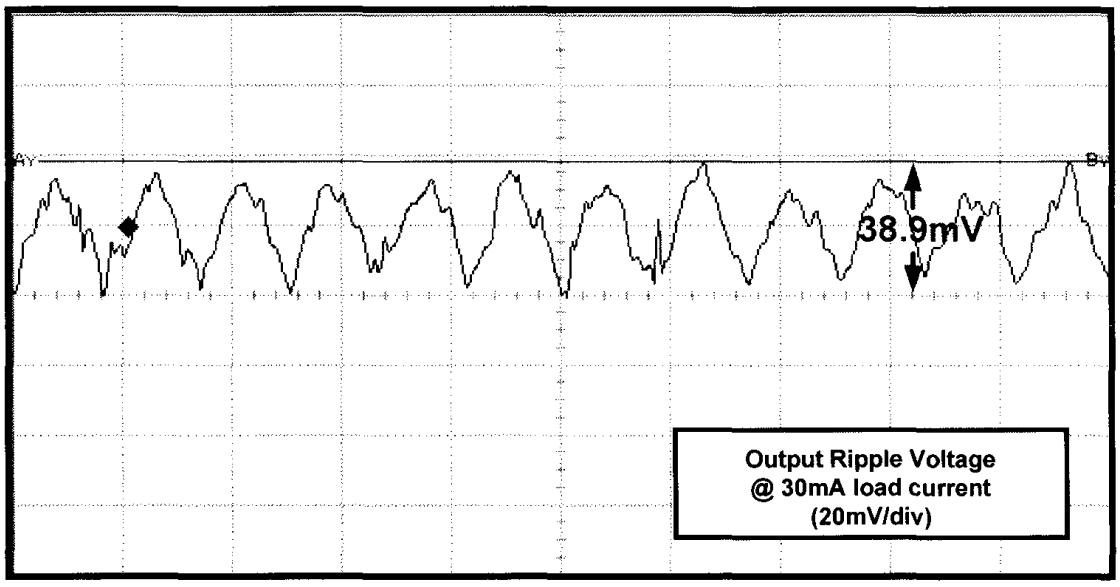


Fig 6.1.2. Ripple voltage with 30mA output current

Based on the measurement result, normalized ripple performance index can be obtained. Normalized ripple performance index is given by

$$\text{Normalized Performance Index} = \frac{\text{Current}_{Load}(mA)}{\text{Voltage}_{Ripple}(mV)\times \text{Cap.}_{Load}(uF)\times \text{Freq}_{Clk}(KHz)}$$

Ripple voltage is proportional to output current (Current_{LOAD})

Ripple voltage is inverse proportional to load capacitor (Cap._{LOAD})

Ripple voltage is inverse proportional to clock frequency (Freq_{Clk})

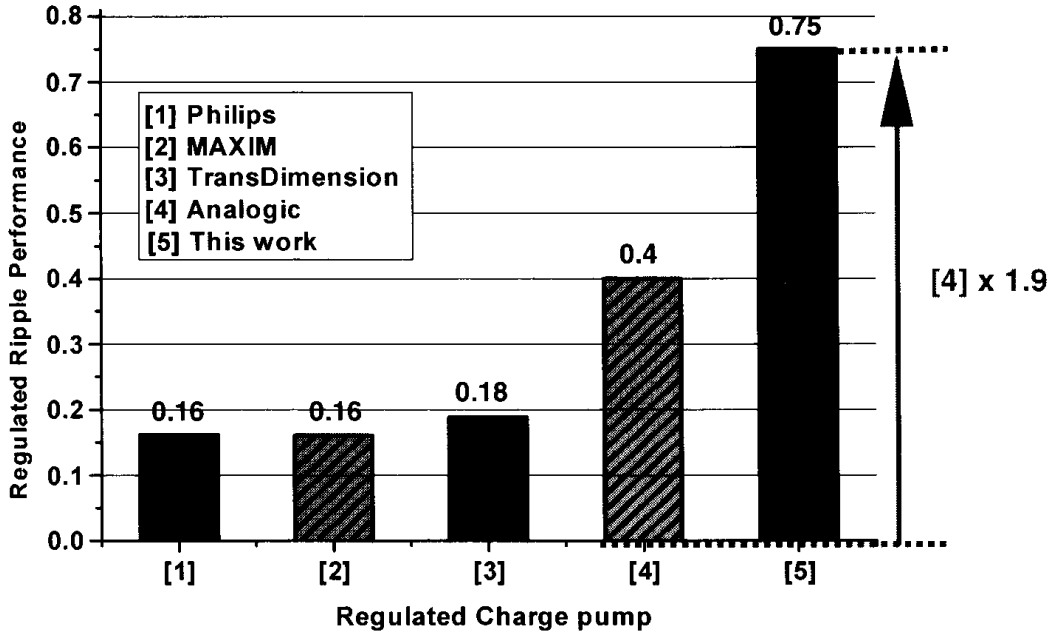


Fig 6.1.3. Performance Comparison

6.2 Conclusion

As USB-OTG scheme is introduced, it has led to the necessity of charge pump. With that flow, most of electrical devices should have their own power supply to exchange data by USB-OTG. To satisfy the requirements of USB-OTG, charge pump should have stable output voltage.

Even though there have been many research efforts to generate stable output voltage, it was hard to do it. This work is focuses on the design and implmentation of regulated charge pump with stable output for USB-OTG application with the analysis of conventional charge pump. The proposed charge pump is implemented with 3.3V 0.13um I/O CMOS technology with 330nF external pumping capacitor.

To make stable output voltage, the regulated charge pump detects the variation of output boosted voltage which is higher than power supply voltage. As the variation of detected output voltage, 6-bit control signal is obtained and controls the 'Automatic Driving Buffer' which is composed of four parallel buffers. The 'Automatic Driving Buffer' operates selectively by 'Driving Buffer Size Control Unit' and controls pumping current with 6-bit control signals. Therefore, by controlling of charge current as the variation of boosted output voltage, the regulated charge pump generates stable boosted output voltage.

At measurement, the regulated charge pump generates 5V constant output voltage which is independent of load current and to lower output ripple voltage up to 40mV with 2uF load capacitor with supplying 30mA output current. All performance results meet the specification of USB-OTG.

CHAPTER 7

FURTHER WORK

To enhance the performance of regulated charge pump, such as stable output voltage and small ripple voltage, frequency scaling scheme can be used. Fig. 7.1. shows the overall block diagram of charge pump for frequency scaling and Fig. 7.2 shows block diagram of variable frequency generator for small output ripple.

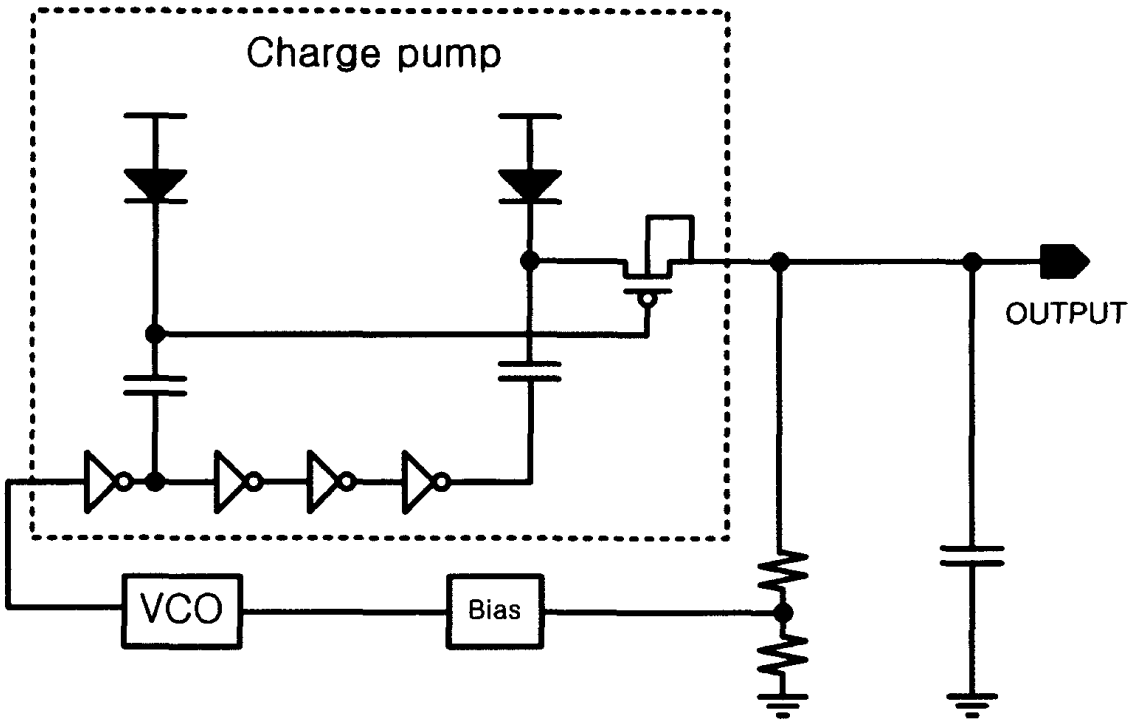


Fig. 7.1 Block diagram of charge pump for frequency scaling

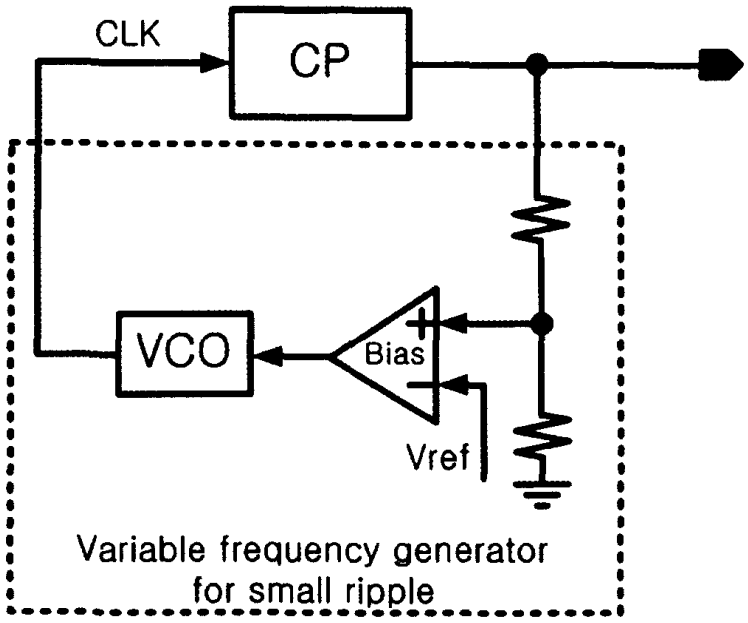


Fig. 7.2 Variable frequency generator for small output ripple

In Fig. 7.1. charge pump block generates high output voltage and bias block generates input signal of VCO (Voltage Controlled Oscillator) based on output voltage of charge pump. VCO generates clock signal which has frequency proportional to VCO input signal. As the input signal voltage of VCO rises, VCO generates output clock signal with higher frequency, and as the input signal voltage of VCO falls, VCO generates output clock signal with lower frequency. According to the input voltage, output clock frequency varies.

As shown in Fig. 7.2, output voltage of charge pump is divided by

two resistors and divided voltage is used as input of bias block. Output signal of Bias controls the output clock frequency of VCO. By using this scheme, when output voltage of charge pump is low, VCO generates low output clock frequency. Then pumping frequency of charge pump becomes low. And input clock frequency of charge pump goes high proportional to the output voltage of charge pump. Then pumping frequency of charge pump becomes high. Because the magnitude of output ripple voltage is inverse proportional to the input clock frequency of charge pump, high input clock frequency makes the magnitude of output ripple voltage low.

SUMMARY

전자 제품들 간의 data 교환시 더욱 유용한 기술인 USB-OTG통신을 위해서 전자 제품들은 power를 공급할 수 있는 power supply 능력을 갖추어야 한다. USB-OTG 통신 규격에 맞는 power를 공급하기 위해서는 전자제품에서 일반적으로 사용하는 전압에 비하여 높은 전압을 생성하여야하며 이를 위해서는 Charge pump회로가 가장 적합한 power supply공급 장치이다.

본 논문에서는 출력 전류에 무관하게 최소의 흔들림을 가지며 일정한 전압을 생성해내는 Charge pump회로를 설계 및 구현을 하였다. 'Automatic Driving Buffer' 기술을 이용하여 기존의 출력 전압의 흔들림 현상을 최소화하였으며 환경 변화로 인한 출력단의 전압 변화가 최소화 되도록 설계를 하였다. 3.3V 입력 전압으로부터 5V 출력 전압을 생성해내며 출력 전류는 30mA까지 공급할 수 있다. 출력 전압은 2uF의 load capacitor를 달았을 때 최대 40mV의 흔들림 현상을 가진다.

본 논문에서 제시한 'Automatic Driving Buffer' 기술은 출력측 전압이 최대한 일정한 값을 가질 수 있도록 도와주며 안전한 power공급을 요구하는 시스템에 적합하다.

REFERENCES

[1] John F.Dickson, "On chip high voltage generation in MNOS integrated circuit using improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, No 3., June. 1976.

[2] Jieh Tsorng Wu, "1.2V CMOS switched capacitor circuits," in *IEEE Dig. Tech. Papers of ISSCC*, Feb. 1996, paper sp. 24.4.

[3] Jose silva-Martinez national institute for research in astrophysics,, "Charge pump for optimal dynamic filter" *IEEE J. Solid-State Circuits*, Vol. 36, pp. 1498-1505, Dec. 1995.

[4] William L.martino, JR. Jerry D.moench, Alan R.borman, and Rodney C. Tesch, "An on chip back bias generator for MOS Dynamic memory," *IEEE J. Solid-State Circuits*, No 5., Oct. 1980.

[5] Dragan Maksimovic and Sandeep Dhar Colorado Power Center, "Switched capacitor DC-DC converters for low power on-chip applications,"Power Electronics 1999.

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2년이라는 대학원 생활을 마치면서, 그 동안 부족한 점이 많은 저로 하여금 이 논문을 완성할 수 있도록 도와주신 분들께 감사의 말을 전합니다.

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Publication

1.Sung-Eun Kim, Seong-Jun Song, Sung-Min Park and Hoi-Jun Yoo "CMOS Optical Receiver Chipset for Gigabit Ehternet Application" Circuits and Systems, 2003., ISCAS '03, 2003 IEEE International Symposium

2. Ramchan Woo, Sungdae Choi, Ju-Ho Sohn, Seong-Jun Song, Young-Don Bae, Chi-Weon Yoon, Byeong-GyuNam, Jeong-Ho Woo, Sung-EunKim, In-Cheol Park,

Sungwon Shin, Kyung-Dong Yoo, Jin-Yong Chung and Hoi-JunYoo "A 210mW Graphics LSI Implementing Full 3D Pipeline with 264Mtexels/s Texturing forMobile Multimedia Applications" in IEEE Int. Solid-State Circuits Conf.(ISSCC), Feb. 2003

3. Se-Joong Lee, Seong-Jun Song, Kangmin Lee, Jeong-HoWoo, **Sung-Eun Kim**, Byeong-Gyu Nam and Hoi-Jun Yoo "An 800MHz Star-Connected On-Chip Network for Application to Systems on a Chip" in IEEE Int. Solid-State Circuits Conf.(ISSCC), Feb. 2003

4. Kangmin Lee, Se-Joong Lee, **Sung-Eun Kim**, Hye-Mi Choi, Donghyun Kim, Sunyoung Kim, Min-Wuk Lee and Hoi-Jun Yoo "A 51mW 1.6GHz On-Chip Network for Low-Power Heterogeneous SoC Platform"in IEEE Int. Solid-State Circuits Conf.(ISSCC), Feb. 2003

Patent

1.*Sung-Eun Kim, and Hoi-Jun Yoo* "Control-Method and Apparatus for small output ripple of Charge pump circuit" Korea, US, Japan, Nether-land (Pending)

Current Interest

1. High Speed Full Analog Interface
2. Optical Interface
3. OLED Driver
4. Power Supply Design