Design and Implementation of High-Speed CMOS Clock and Data Recovery Circuit for Optical Interconnection Applications

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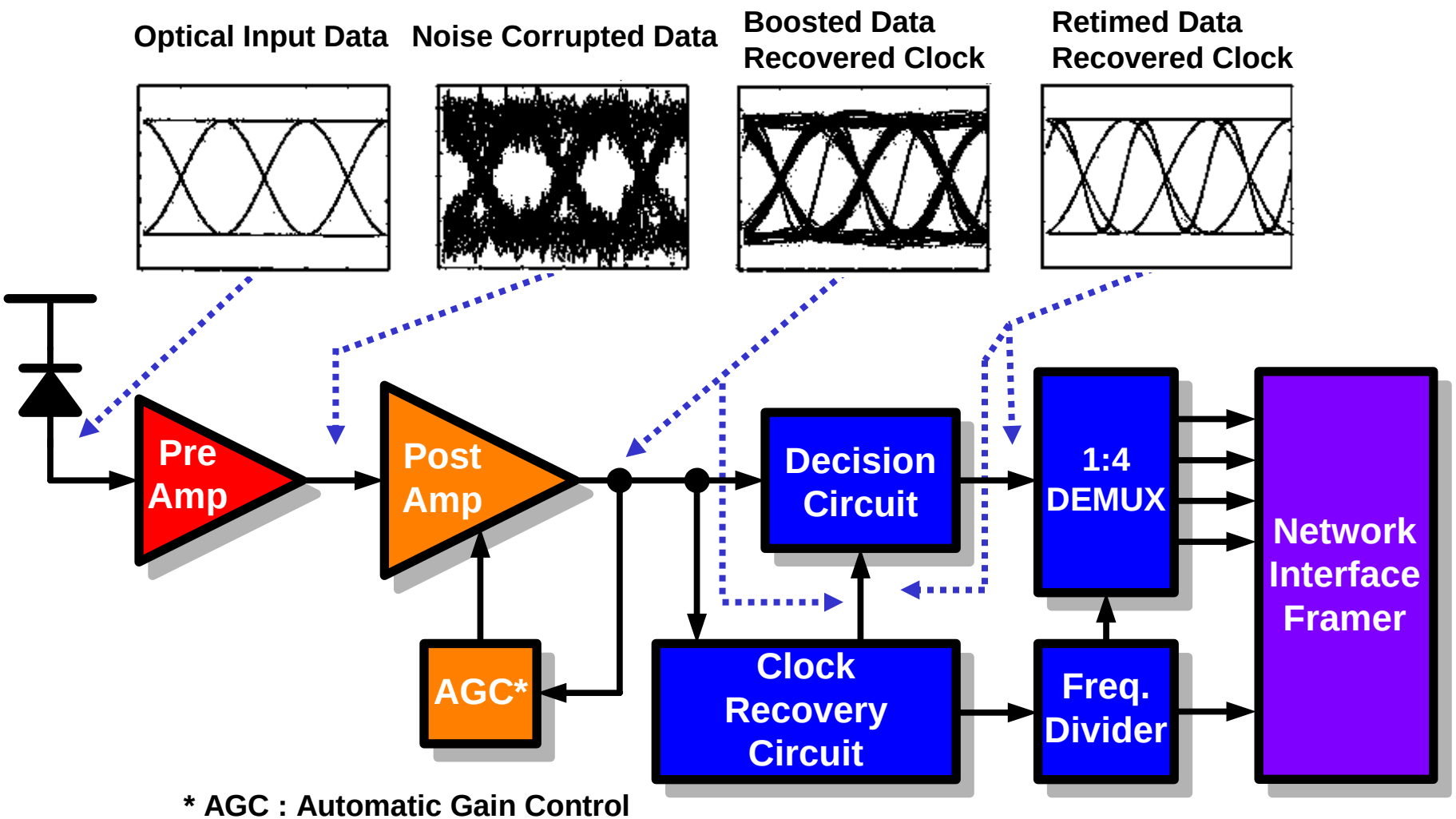
Outline

- Introduction
- Motivation
- Problem Definition
- Proposed 1/8-Rate CDR
- Building Blocks
- Measurement Results
- Conclusion & Further Works

Introduction



* AGC : Automatic Gain Control

Motivation

Long-Haul Applications (SONET, Gigabit Ethernet)

III-V, Si Bipolar, SiGe HBT

- ☺ Very high-speed
- ☺ Inherently low noise
- ☹ High cost
- ☹ High power consumption
- ☹ Not compatible with other technologies

Short-Haul Applications (Backplane, Chip-to-Chip)

CMOS

- ☺ Low cost
- ☺ High level of integration
- ☺ Low power consumption
- ☹ Less speed
- ☹ High noise

The Solution is
Novel CDR Architecture and Circuit Techniques In CMOS !!!

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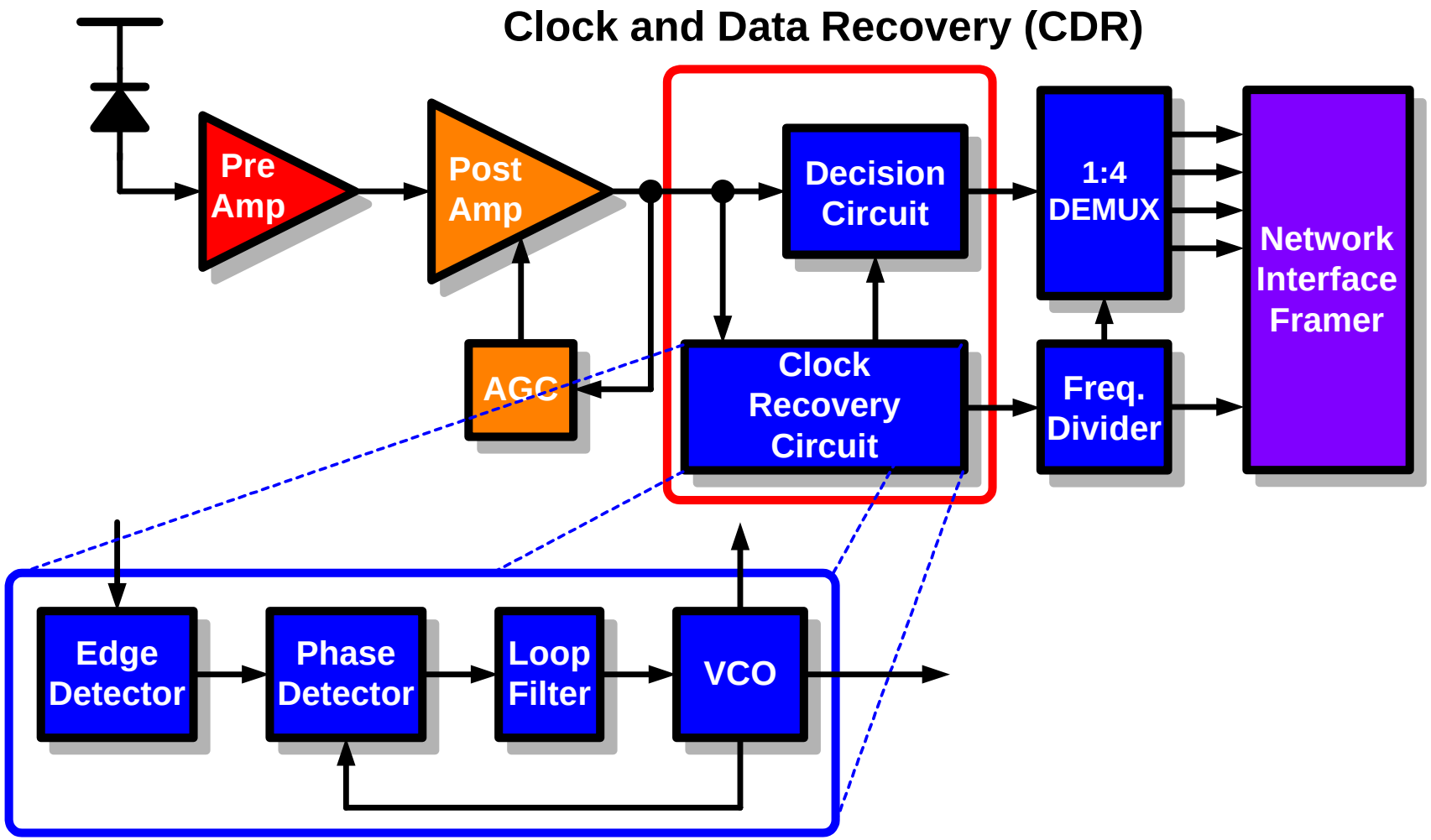
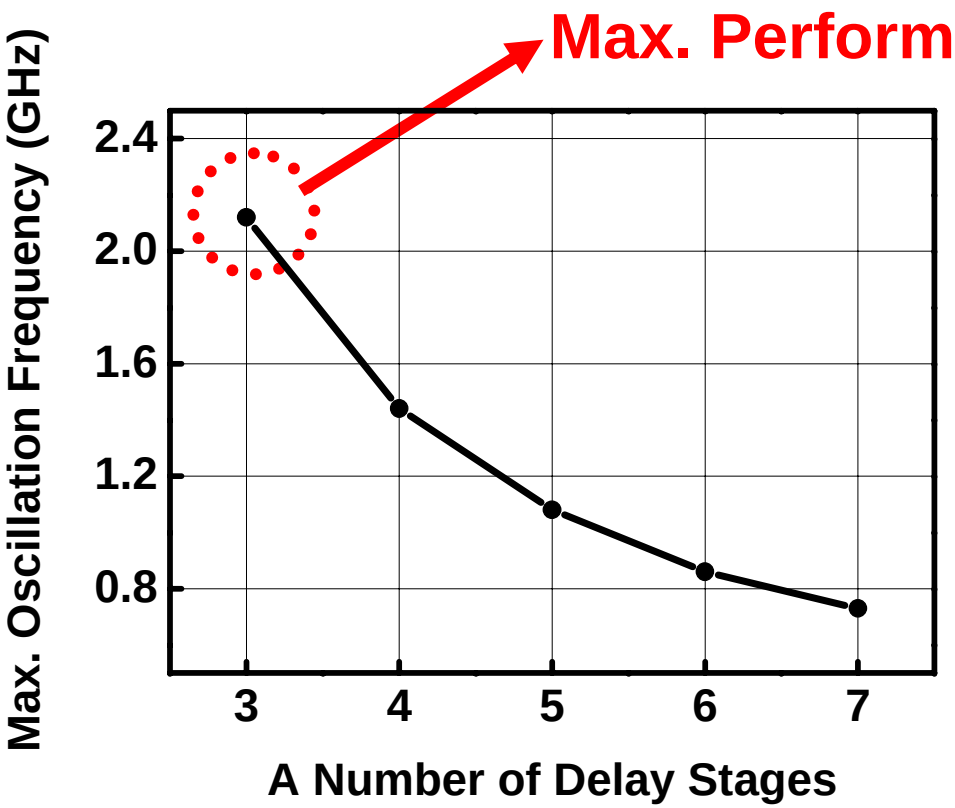
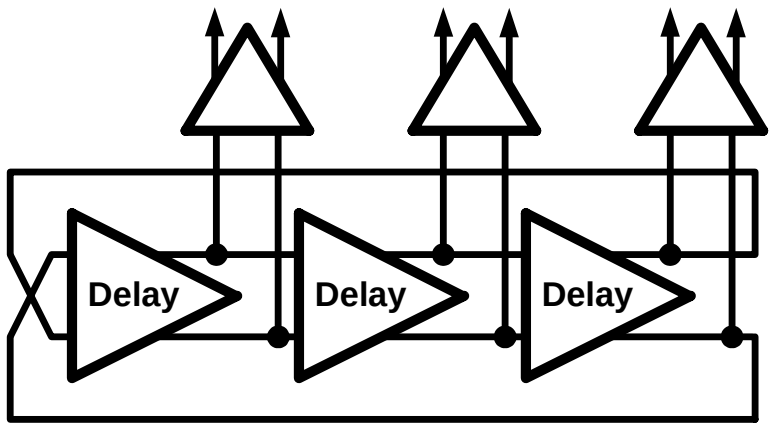
Generic CDR Configuration



Performance Limitation of 0.25-μm CMOS *



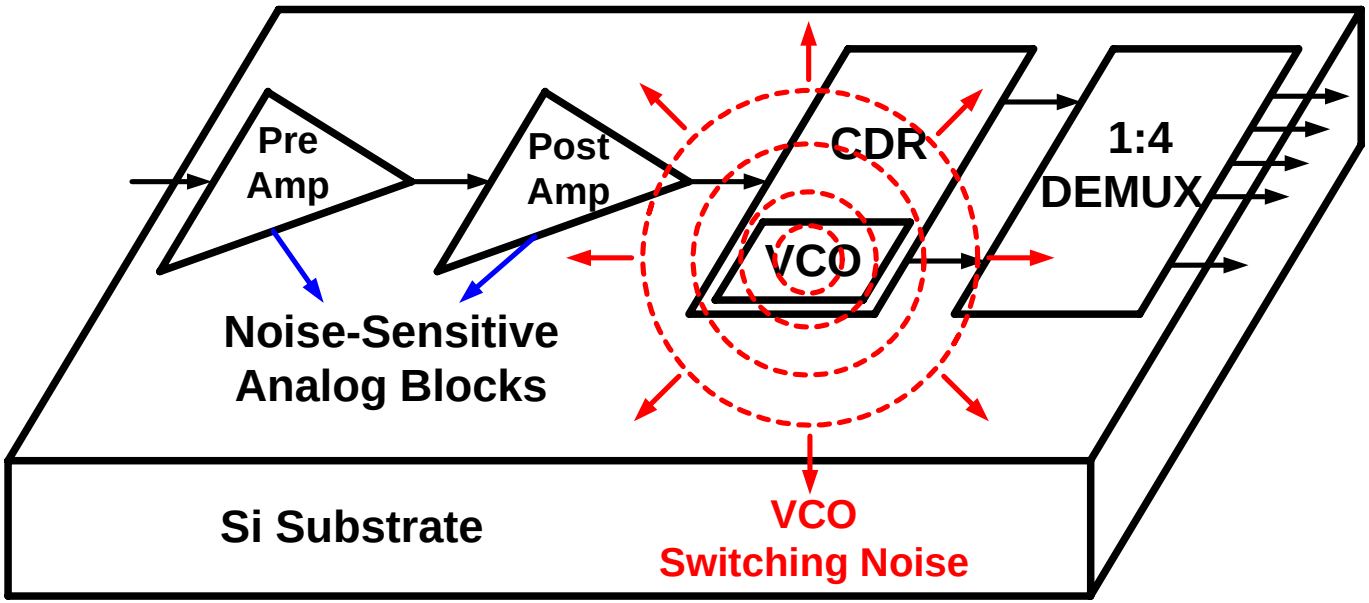


Simple VCO

* M. Fukaishi, et al., JSSC, Dec. 1998

- Simulation result for 0.25-μm CMOS differential ring oscillators with resistive loads and isolation buffers

Substrate Noise Effect of VCO

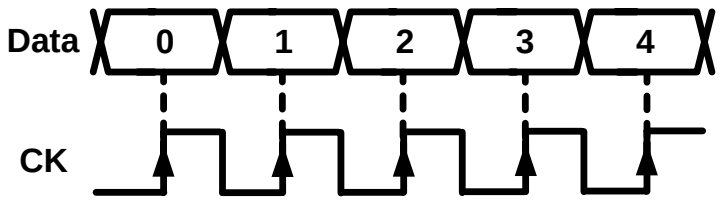


Substrate noise voltage $\propto \sqrt{f}$ *

* M. van Heijningen, et al., JSSC, Aug. 2002

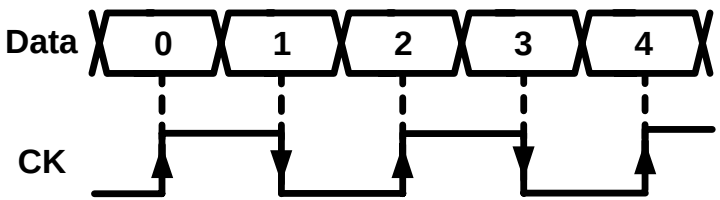
Conventional CDR Techniques (1/2)

- **Full-Rate Clock Technique ***
  - ☹ Full-rate clock frequency (4GHz)
  - ☹ Impossible to design VCO



* M. Soyuer, et al., JSSC, Dec. 1993

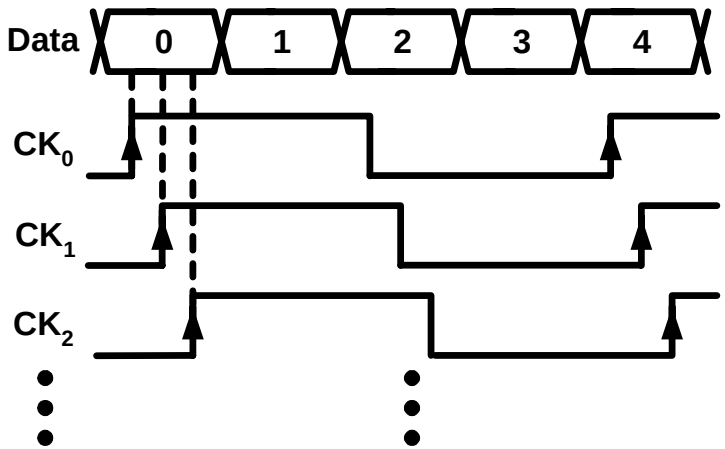
- **Half-Rate Clock Technique ****
  - ☹ Half-rate clock frequency (2GHz)
  - ☹ Close to performance limitation
  - ☹ Difficult to design VCO



** M. Rau, et al., JSSC, July 1997

Conventional CDR Techniques (2/2)

- **Oversampling Technique ***
  - ☺ Quarter-rate clock frequency (1GHz)
  - ☺ Easier to design VCO
  - ☹ Highly clock phase resolution
  - ☹ Quantization jitter
  - ☹ Extra decision logic



* C.-K. Yang, et al., JSSC, May 1998

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- **Proposed 1/8-Rate CDR**
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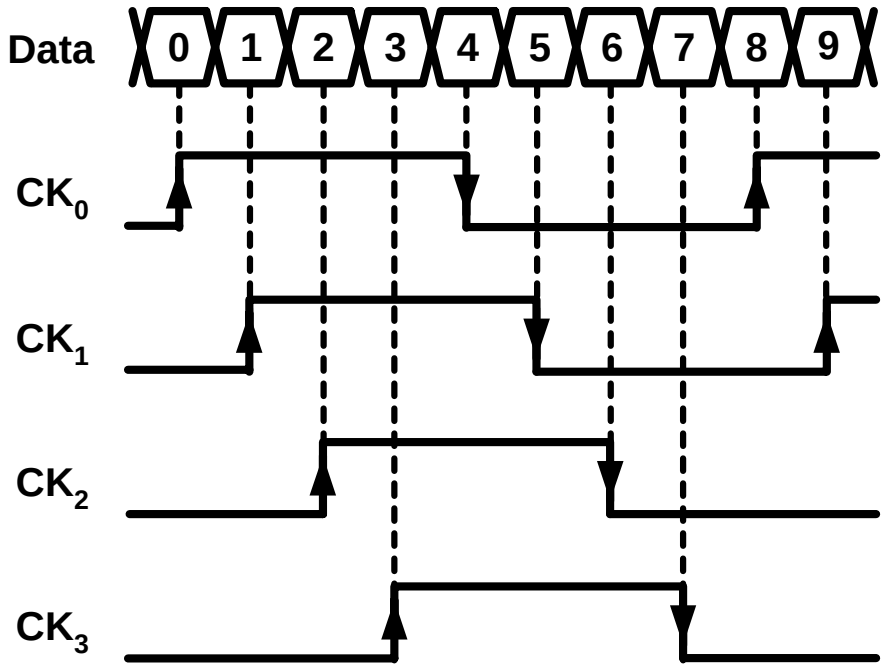
Proposed CDR Technique

- 1/8-Rate Clock Technique *
  - ☺ 1/8-rate clock frequency (0.5GHz)
  - ☺ Very easy to design VCO
  - ☺ No quantization jitter
  - ☺ No extra decision logic
  - ☺ Can do 1:4 DEMUX
  - ☹ Complex design

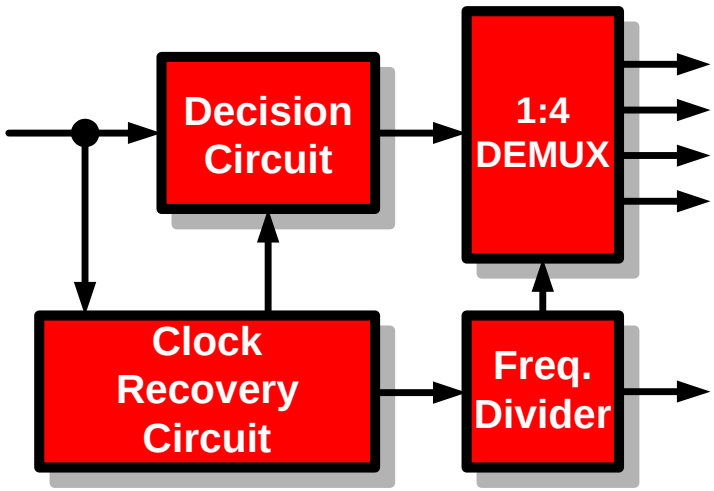


* S.-J. Song, et al., ESSCIRC, Sept. 2002

* S.-J. Song, et al., to be published for JSSC, July 2003

Proposed 1/8-Rate CDR Architecture

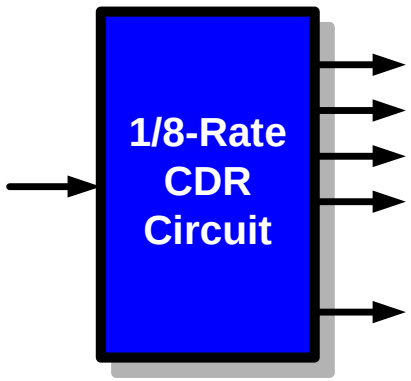
Conventional Full-Rate CDR



Multiple Funtional Blocks

Merging

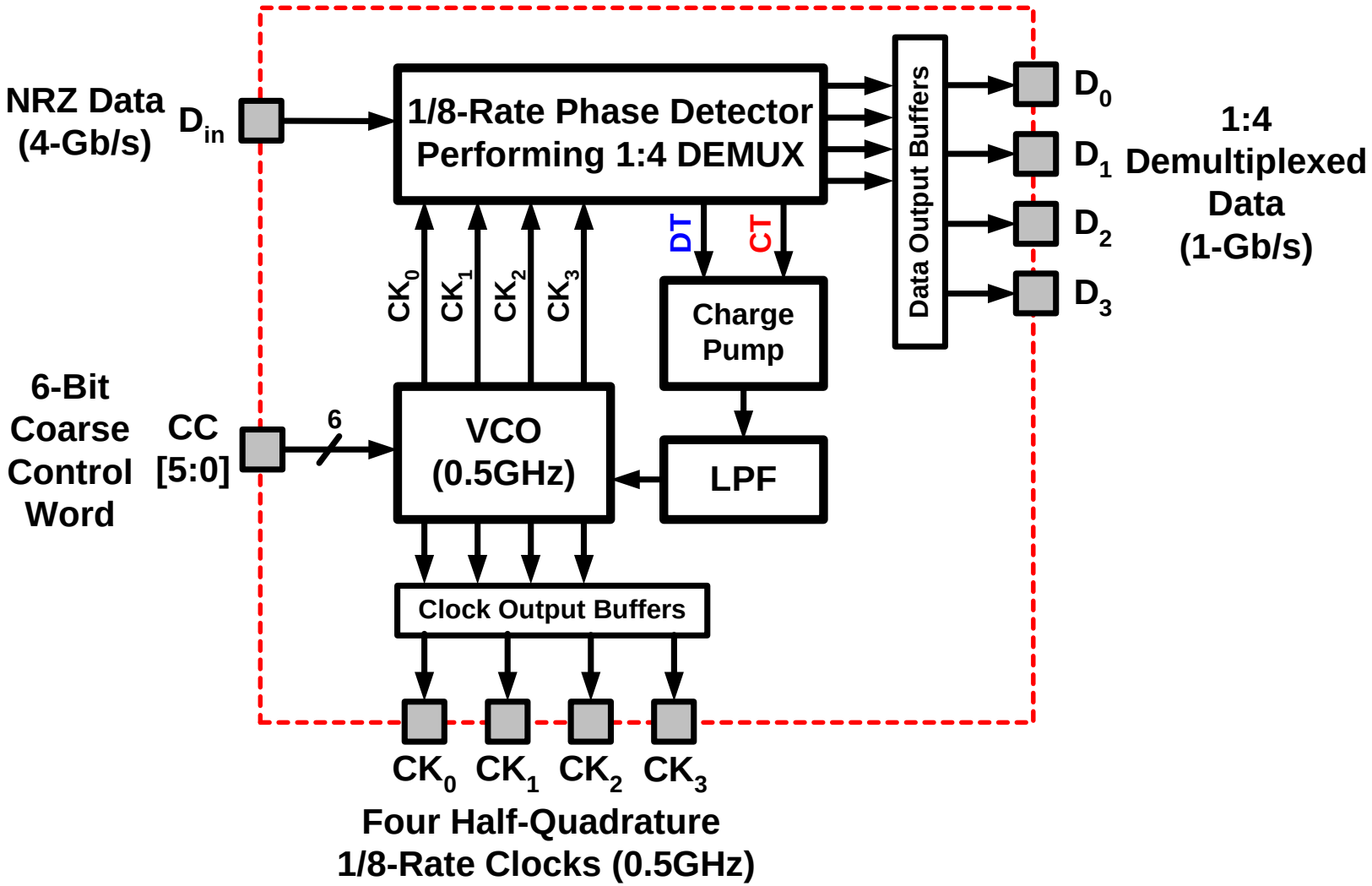
Proposed 1/8-Rate CDR



A Single Functional Block

- **Proposed 1/8-rate CDR circuit can achieve higher speed operation, lower power consumption, and smaller area.**

Proposed 1/8-Rate CDR Circuit



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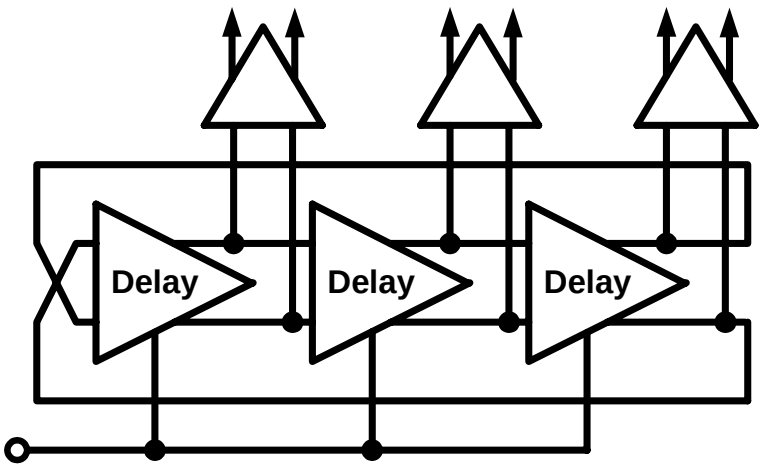
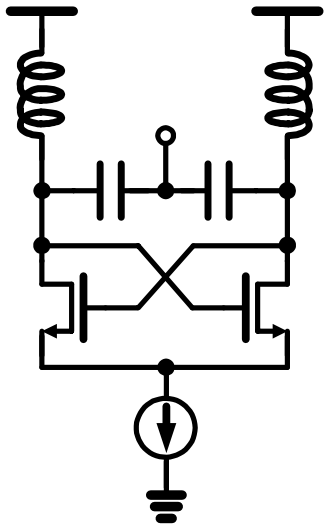
Choice of VCO Configuration

✓ Ring Oscillator



- ☺ Wide tuning range
- ☺ Different phase clock generation
- ☹ Low center frequency
- ☹ Low Q factor
- ☹ High phase noise & jitter

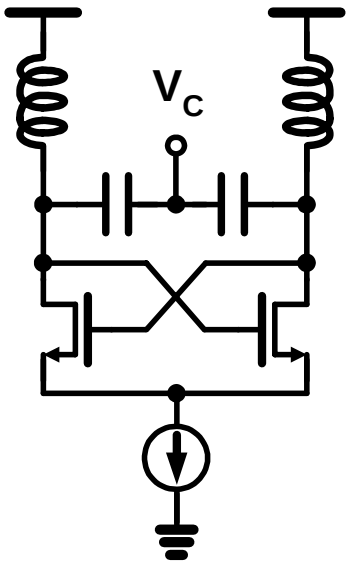
LC Oscillator



- ☺ High center frequency
- ☺ High Q factor
- ☺ Low phase noise & jitter
- ☹ Narrow tuning range
- ☹ Large area

Choice of Inductor Load

Spiral Inductor Load

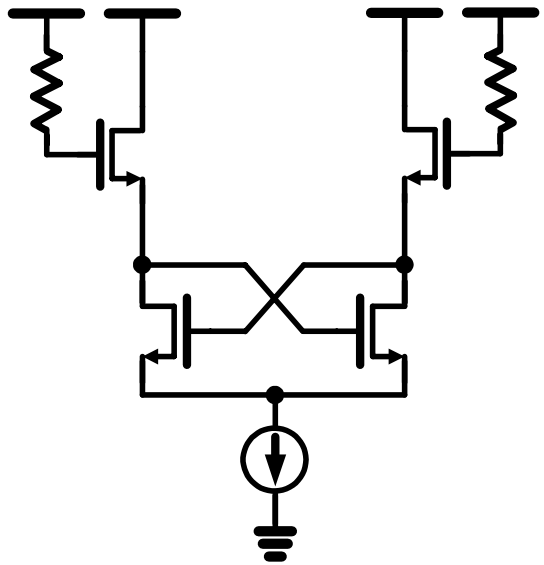


$$C \propto V_C$$

$$\omega_{osc} \propto \frac{1}{\sqrt{LC}} \propto \frac{1}{\sqrt{V_C}}$$

- ☹ Low Q factor (3~5)
- ☹ Large area
- ☹ Dependent on process
- ☹ Difficult to design

✓ Active Inductor Load

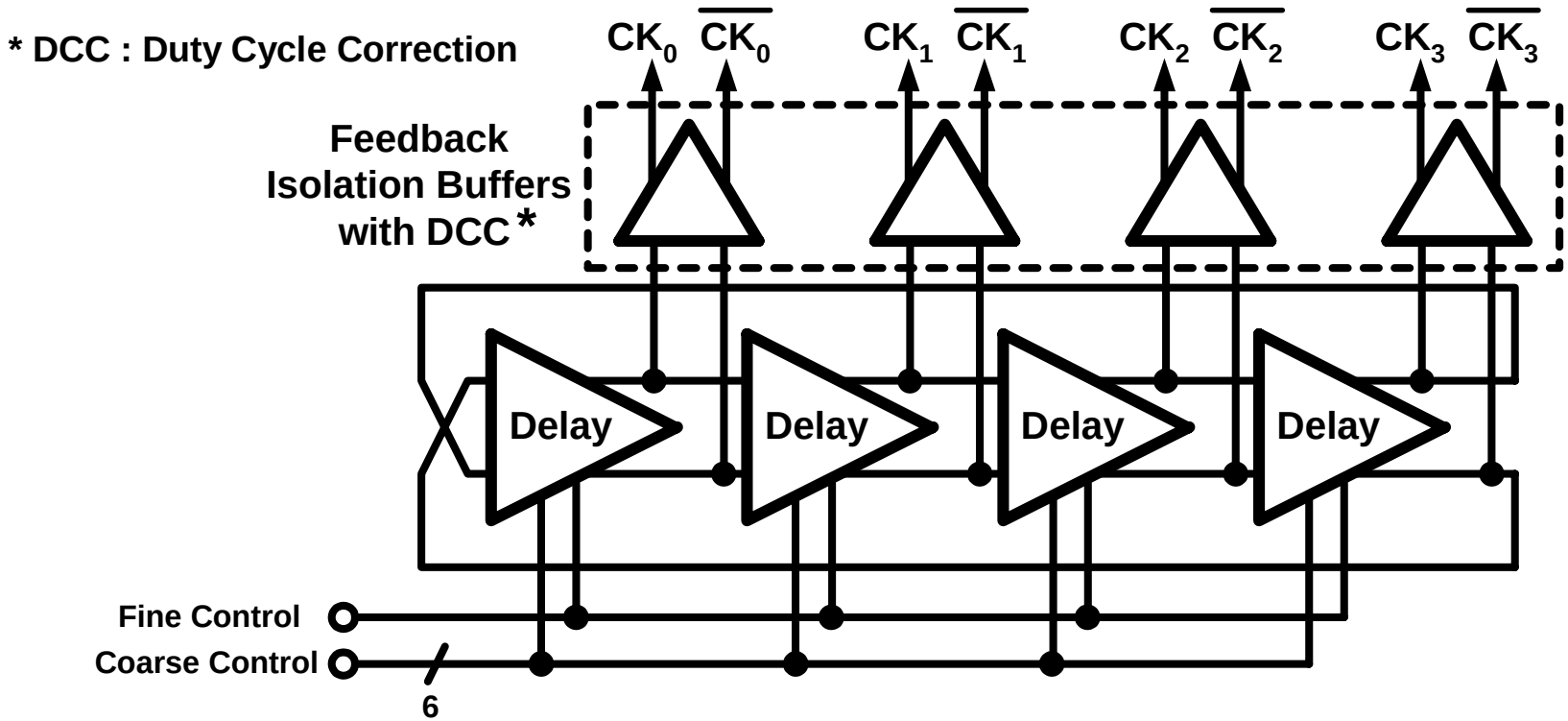


$$L \propto \frac{1}{g_m}$$

$$\omega_{osc} \propto \frac{1}{\sqrt{LC}} \propto \sqrt{g_m} \propto \sqrt{\sqrt{I_D}}$$

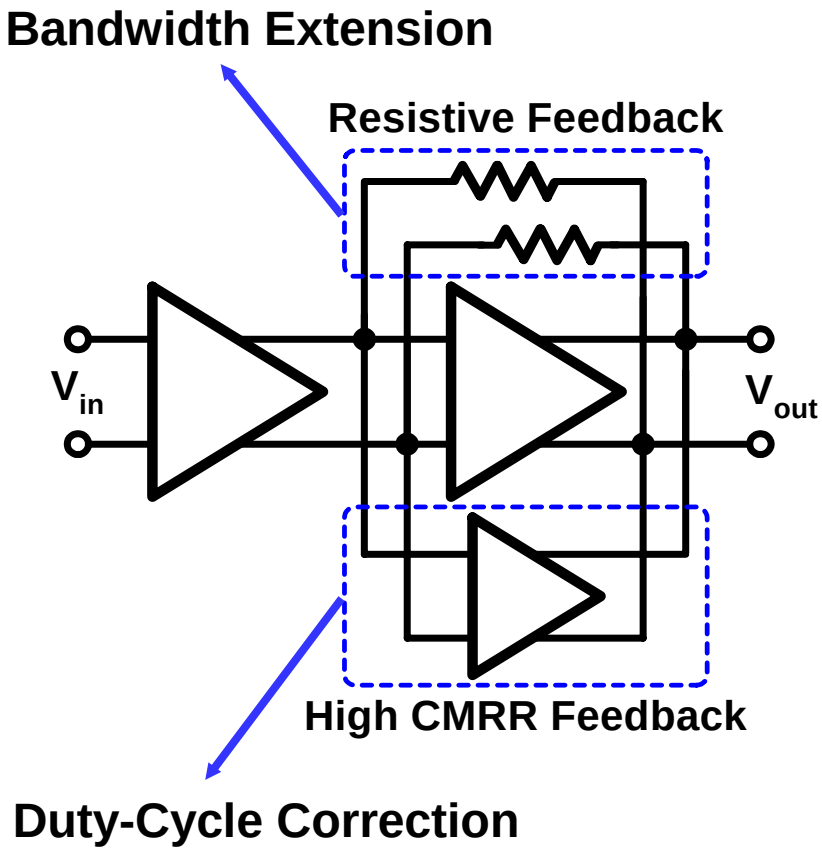
- ☺ Moderately high Q factor (>>10)
- ☺ Small area
- ☺ Easy to design
- ☹ Noise caused by resistor and MOS

Voltage-Controlled Oscillator

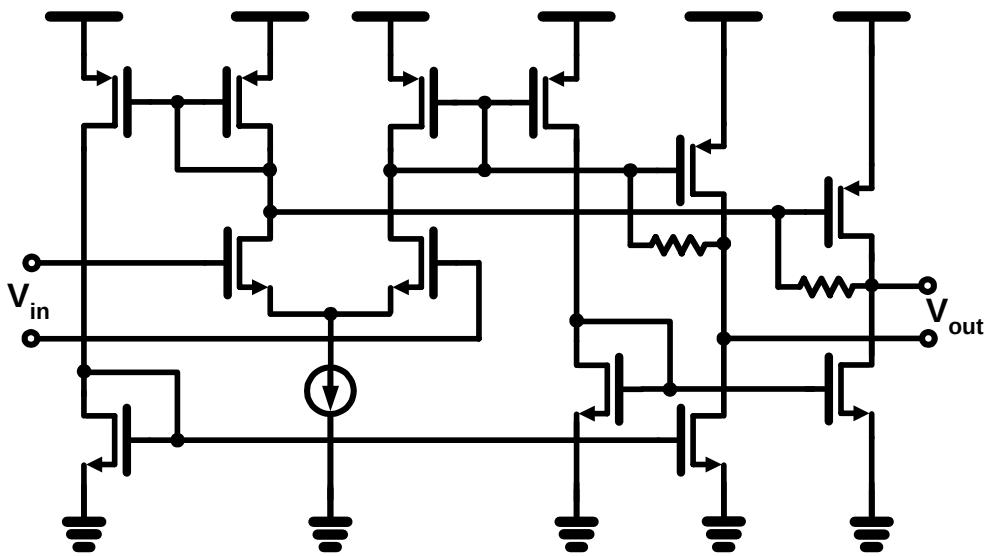


- Four half-quadrature phase clocks
- Delay stage with active inductor load
- DCC for using both rising and falling edges of clock

Feedback Isolation Buffer

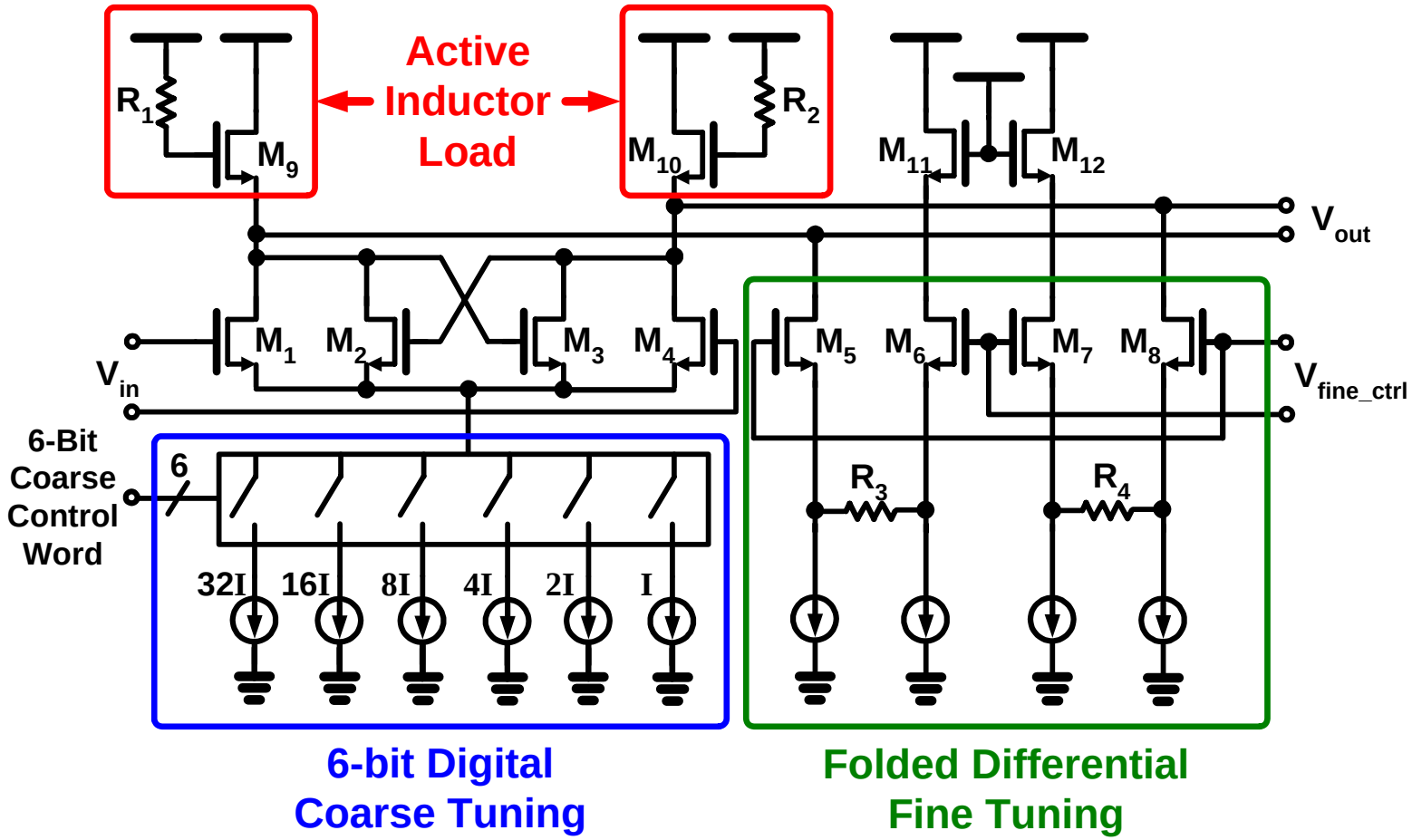


(a) Block Diagram



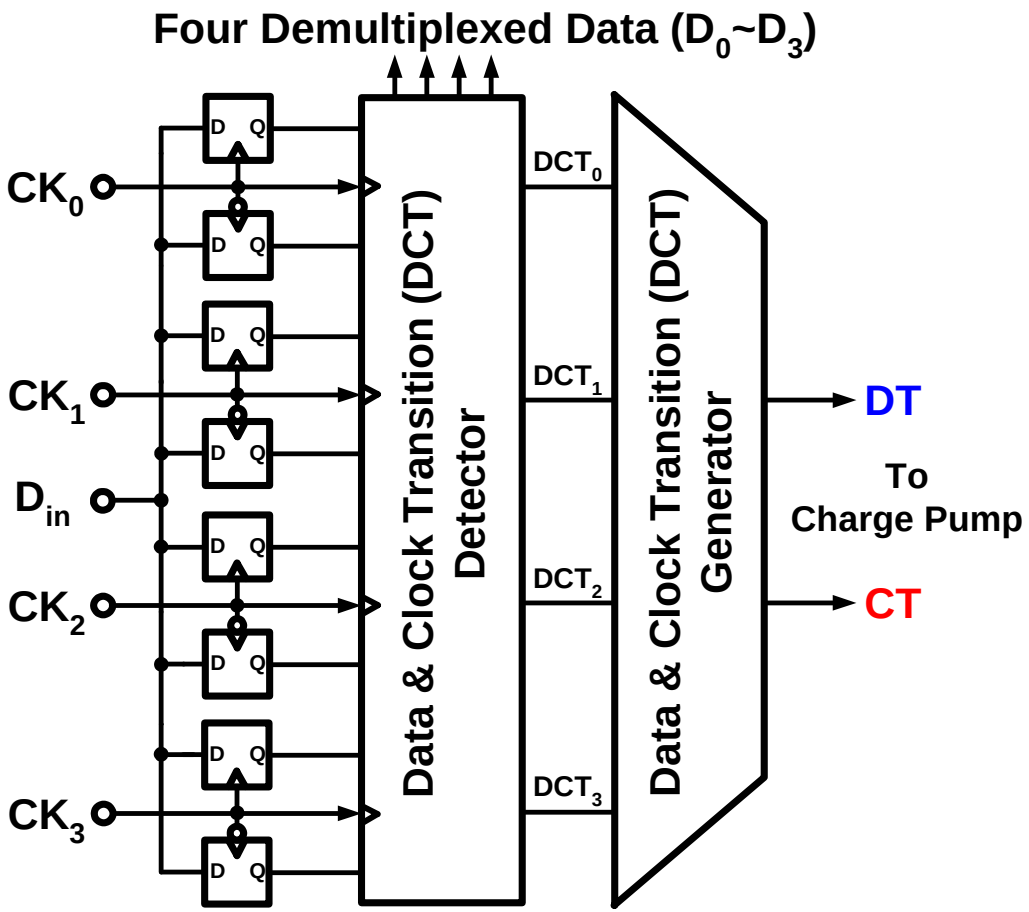
(b) Transistor-Level Implementation

Single Delay Stage of the VCO



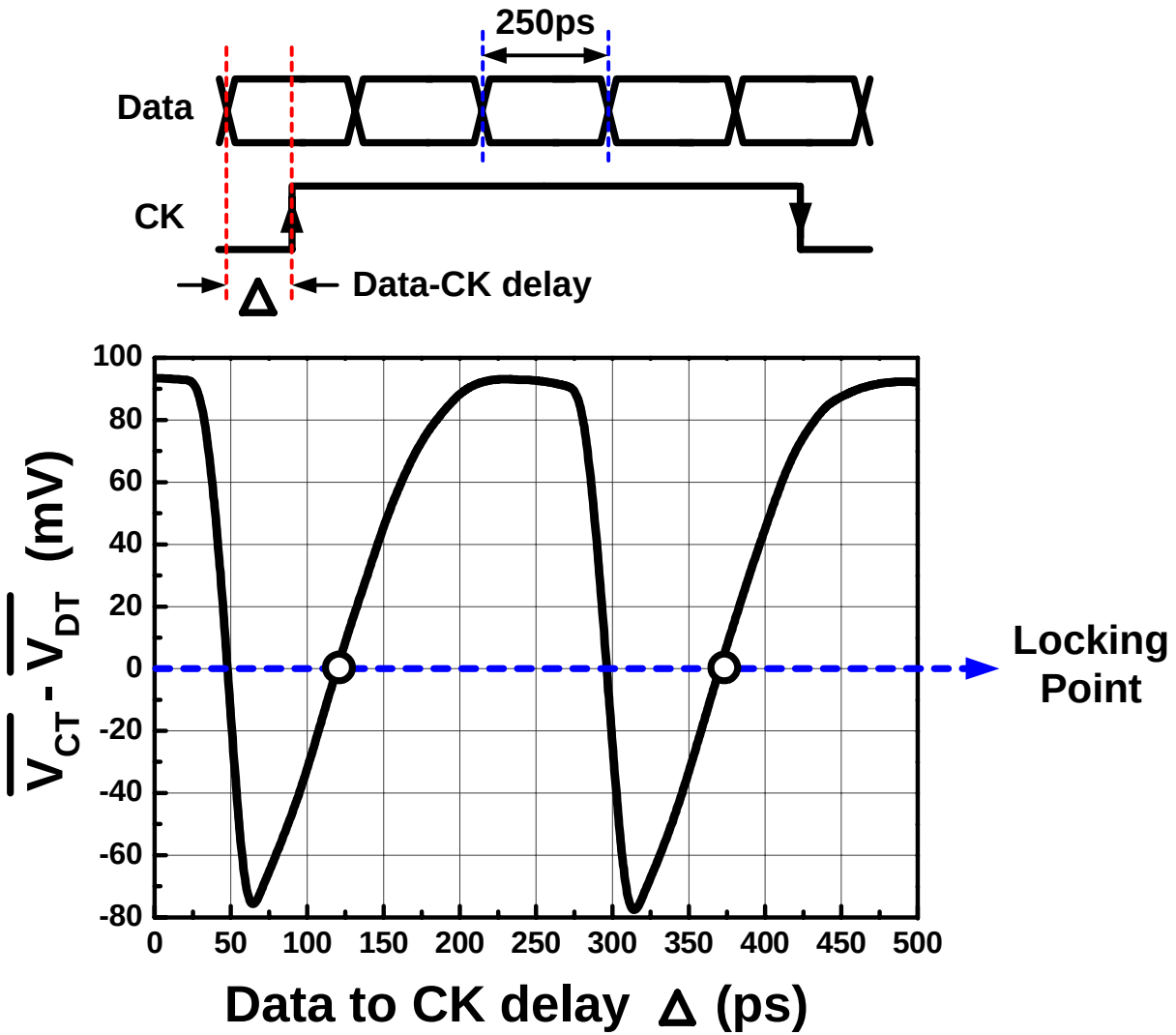
$$\therefore\ \omega_{osc} = \omega_{FR} + K_{\text{VCO\_Fine}} V_{\text{fine\_ctrl}} + K_{\text{VCO\_Coarse}} N \quad \text{for } N = 0,\ldots,63$$

1/8-Rate Linear Phase Detector



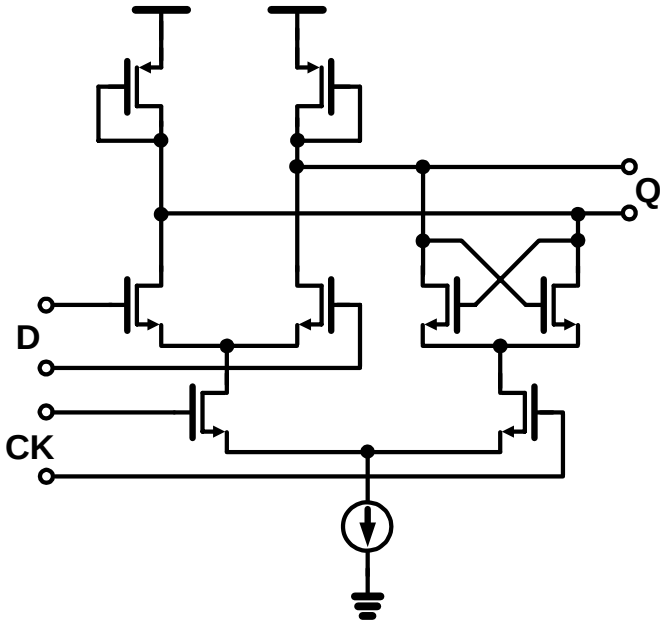
- Three tasks
  - Data Transition Detection
  - Linear phase error detection
  - Data regeneration
- Data demultiplexing
- No systematic offset
- Employing proposed folded current-mode logic family (D-latch, MUX, and XOR)

1/8-Rate Linear PD Characteristic



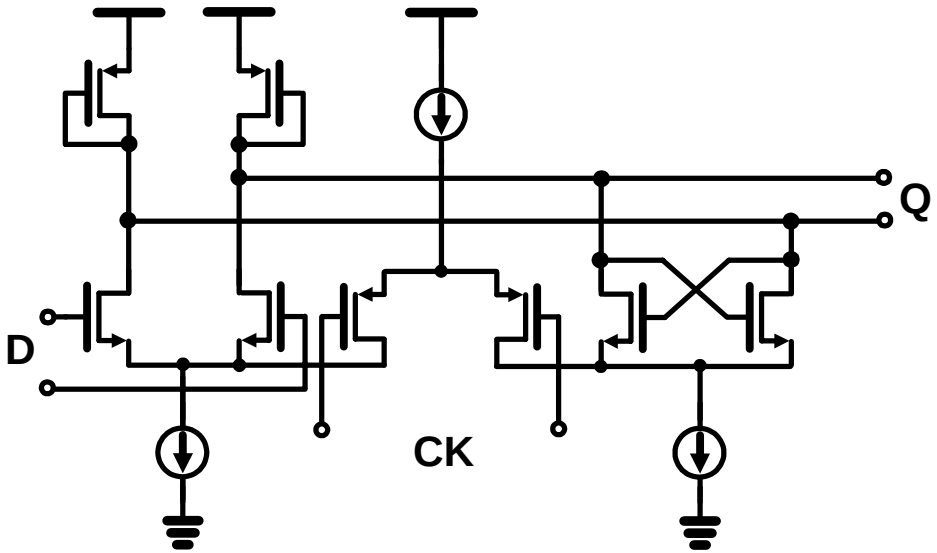
Current-Mode Logic (CML)

Conventional CML D-Latch



- ☺ High speed operation
- ☺ Low power consumption
- ☹ High supply voltage
- ☹ Need for level shifter

Proposed Folded CML D-Latch

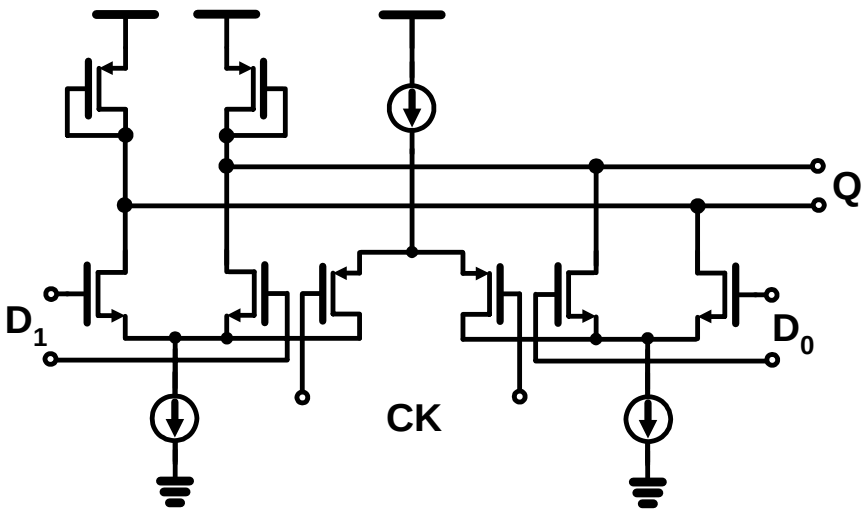


- ☺ Higher speed operation
- ☺ Low supply voltage
- ☺ No need for level shifter
- ☺ Wide input/output range
- ☹ High power consumption
- ☹ Large area

Proposed Folded CML Family *

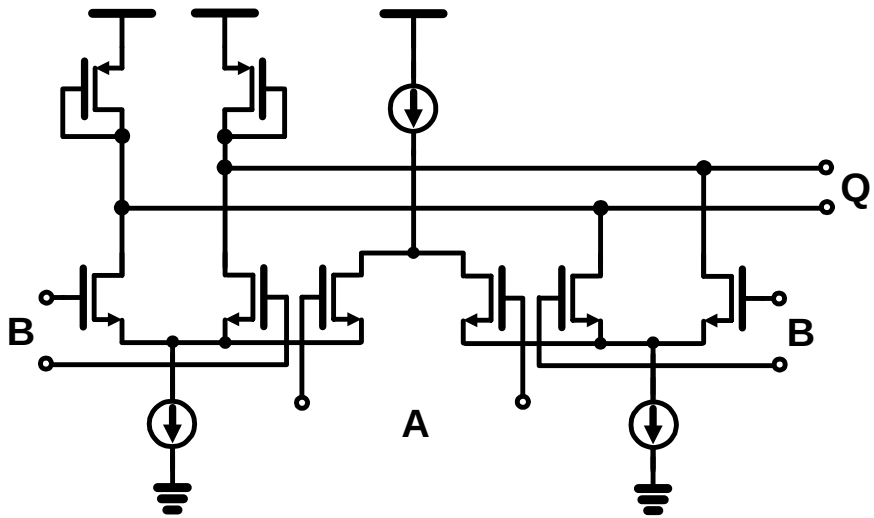
Folded MUX *

$$Q = CK \cdot D_1 + \overline{CK} \cdot D_0$$



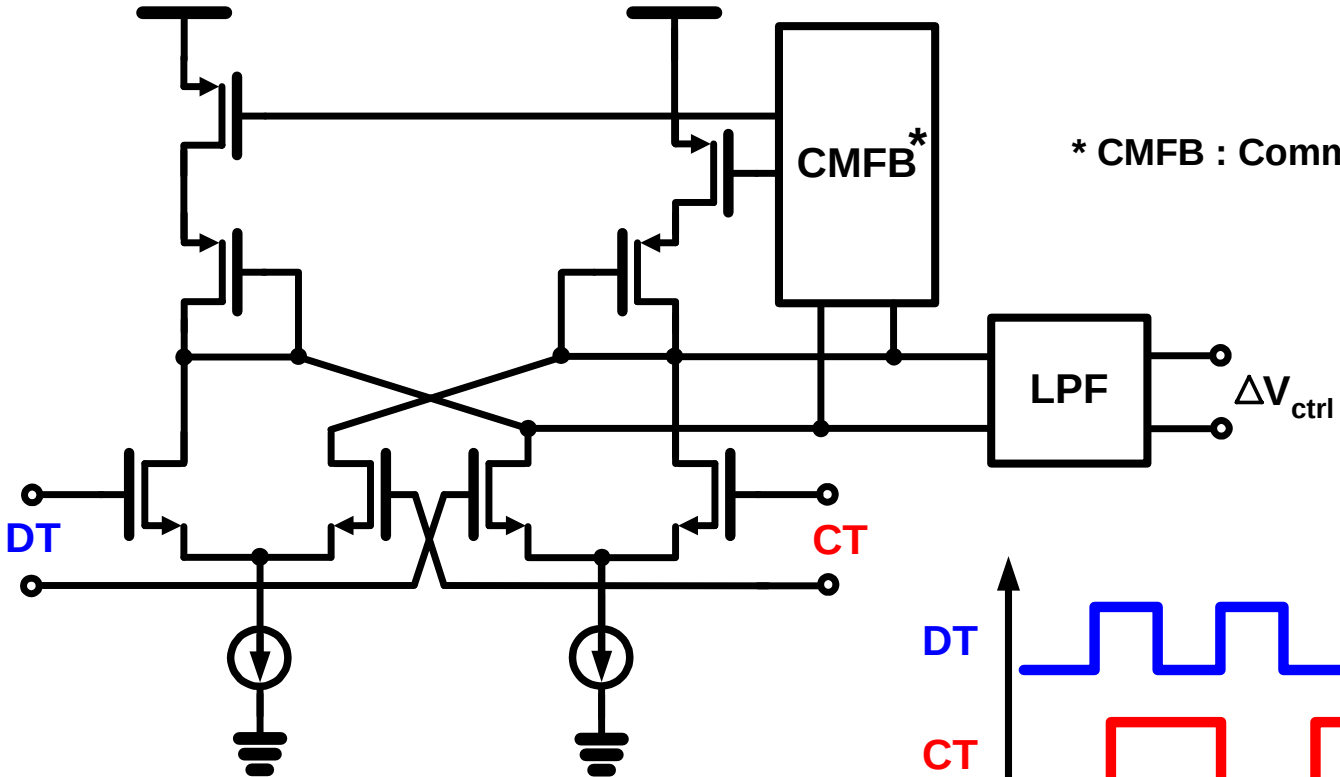
Folded XOR *

$$Q = A \cdot \overline{B} + \overline{A} \cdot B = A \oplus B$$

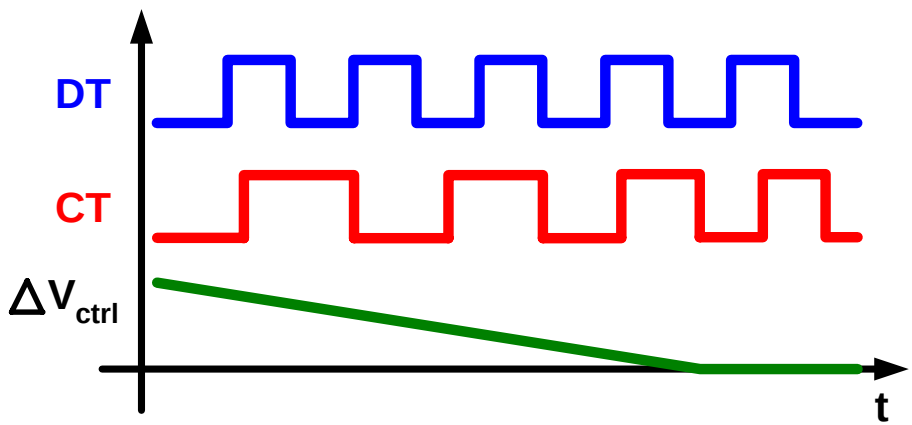


* S.-J. Song, et al., to be published for JSSC, July 2003

Fully Differential Charge Pump



* CMFB : Common-Mode Feedback



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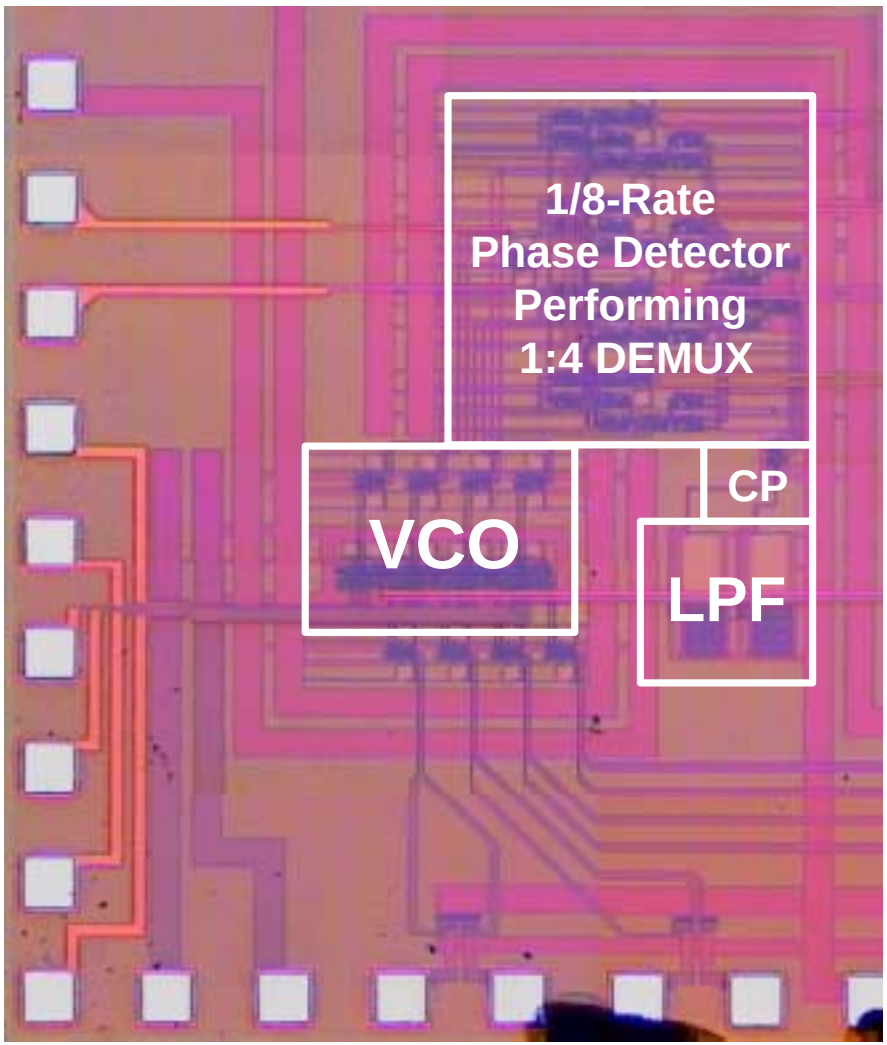
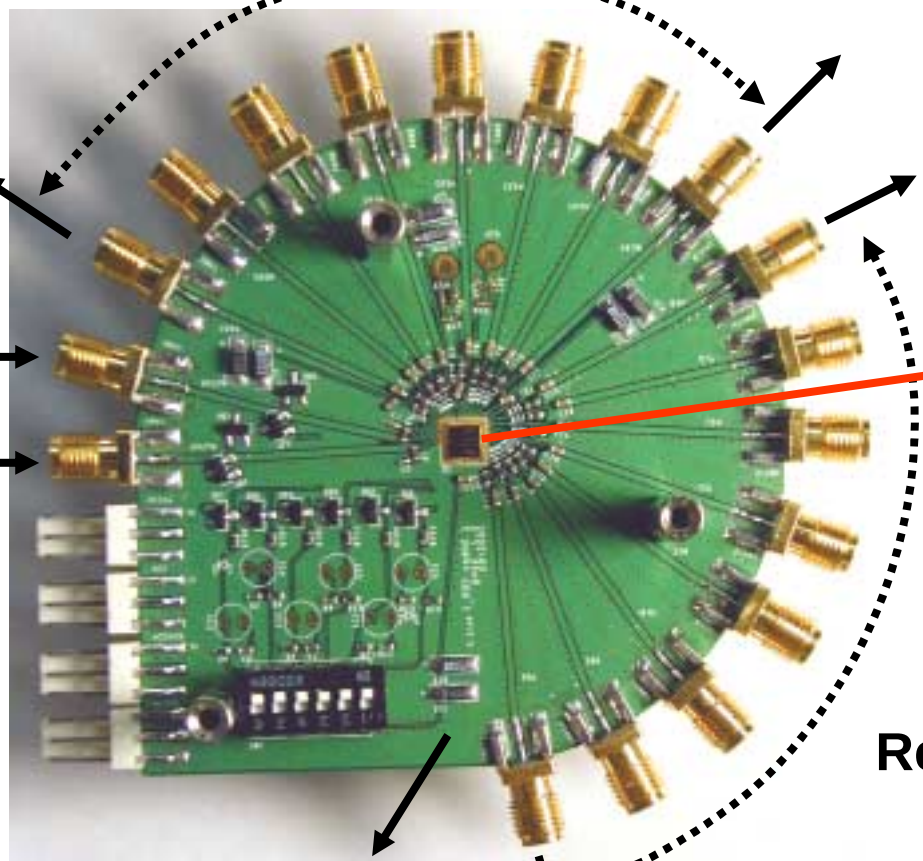
Chip Microphotograph



- 0.25-μm Standard CMOS
- 0.9 x 1.0 mm²

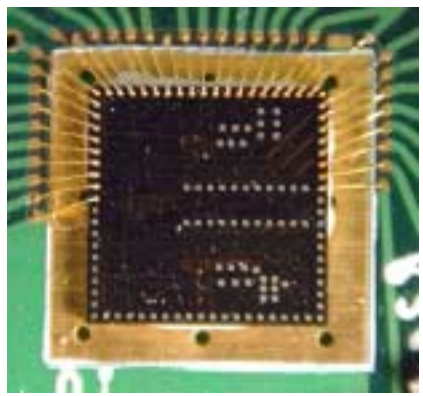
Test Fixture

Four 0.5GHz Recovered Clock Out



4-Gb/s Data In

Gold Wire Bonding

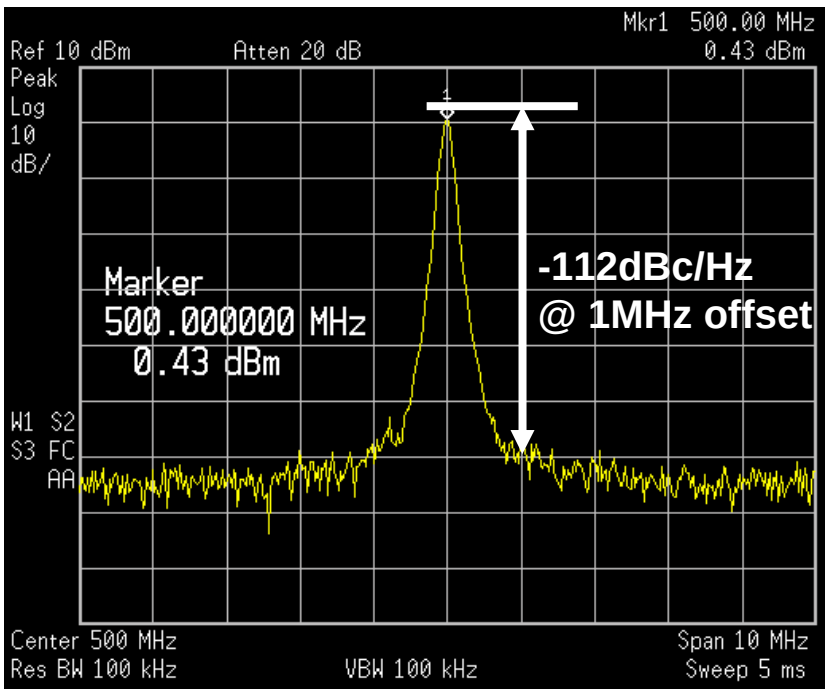


Four 1-Gb/s
Recovered Data Out

FR-4 PCB

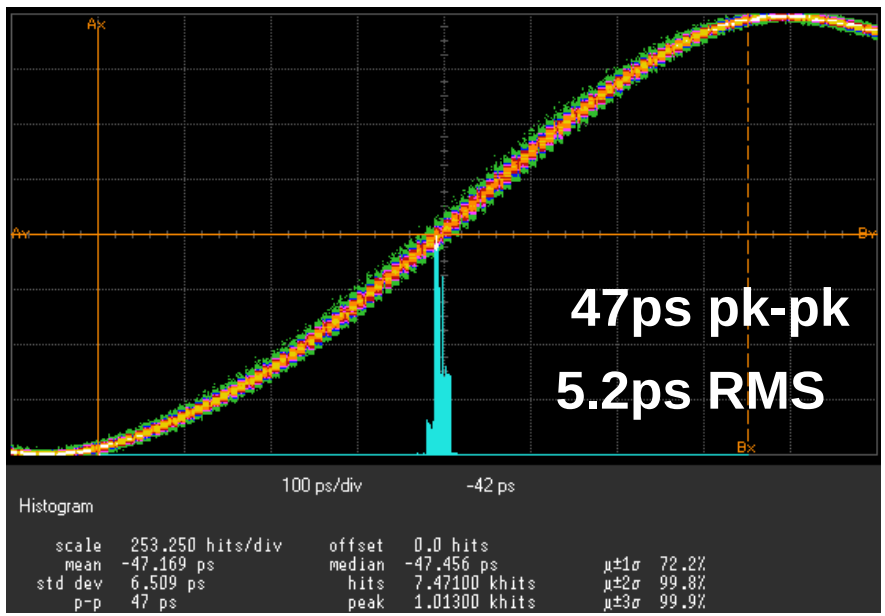
Measured Recovered Clock

- For 2^{31}-1 PRBS input data at 4-Gb/s,



10 dB/div

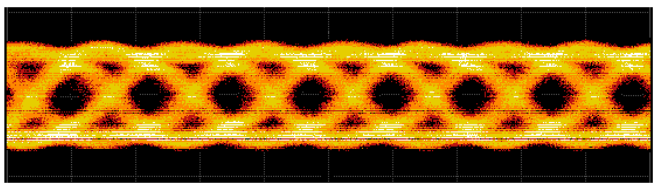
1 MHz/div



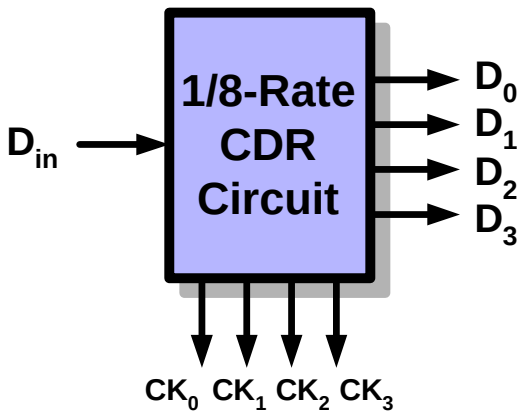
100 ps/div

Measured Eye Diagrams

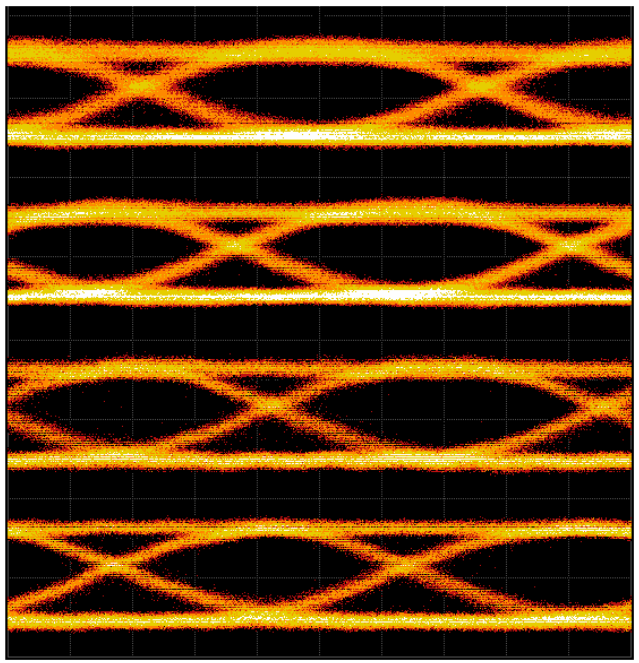
2^{31}-1 PRBS Data Input (4-Gb/s)



V: 200 mV/div, H: 200 ps/div

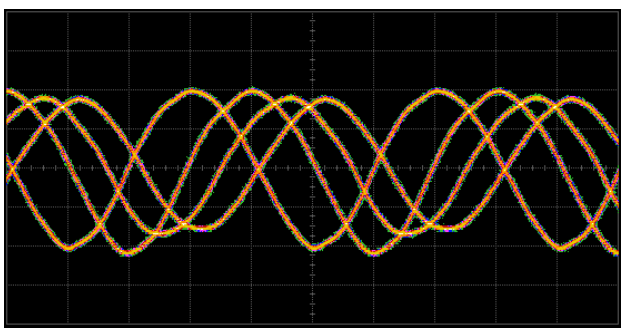


Four Recovered Data Output (1-Gb/s)



V: 200 mV/div, H: 200 ps/div

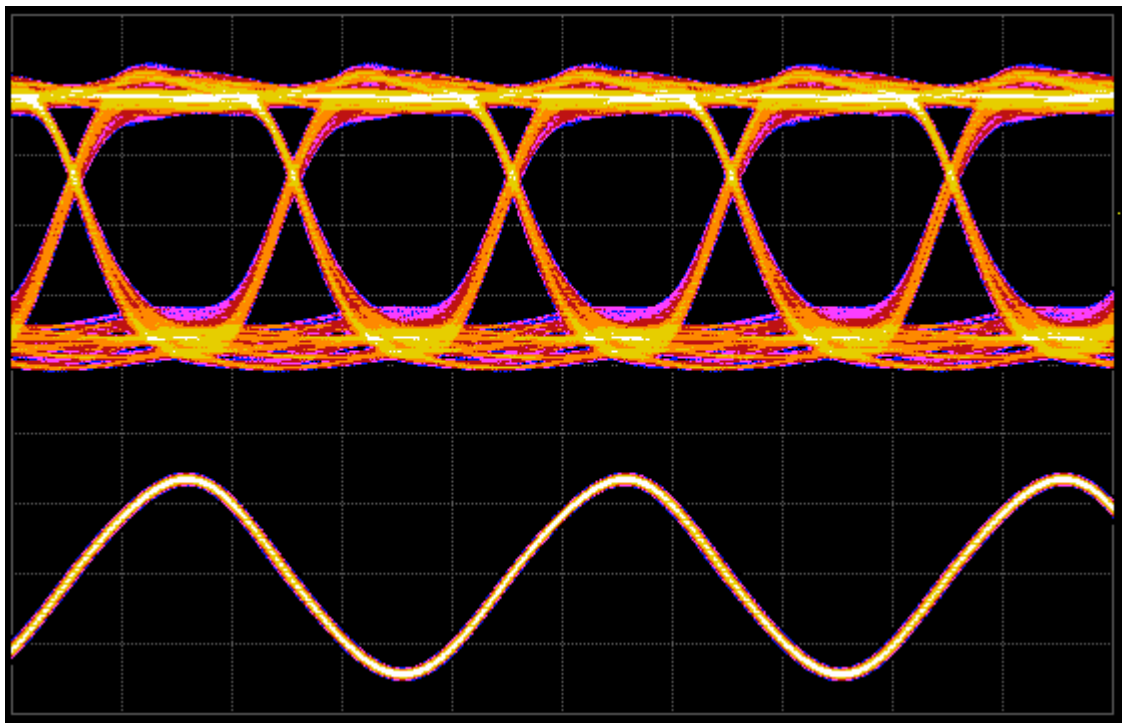
Four Recovered Clock Output (0.5GHz)



V: 200 mV/div, H: 500 ps/div

Recovered Clock and Data

- For 2^{31}-1 PRBS input data at 4-Gb/s,

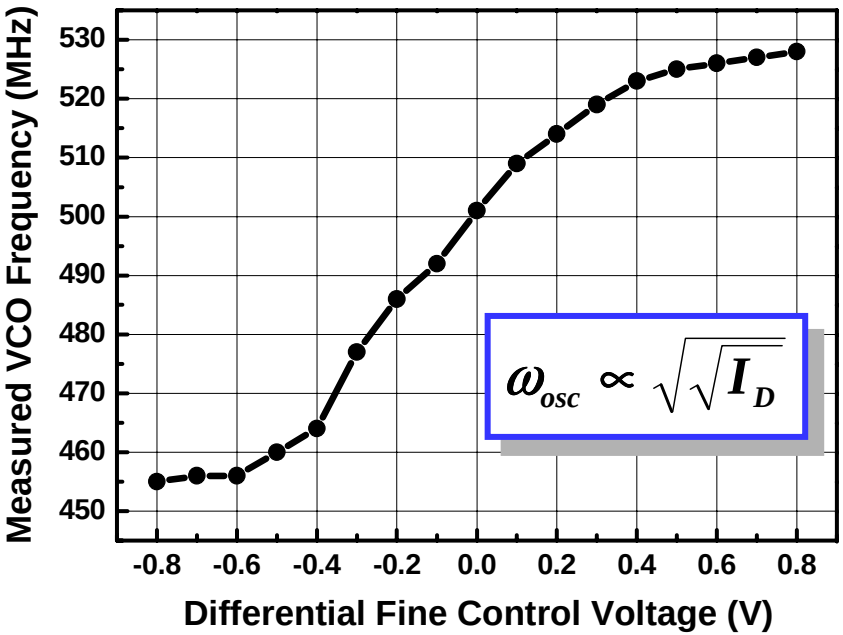


1-Gb/s Demultiplexed Recovered Data (D_0)

0.5GHz Recovered Clock (CK_0)

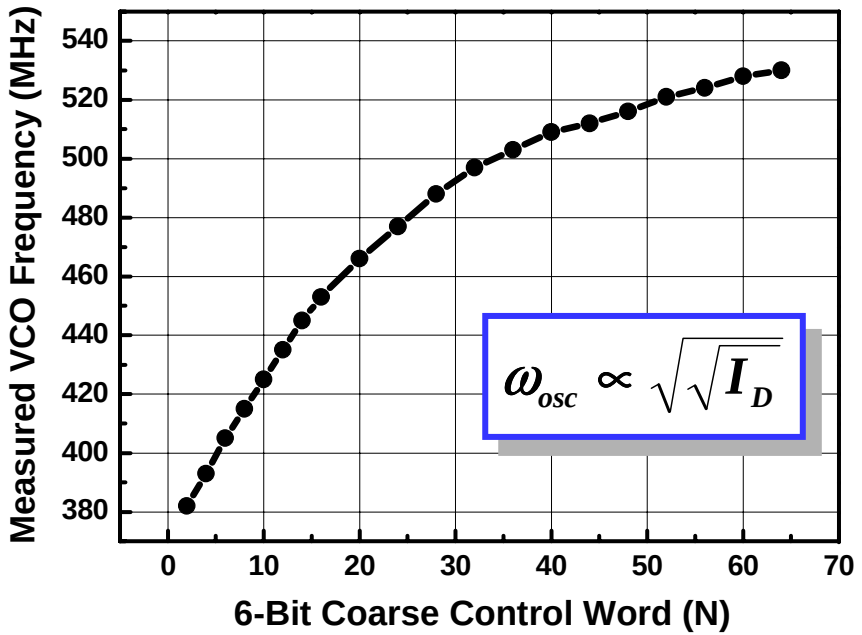
Measured VCO Characteristic

Differential Fine Tuning



- K_{VCO_Fine} = 75 MHz/V
- Fine Tuning Range = 70 MHz (14%)

6-Bit Digital Coarse Tuning



- K_{VCO_Coarse} = 2.5 MHz/Word Step
- Coarse Tuning Range = 150 MHz (30%)

$$\therefore\ \omega_{osc} = \omega_{FR} + K_{VCO\_Fine} V_{fine\_ctrl} + K_{VCO\_Coarse} N \quad \text{for } N = 0,\ldots,63$$

Performance Summary

NRZ Data Rate	4-Gb/s
Recovered Clock	0.5 GHz
Recovered Data	Four 1-Gb/s
Capture Range	16 MHz
VCO Fine Tuning Gain	75 MHz/V
Phase Noise at 1-MHz offset	-112 dBc/Hz
Clock Jitter for 2^{31}-1 PRBS	5.2 ps RMS
BER for 2^{31}-1 PRBS	$< 10^{-6}$
Power Dissipation (excluding output buffers)	70 mW
Supply Voltage	2.5 V
Active Area	0.9 x 1.0 mm^2
Technology	0.25-μm standard CMOS

Proposed Performance Index

- From O. T.-C. Chen, et al., JSSC, Jan. 2002,
- Frequency index in PLL is derived by

$$F^* = \left(\frac{\text{Technology}}{0.35\mu\text{m}}\right)\cdot\left(\frac{1.8\text{ V}}{\text{Supply Voltage}}\right)\times F \text{ (MHz)}$$

- By taking account into power consumption in CDR circuit,
- Proposed performance index in CDR circuit can be expressed as

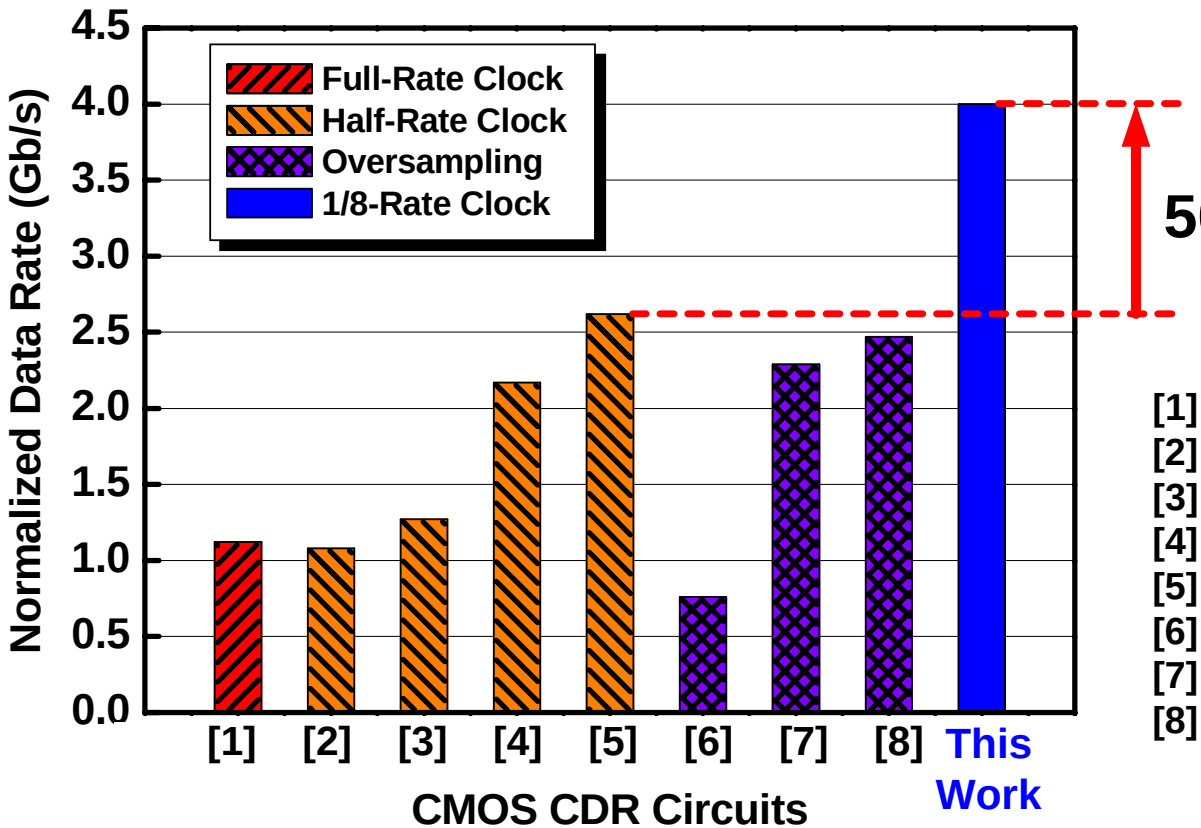
$$\text{Normalized Data Rate} = \left(\frac{\text{Technology}}{0.25\mu\text{m}}\right)\cdot\left(\frac{70\text{ mW}}{\text{Power Consumption}}\right)\cdot\left(\frac{\text{Supply Voltage}}{2.5\text{ V}}\right)\times\text{Data Rate (Gb/s)}$$

Performance Comparison

Reference	CDR Technique	Normalized Data Rate	Data Rate	Power Consumption	Supply Voltage	Technology
[1]	Full-Rate Clock	1.12-Gb/s	1-Gb/s	300 mW	5 V	0.6-μm CMOS
[2]	Half-Rate Clock	1.08-Gb/s	1.25-Gb/s	150 mW	3.3 V	0.35-μm CMOS
[3]	Half-Rate Clock	1.27-Gb/s	10-Gb/s	285 mW	1.8 V	0.18-μm CMOS
[4]	Half-Rate Clock	2.17-Gb/s	1-Gb/s	85 mW	3.3 V	0.5-μm CMOS
[5]	Half-Rate Clock	2.62-Gb/s	6-Gb/s	83 mW	1.8 V	0.18-μm CMOS
[6]	3x-Oversampling	0.76-Gb/s	4-Gb/s	973.5 mW	3.3 V	0.5-μm CMOS
[7]	3x-Oversampling	2.29-Gb/s	5-Gb/s	153 mW	2.5 V	0.25-μm CMOS
[8]	2x-Oversampling	2.47-Gb/s	4-Gb/s	84 mW	1.93 V	0.24-μm CMOS
This Work	1/8-Rate Clock	4-Gb/s	4-Gb/s	70 mW	2.5 V	0.25-μm CMOS

$$\text{Normalized Data Rate} = \left(\frac{\text{Technology}}{0.25\mu m}\right)\cdot\left(\frac{70\,\text{mW}}{\text{Power Consumption}}\right)\cdot\left(\frac{\text{Supply Voltage}}{2.5\,\text{V}}\right)\times\text{Data Rate (Gb/s)}$$

Normalized Performance Comparison



50% Increase

[1] H. Wang, et al., ISSCC, 1999
[2] K. Iravani, et al., CICC, 1998
[3] J. E. Rogers, et al., ISSCC, 2002
[4] M. Rau, et al., JSSC, July 1997
[5] K. Nakamura, et al., SOVC, 1998
[6] C.-K. Yang, et al., JSSC, May 1998
[7] S.-H. Lee, et al., JSSC, Dec. 2002
[8] M.-K.E. Lee, et al., SOVC, 2002

Outline

- Introduction
- Motivation
- Problem Definition
- Proposed 1/8-Rate CDR
- Building Blocks
- Measurement Results
- **Conclusion & Further Works**

Conclusion

- A high-speed and low-power CDR circuit has been introduced :
  - Exploiting 1/8-rate clock technique
  - Using a 0.25-μm standard CMOS technology
  - Single functional block merging clock recovery circuit, decision circuit, divider, and 1:4 DEMUX

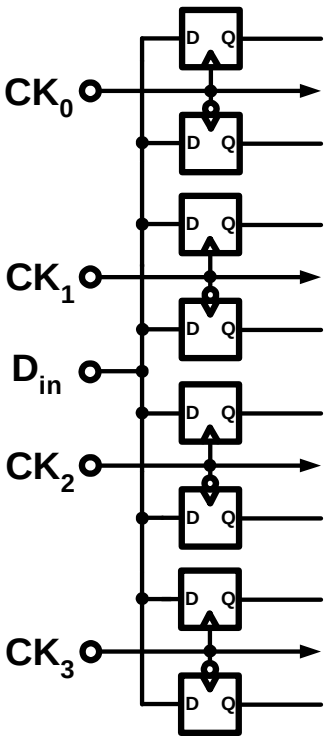
- The proposed CDR demonstrates 4-Gb/s and 70mW operation suitable for low cost optical interconnection applications.

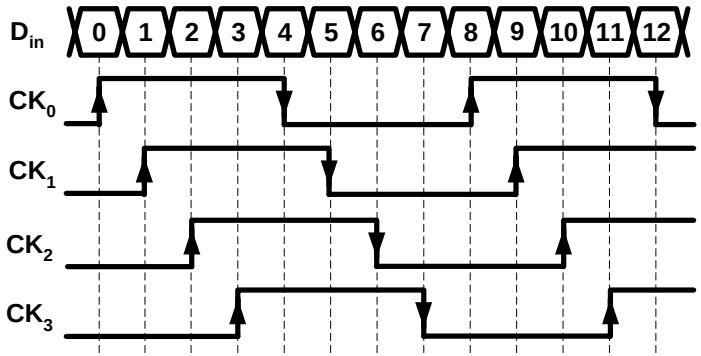
Further Works

- Fully Integrated Frequency-Locked Loop
  - Broadband frequency detection
- Improvement of BER
  - To improve SNR
  - To improve Clock Jitter Characteristic
- Need for Detailed Mathematical Analysis

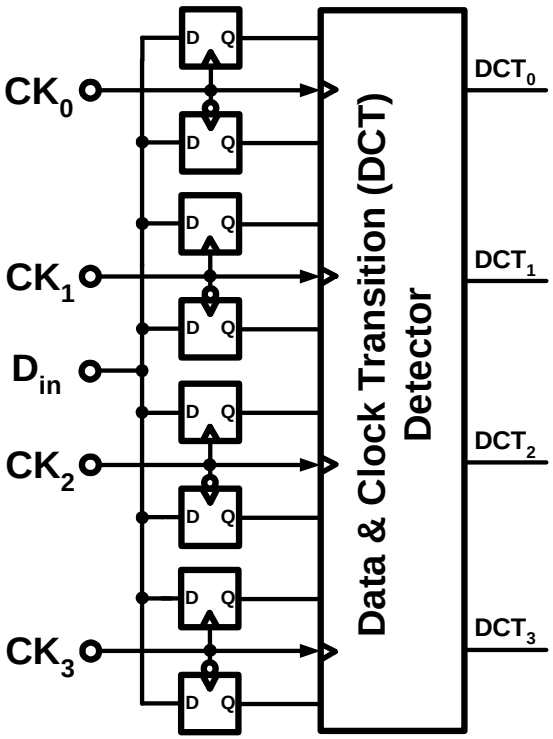
Supplemental Materials

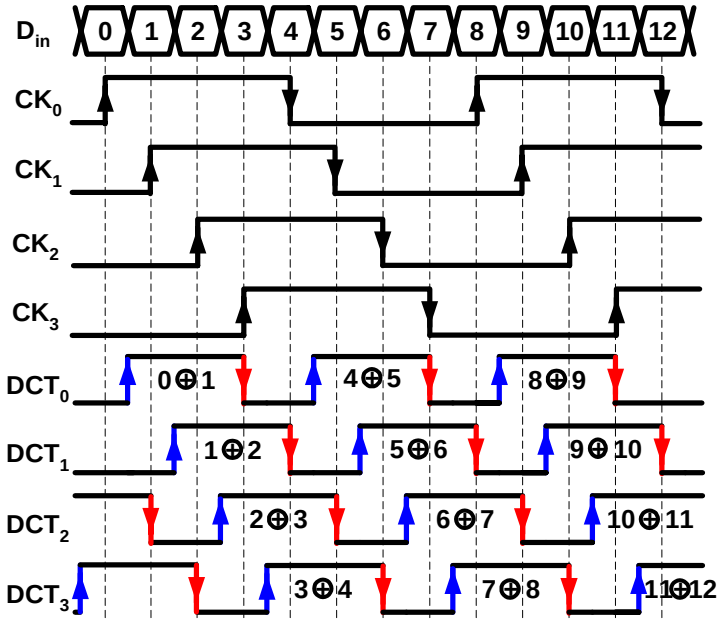
Operation of 1/8-Rate PD (1/4)



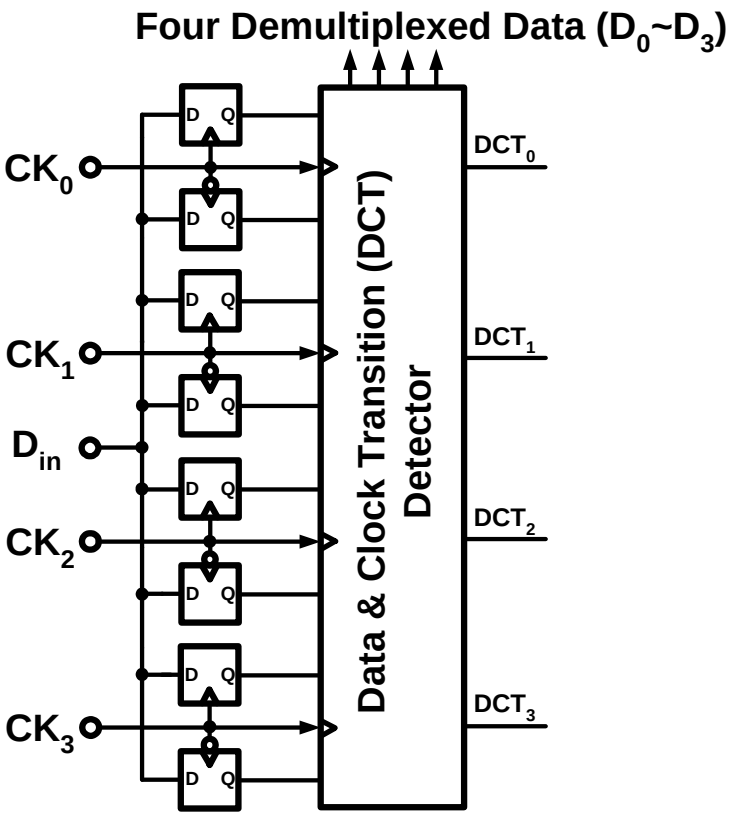


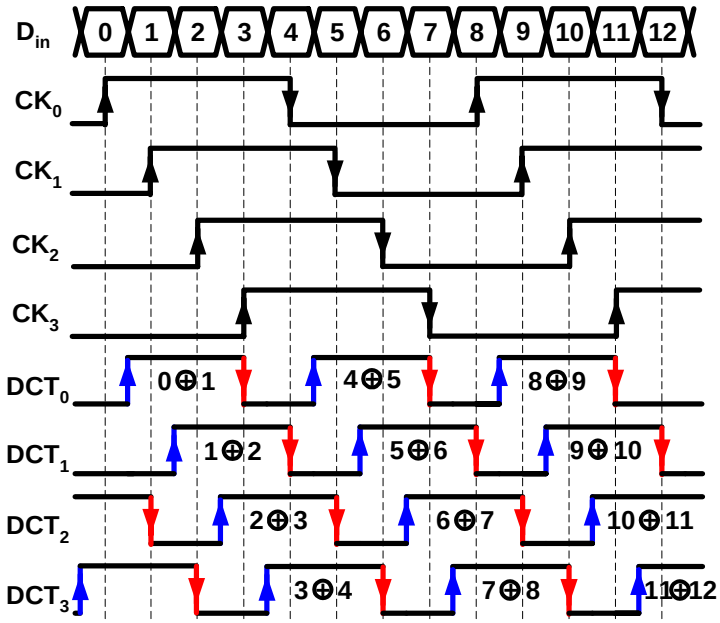
Operation of 1/8-Rate PD (2/4)

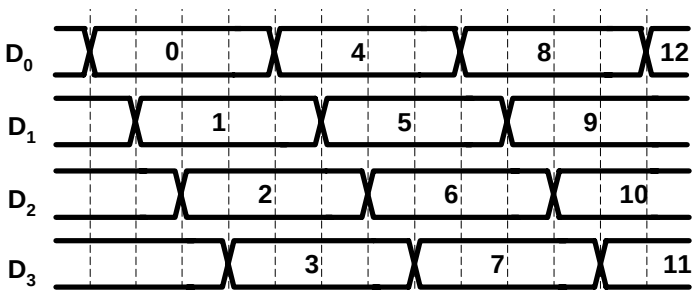




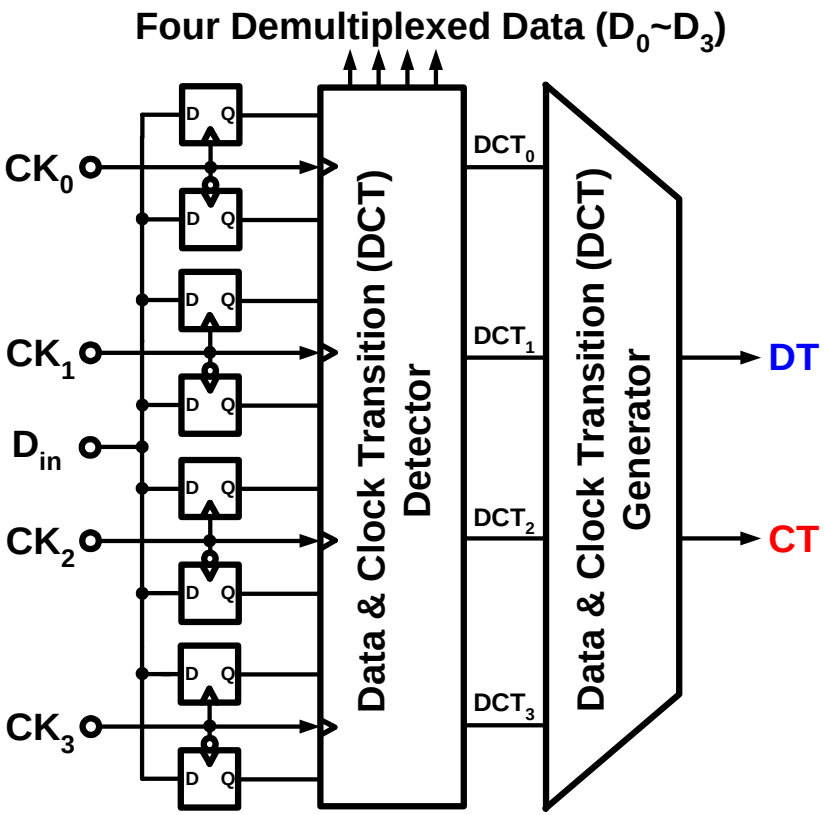
Operation of 1/8-Rate PD (3/4)

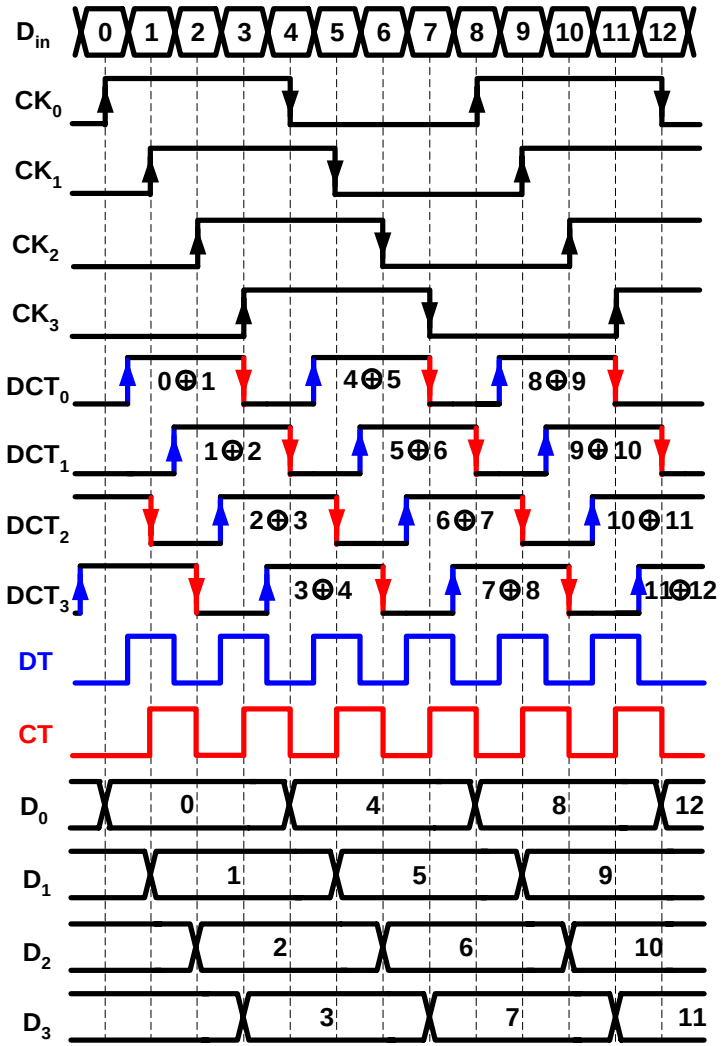






Operation of 1/8-Rate PD (4/4)





Example