석사학위논문

Master's Thesis

무선 환경 감지를 위한 센서들을 집적시킨 저 전력, 고주파 대역 RFID 태그 칩의 설계 및 구현

Design and Implementation of Ultra-low power, UHF RFID Tag Chip Integrated with Sensors for Wireless Environmental Monitoring

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Design and Implementation of
Ultra low-power, UHF RFID Tag Chip Integrated with Sensors for Wireless Environmental Monitoring

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Abstract

A RF-powered transponder with temperature and photo sensors is designed for environmental monitoring. The transponder gathers its operating power from external ISM (860 - 960MHz) band RF signal and senses ambient temperature and light intensity. The power-efficient and robust clock generator which consists of the temperature compensated ring oscillator and the oversampling synchronizer is proposed. The single slope ADC utilized in the integrated sensors can reduce their power and area overheads efficiently. The internal clock frequency has variation less than 7% for 1.5-V supply voltage and 90-^{o}C temperature changes. The proposed transponder can operate up to 3.4-m from the base station in the 2-W transmit power and the total power consumption is only 5.1-μW during active state. The transponder is fabricated in 0.25-μm CMOS process and occupies 0.4-mm^{2}.

사랑하는 가족에게 바칩니다.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Recently, the radio frequency identification is very popular in a number of areas including access control, supply chain management, public transportation and many others. Moreover, continuous improvements of the UHF RFID technology are creating new applications overcoming the size limitation and the short range communication confronted in the widespread 13.56-MHz RFID [1, 2]. One of the most valuable applications supported by the UHF RFID system is the wireless environmental monitoring. Traditionally, the batteryless and wireless sensors borrowing RFID technology have been widely utilized in the bio-chemical telemetries such as bio-assays and retinal prosthesis [3, 4]. However, the architectures adopted for such systems cannot be applied to the environmental monitoring because of their functional deficiency and the short operational distance. The IC

presented in this paper can provide the operating range more than 3-m which is suitable for the environmental monitoring and reduce the total power consumption down to only 5-μW even with the integration of multiple sensors.

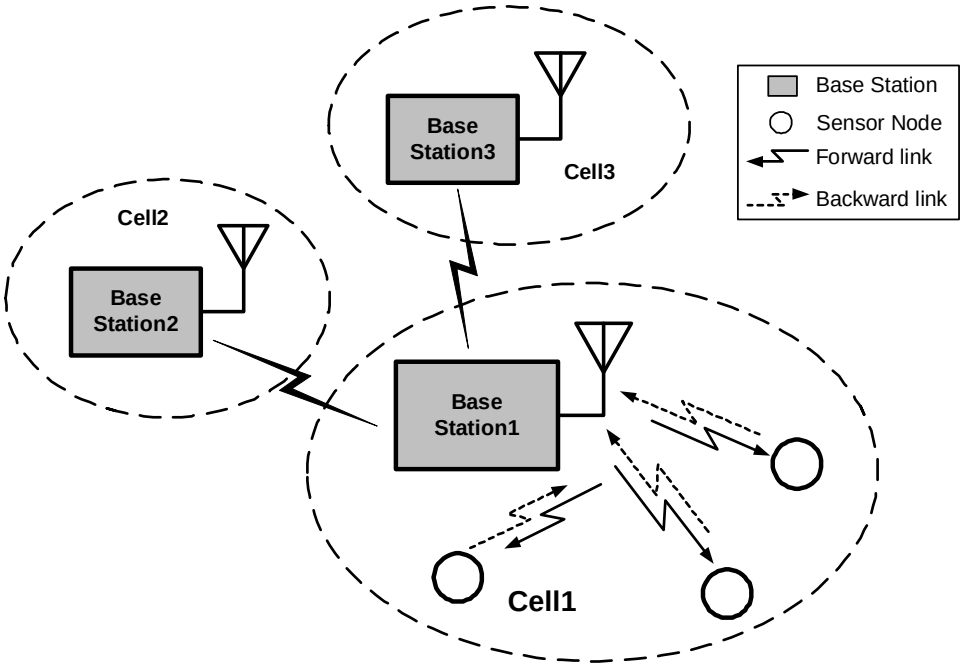


Figure 1.1. Environmental monitoring system using RFID

Fig. 1.1 shows the environmental monitoring system using RFID. In this system, the measured space is divided into several cell areas. Each sensor

node in the cell area has the master-slave relation with the base station. When the sensor nodes are activated by the RF-power coming from the base station, they can start sensing operations and transmit their sensed information. In the construction of the system, the batteryless and wireless characteristics of the RFID can be applied for the small size and easy deployment of multiple sensor units in the measured place. And the ID number assigned to each sensor can provide the efficient management to the base station.

According to these considerations, this work implements a transponder in which the RFID tag and the environmental sensors are integrated. The transponder operates in the UHF (860-960MHz) band for the longer operational distance and the smaller antenna size. As the sensors, the temperature and photo sensors are adopted because these sensors can represent the environmental conditions well and they can be implemented easily in the standard CMOS technology.

1.2 Thesis Organization

The overall descriptions of the proposed system architecture are presented in Chapter 2. Chapter 3 describes the design of the building blocks in detail.

In Chapter 4, the implementation result of the sensor chip and its measurements are presented. Finally, conclusions are made in Chapter 5.

CHAPTER 2

SYSTEM ARCHITECTURE

2.1 Proposed System Architecture

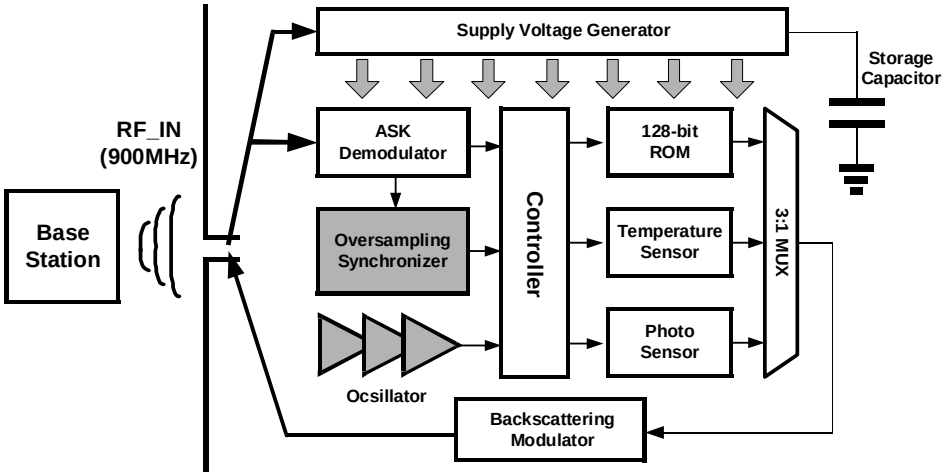


Figure 2.1. Architecture of the proposed transponder

The architecture of the proposed transponder is shown in Fig. 2.1. The

incident RF power from the base station is converted to the DC voltage by the supply voltage generator and stored in a large capacitor. The stored energy can provide the operating currents to all active blocks in the transponder. The forward communication from the base station is done by modulating the input RF signal in ASK form. The modulation depth is 70-% and the data rate of the forward link is 20-kbps. In typical 13.56-MHz RF transponders, the system clock for the synchronous digital blocks is extracted from the incoming RF signal by using the schmitt trigger [5, 6]. But when the carrier frequency is much higher for the longer operational distance and the small antenna size, the clock extraction is inefficient because of its huge power consumption. A recent work which utilizes clock extraction from the 900-MHz RF signal reported 1.1-mA current consumption during the operation [7]. So, the recent UHF band RFID systems choose other approaches for the clock generation. A clock modulation is one of the most widely used techniques [1]. That is, the clock signal is modulated on the envelope of the input RF signal and the clock and data are demodulated simultaneously in the transponder. However, it has some disadvantages. Since the modulated data should always have the clock information, the selection of the coding methods is limited. And the power loss due to the continuous modulation of RF envelope is unavoidable. To remedy such

problems, the proposed transponder has the clock generator fully independent of the external RF signal. Because the required clock frequency is much lower than the input frequency, the low power clock generator can be obtained by this architecture. Additionally, there is no need for the continuous modulation and the special coding of the transmitted data. But this structure also has some drawbacks which are the frequency variation and the phase error. To deal with the difficulties, an oscillator robust on both of the supply voltage and temperature variations is designed. In addition, an oversampling synchronizer is implemented to enhance the timing correlation between the clock and data.

The two integrated sensors have the low power structure and the single slope ADC based on the time to digital converter. Thanks to its simplified structure and superior power-efficiency compared to other types of ADC, the area and power burdens caused by the additional sensor blocks can be reduced efficiently. And the total bias current of the amplifiers used in the sensors is controlled under 1-μA.

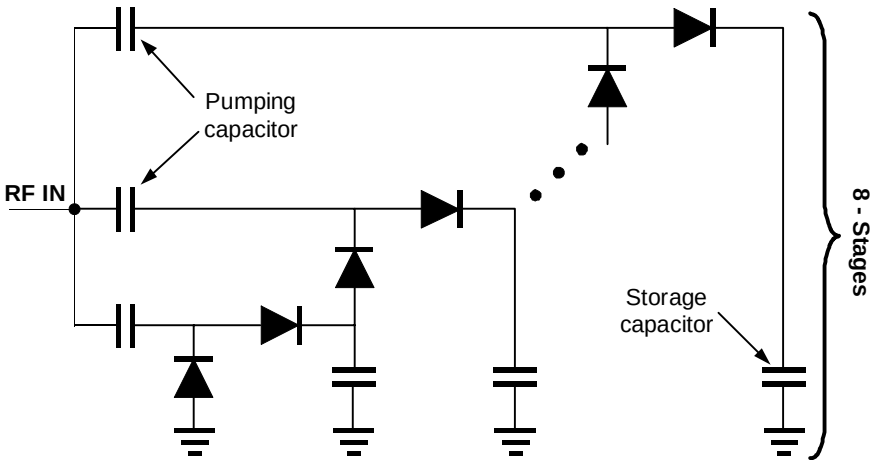
CHAPTER 3

BUILDING BLOCKS DESIGN

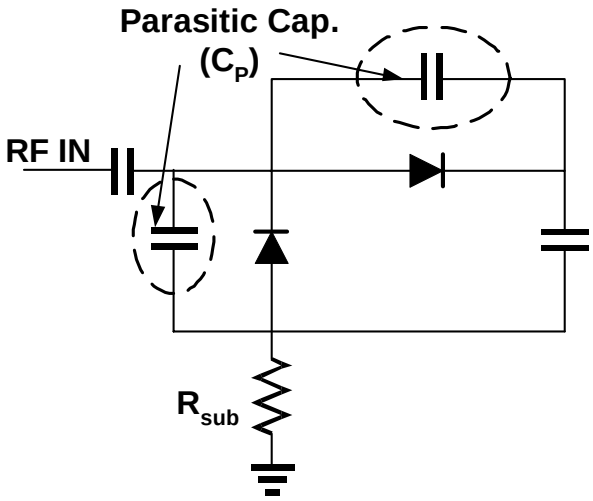
3.1 Supply Voltage Generator

The DC supply voltage for the transponder is generated from the incident RF power by using the charge pump called dickson voltage multiplier. Fig. 3.1.(a) shows the multistage structure of the dickson multiplier which can generate the enough supply voltage from the low swing of the input RF signal. The schottky diode utilized as the pumping unit is a common choice in most passive type RF transponders because of its small resistance and low threshold voltage. The major considerations in the design of the charge pump are the power efficiency and the ripple of the supply voltage. These constraints bring lots of trade-offs in the size optimization of the devices such as the schottky diode, pumping and storage capacitors.

3.1.1 Trade-offs for power efficiency



(a)



(b)

Figure 3.1. (a) Dickson voltage multiplier

(b) Unit stage including parasitic devices

Since the voltage multiplier is directly connected to the antenna, the antenna impedance should be matched to the complex conjugation of the input impedance of the multiplier for the highest power transfer. With the conjugate matching, we can assume the maximum power is transferred from the antenna, and exclude the effect of the antenna in power analysis. Then, the power efficiency of the voltage multiplier can be defined as

$$Power\,efficiency = \frac{Power\ consumed\ in\ transponder}{Power\,consumed\,in\,transponder + Power\,loss} \quad (1)$$

For a fixed power consumption of the transponder core, the power loss in the voltage multiplier should be minimized to get the best efficiency. When the parasitic elements in Fig.3.1.(b) are included, the power loss can be approximated to

$$\begin{aligned} P_{loss} &= \frac{1}{2}\, Re\{V_{in} * \frac{V_{in}}{Z_{in}}\} = \frac{1}{2}|Vin|^2\ Re\{Y_{in}\} \\ &\approx \frac{1}{2}|V_{in}|^2\ Re\{\frac{1}{R_{sub} - j(1/4\pi fnC_P)}\} \\ &\approx 8|V_{in}|^2 (\pi fnC_P)^2 R_{sub} \end{aligned} \quad (2)$$

where V_{in} is the phasor of the input RF signal, R_{sub} is the resistance of the doped silicon substrate, the C_P is the sum of the parasitic capacitances which are the junction, substrate capacitance of the schottky diode and the coupling capacitance from the bottom plate of the pumping capacitor to ground and the parameter n represents the stage number of the voltage multiplier.

From the equation, the parasitic capacitance of the schottky diode should be minimized to enhance the power efficiency. The only way to decrease the parasitic effect is reducing the size of the schottky diode. However, the requirement on the series resistance of the schottky diode prevents the free scale-down of the device. For the parameter n, as the number of the stages increases, the swing level of the input signal can be reduced. But, the stage number cannot be raised arbitrarily because the power loss shows the quadratic dependency on the value and the power efficiency can degrade severely.

3.1.2 Ripple constraint

During the forward communication, the power received in the transponder is continuously turned on and off with the 50-μs period due to the deep modulation on the envelope of the input RF signal. The voltage drop in the turn-off phase is given by

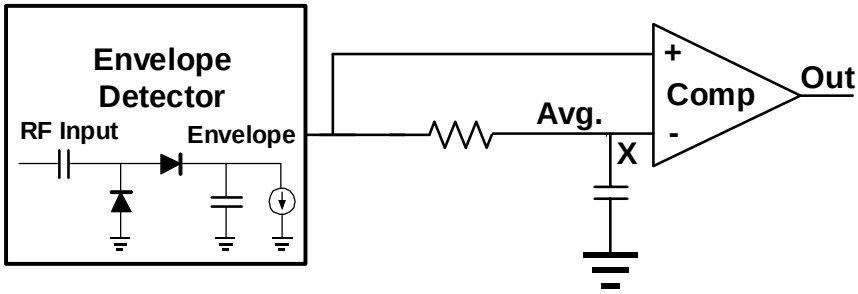
$$V_{Ripple} = \frac{I_{avg} T_b}{C_S} \qquad (3)$$

where I_{avg} is the average current of the transponder core, the T_b is the bit period of the modulated data and C_S is the storage capacitance. To suppress the ripple, the storage capacitor should be enlarged as much as possible. But, the scale-up of the storage device can delay the start-up time and consume the silicon area significantly. As a result, the size of the storage capacitor should be selected carefully through the trade-off among the area, response time and the noise margin due to the ripple.

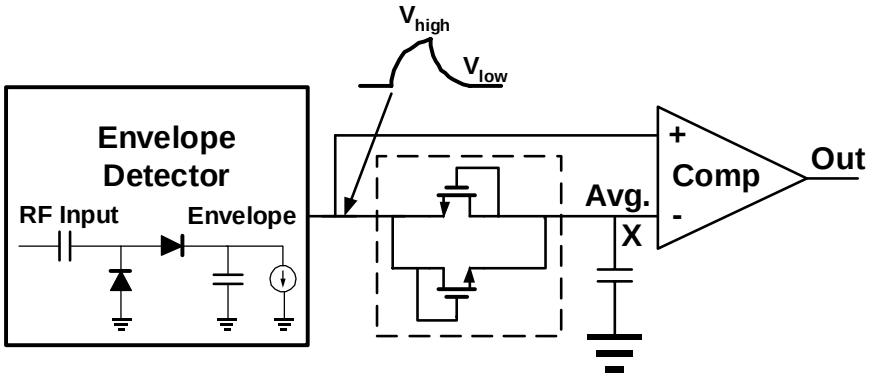
3.2 ASK Demodulator

To obtain full swing bit sequence from the ASK modulated signal, the envelope of the input signal is compared to average level and the difference is regenerated. Typically, the average signal is obtained by sending the envelope signal to RC network with large time constant as shown in Fig. 3.2.(a) [8]. But, this method needs too large capacitor and resistor resulting in the increase of the chip area . The proposed demodulator of Fig. 3.2.(b) employs diode-connected NMOS pair instead of the huge resistor.

When the envelope signal is at V_{high} and V_{low}, the NMOS pair limits voltage on node X to V_{high}-V_{th} and V_{low}+V_{th}. And when the difference between V_{high} and V_{low} is less than $2V_{th}$, the NMOS in sub threshold acts as a large resistor.



(a)



(b)

Figure 3.2. (a) Conventional ASK demodulator

(b) ASK demodulator using diode-connected NMOS pair

As a result, the NMOS pair can effectively make average signal while saving much area by removing the large passive units.

3.3 Fully Integrated Clock Generator

The clock generator is the essential part to ensure safe operation of the synchronous digital blocks in the transponder. Fig. 3.3. shows the concept of the integrated oscillator for the clock generation. The current starved ring oscillator is often adopted in low power oriented systems, and most of them focus on the robustness against supply voltage variation [9]. However, in the proposed transponder, independence of the reference clock to both of the supply voltage and temperature changes is mandatory for two purposes. The first purpose is the correct sampling of the demodulated data in various conditions and the second one is the accurate operation of ADC in the integrated sensors. Through the first order analysis, the output frequency of the current starved oscillator and the conditions for the supply voltage and temperature compensation can be expressed as

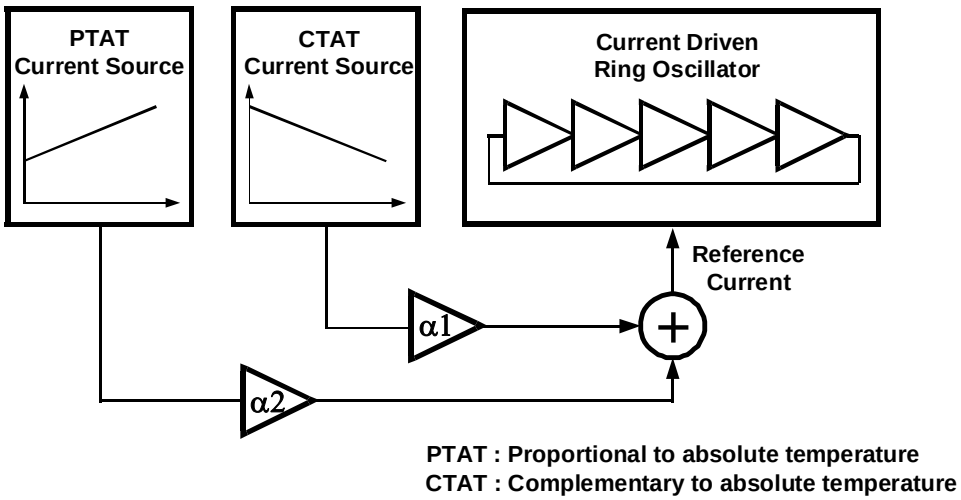


Figure 3.3. Conceptual diagram of the proposed oscillator

$$Output\,Frequency: f_{out} = \frac{I_{drv}}{V_{TH} C_L}$$

$$Supply Voltage Compensation: \Delta f_{out} = \frac{1}{C_L V_{TH}} \frac{\partial I_{drv}}{\partial V_{\sup}} \Delta V_{\sup} \Rightarrow \frac{\partial I_{drv}}{\partial V_{\sup}} = 0$$

$$Temperature Compensation: \Delta f_{out} = \frac{1}{C_L} \frac{(\partial I_{drv} / \partial T) V_{TH} - (\partial V_{TH} / \partial T) I_{drv}}{V_{TH}^{\,2}} \Delta T$$

$$\Rightarrow \frac{\partial I_{drv} / \partial T}{\partial V_{TH} / \partial T} = \frac{I_{drv}}{V_{TH}} = f_{out} C_L \qquad (4)$$

where the I_{drv} is the driving current, the V_{TH} is the threshold voltage of the mosfet in the oscillator, and the C_L is the load capacitance of the delay elements in the oscillator.

From the equation, the supply voltage variation affects only the driving current, and its effect can be easily minimized by generating the current with the supply independent current source. But, for the temperature compensation, both of the magnitude and derivative ratios between the driving current and the threshold voltage must be fixed to a desired value. In the proposed oscillator, we generate the two current sources which have the positive and negative slopes along the temperature change. By tuning the slopes of the currents independently and summing them, the desired current satisfying the two conditions can be obtained. The detailed implementation of the oscillator is shown in Fig. 3.4.

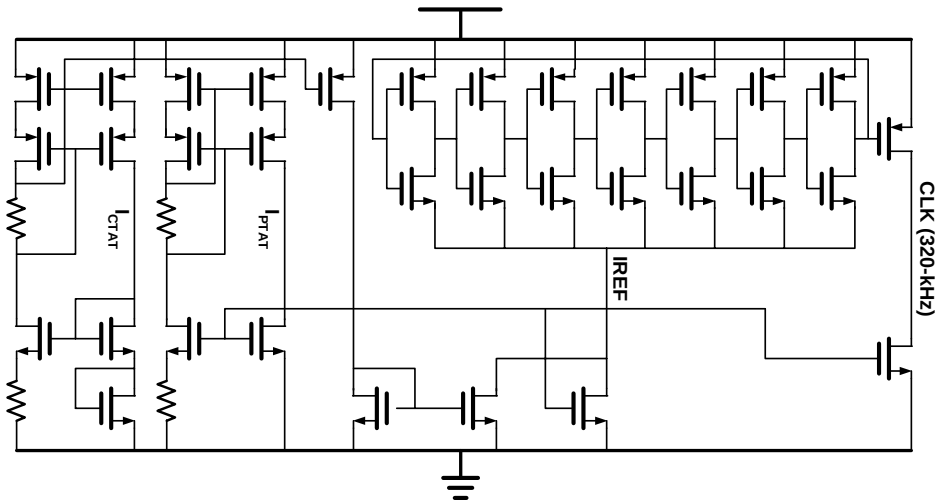


Figure 3.4. Implementation of the temperature compensated ring oscillator

The seven stage ring oscillator is driven by the reference current adjusted for the supply voltage and temperature compensations. The source terminals of PMOS devices are directly connected to power line to eliminate the threshold voltage modulation and enhance the power supply rejection ratio. In the two current sources, the low voltage cascode structure is utilized to reduce the effect of the supply voltage variation without the voltage headroom overhead [10].

The other important issue considered in the fully integrated clock generator is the synchronization. Since the clock generator independent of the input signal loses the correlation with the demodulated bit stream, the separate synchronizer should be incorporated. The oversampling synchronizer for the phase alignment is shown in Fig. 3.5. The synchronization process is initiated by detecting the manchester high violation in the preamble of the command packet. The preamble is selected as the same sequence specified in EPC RFID protocol for generation2 identity tag [11]. When the manchester high violation in the packet preamble is detected, the frequency divider is reset and the clock signal is killed. After that, the 320-kHz clock oversamples the incoming data to detect the following bit's half point. When the half point is detected, the frequency divider is set and clock signal is regenerated. At this moment, the clock starts to sample the input data's half width points which are most resistive

against noise, and the synchronization is completed.

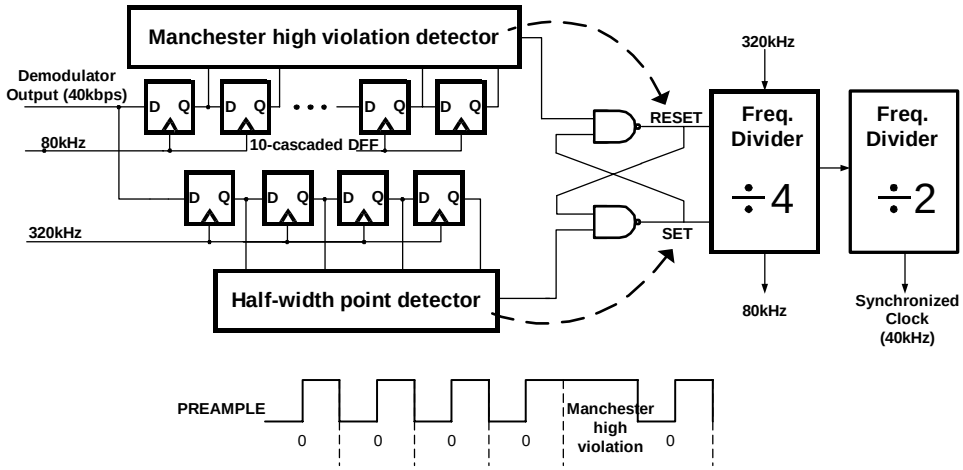


Figure 3.5. Oversampling synchronizer

3.4 128-bit ROM Block

Fig. 3.6. shows the ROM block to store 128-bit ID numbers. 128 bit block size is selected to store IPv6 address which is sufficient to assign unique ID number to all systems in the world without collision. The ID code can be used to identify the unique position of the sensor deployed in the measured area.

The area of the ROM block is reduced by using only NMOS

transistors. The regenerating PMOS can charge up each bit line to full supply voltage level and reduce leakage current caused by threshold voltage drop in NMOS.

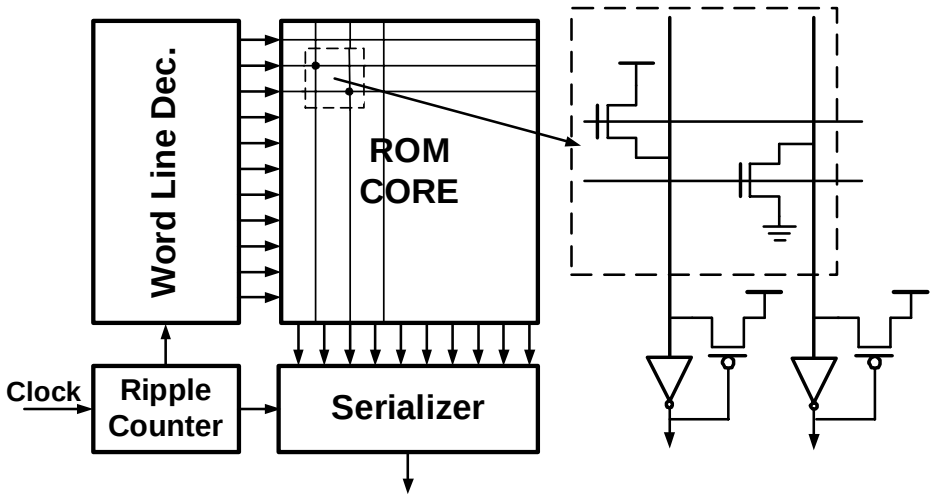


Figure 3.6. 128-bit ROM block with NMOS cell

3.5 Integrated Sensors

3.5.1 Temperature Sensor

The integrated temperature sensor has the low power structure shown in Fig. 3.7. The temperature information is represented by the base-emitter

voltage of the vertical pnp transistor. And the voltage signal which has the negative slope along the temperature change is converted to the digital code in the single slope ADC. The single slope ADC can be optimized to the power and area limited system because of its simplified structure and lower power consumption compared to other types of ADC. The poor conversion rate which is the critical drawback of the single slope ADC is not a limiting factor in the sensor since the highest frequency component of the ambient temperature is constrained to only a few Hz.

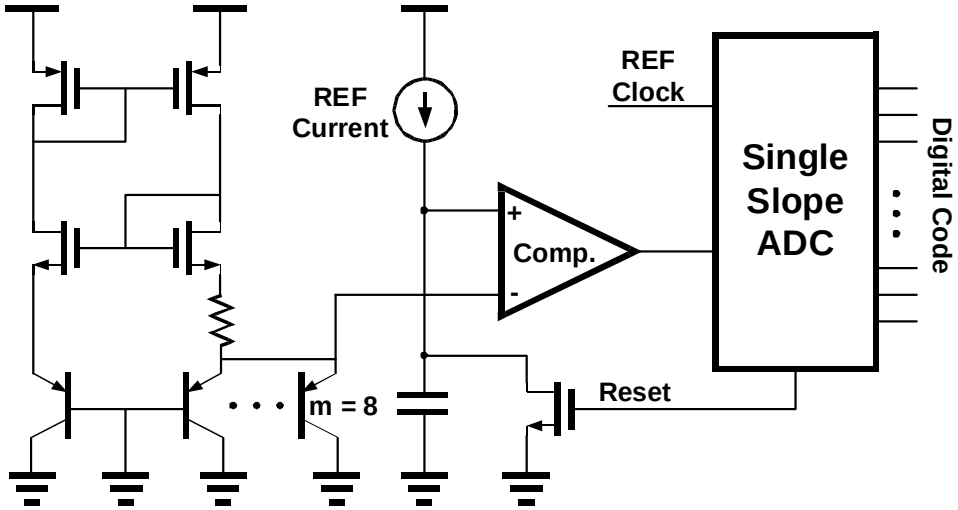


Figure 3.7. Integrated temperature sensor

In addition, the major reference signals such as the reference current and the clock are already considered in the clock generator and shared with this block. This sharing can save the power consumption of the sensor up to 20%.

3.5.2 Photo Sensor

The structure of the integrated photo sensor is presented in Fig.3.8. The operation of the photo sensor is very similar with that of the temperature sensor.

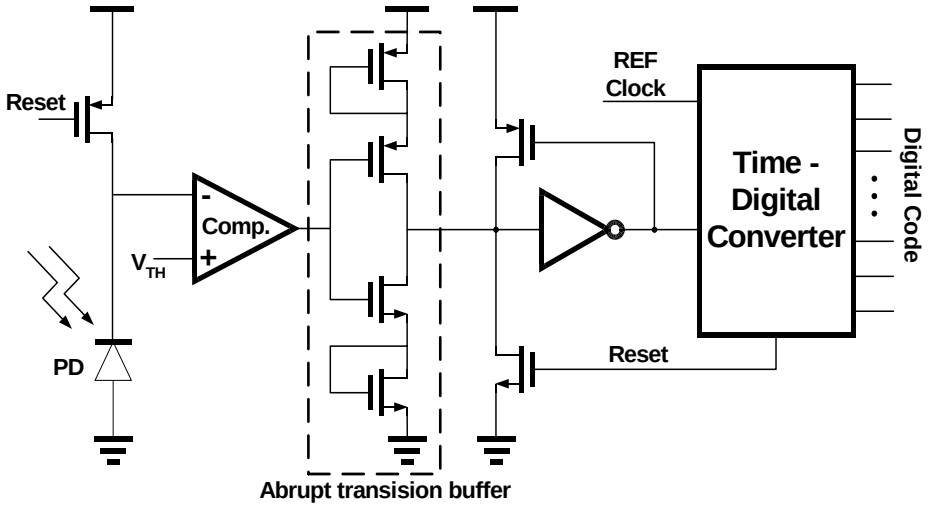


Figure 3.8. Integrated photo sensor

When the reset switch is turned off, the non-salicided pn junction which is utilized as the photo diode generates the current proportional to light intensity. Then, the photo current continues to accumulate negative charge on the inverting node of the comparator until the node voltage goes down to the threshold level. The charging time is transformed to digital code through the time to digital converter. In the sensor, the average amount of the photo current is in the order of pico amperes. This infinitesimal value slows down the rising time of the comparator significantly and causes a short circuit current issue to direct connection of the comparator and the CMOS logic gate. To solve the problem, we designed the interfacing buffer named as the abrupt transition buffer. The two diode-connected mosfets in the buffer can double the effective threshold voltage and generate more resistive path between the power and ground line during transition. Fig.3.9. shows the reduced short circuit current of the logic gate with the interfacing buffer.

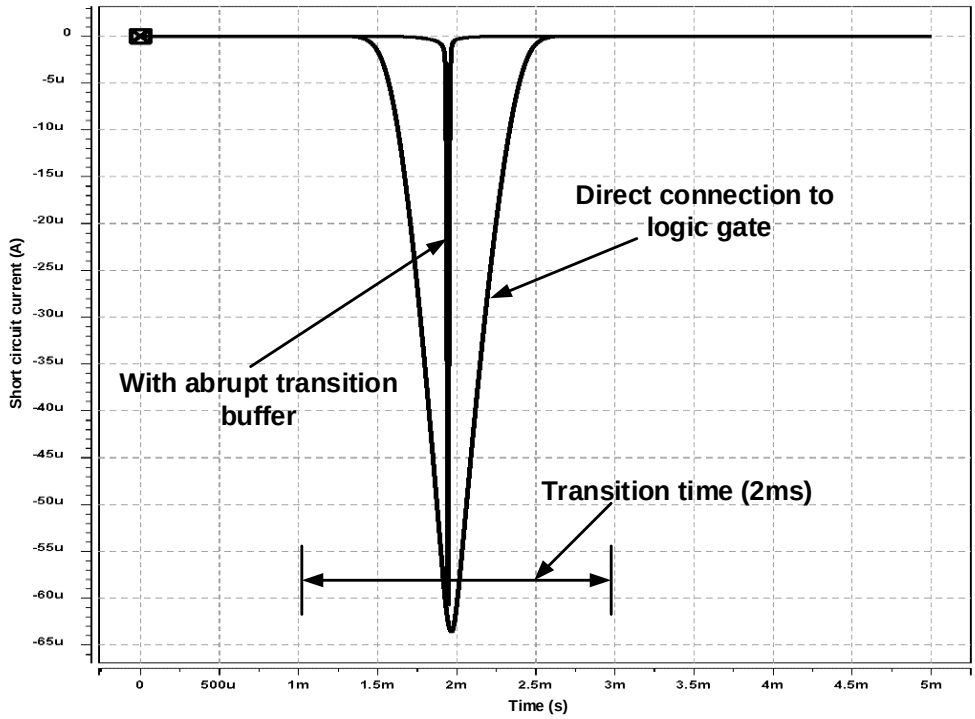


Figure 3.9. Short circuit current of the logic gate connected to the comparator

CHAPTER 4

EXPERIMENTAL RESULTS

4.1 Chip Microphotograph

Fig. 4.1. is the chip micro photograph of the RFID sensor IC. It is fabricated by 0.25-μm CMOS process supporting the schottky diode and the die area is 0.42-mm^2. The pads for connecting to antenna and testing are not shown in the photograph. The MOS capacitor filled in the empty area acts as not only decoupling capacitor but also energy-storage one. During active state, the transponder core dissipates only 5.1-μW at 1.5-V internal supply voltage. The clock generator consumes 1.2-μA and the integrated sensors consume only 0.8-μA at 1.5-V supply voltage.

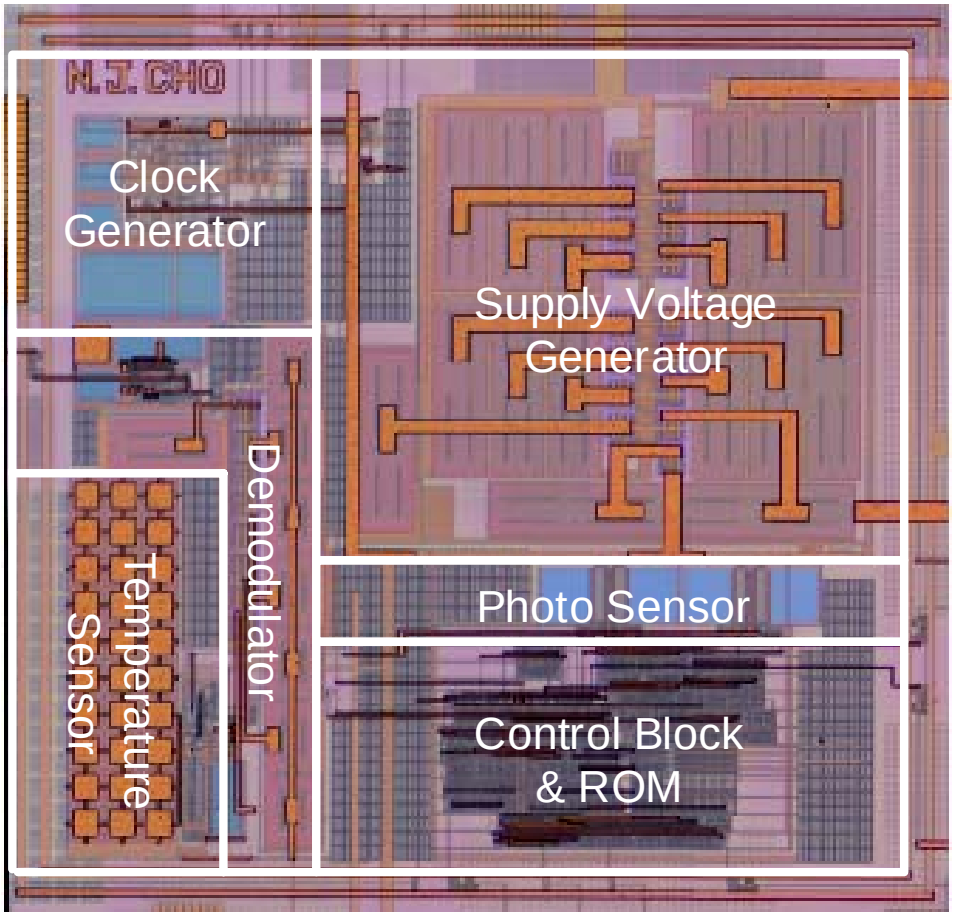


Figure 4.1. Micro photograph of the RFID sensor chip (0.6-mm x 0.7-mm)

4.2 Test Fixture

Fig. 4.2. is the photograph which shows the test board for measurement and the dipole antenna for RF interface. The several pins and the deep switch mounted on the board are just for testing.

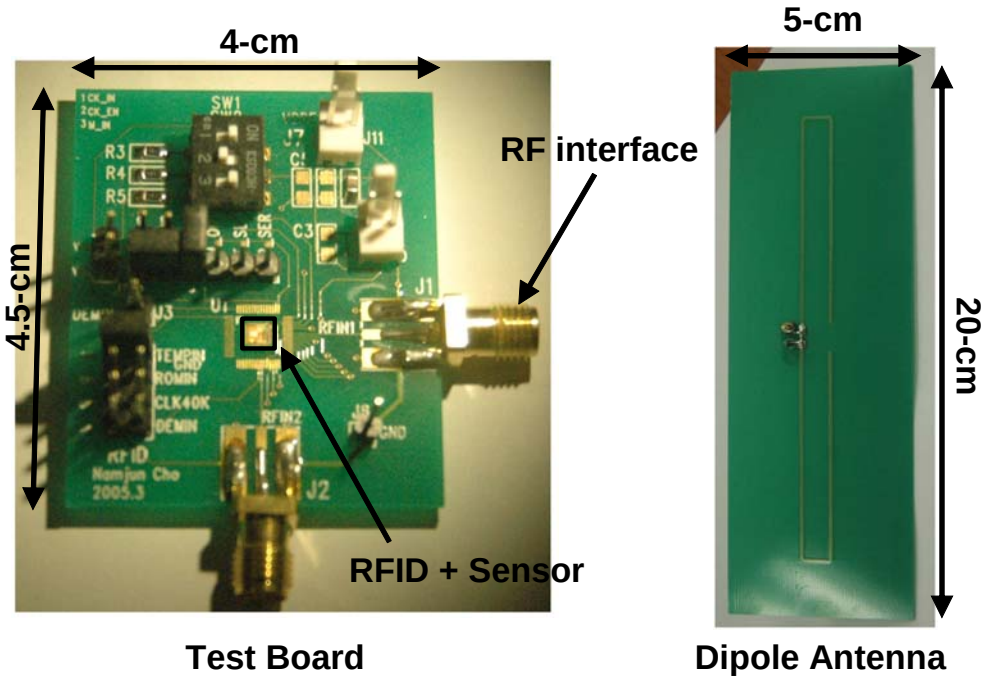


Figure 4.2. Test fixture

4.3 Measurement Results

Fig. 4.3. shows the operational distances of the transponder and the other RF-powered devices in the various power levels transmitted from base station. The measurement results show that even with the huge junction capacitance (≋280fF) of the schottky diode and the integration of the additional sensors, the operational distance comparable to the commercial RFID tags is achieved in this work.

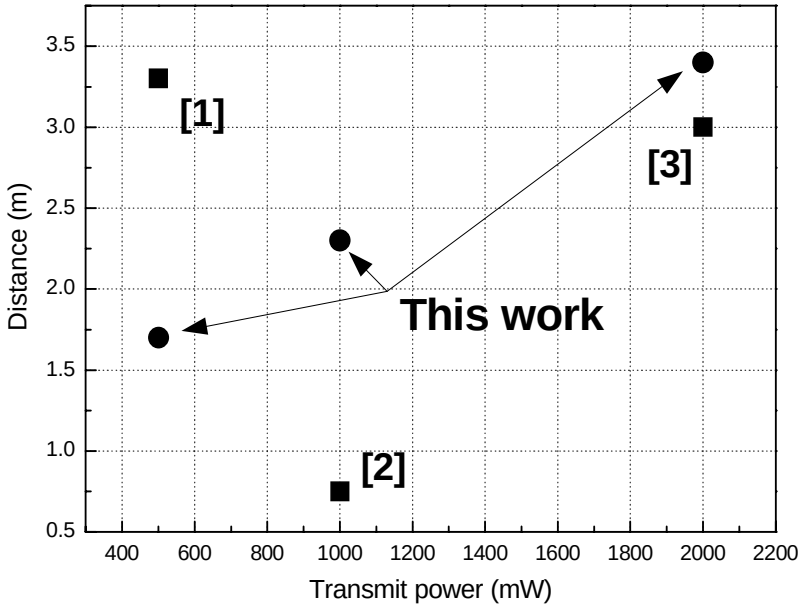


Figure 4.3. Operational distances of the transponder in various transmit power

Fig. 4.4. shows the operational sequence of the transponder. When the manchester high violation in the preamble is detected, the synchronization between the clock and data is achieved. The command following the preamble is translated by the decoder and the requested data are transmitted from the block selected among the ROM and the two integrated sensors. The third waveform shows the bit stream coming out from the internal ROM which has the ID number of the transponder.

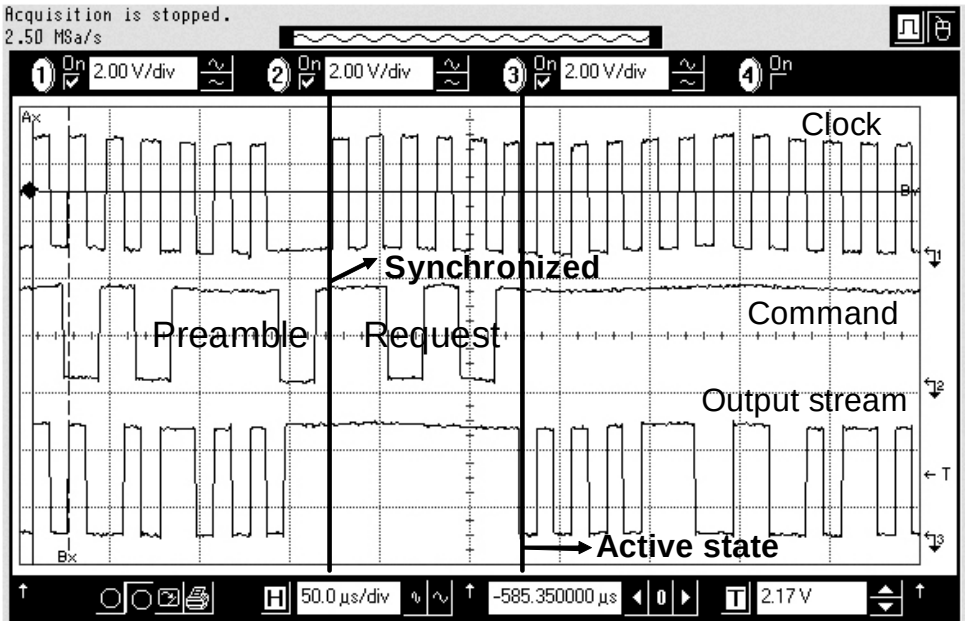


Figure 4.4. Operational sequence of the transponder

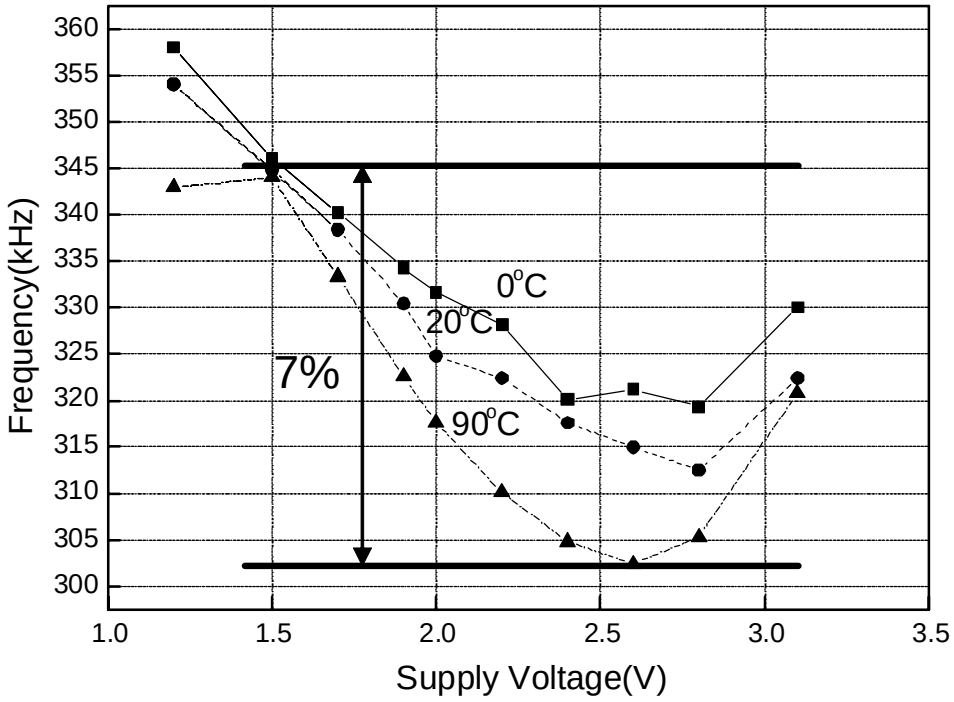
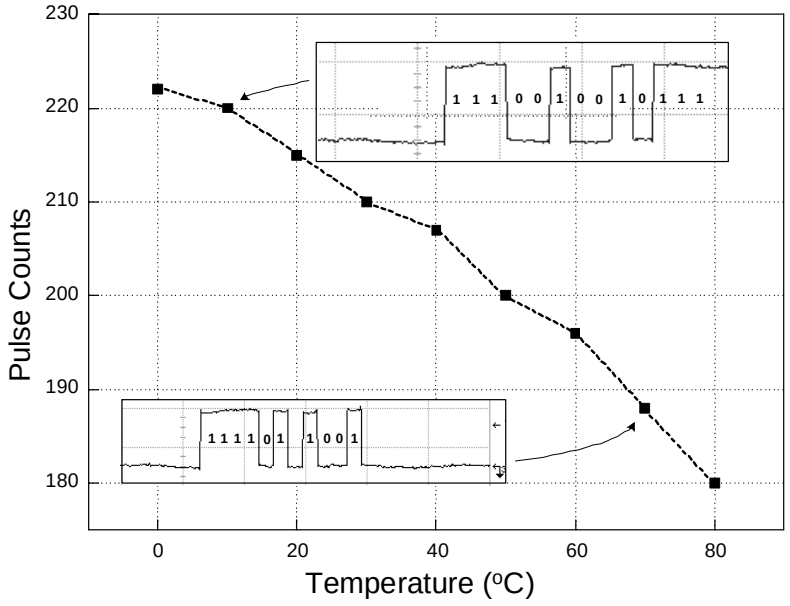


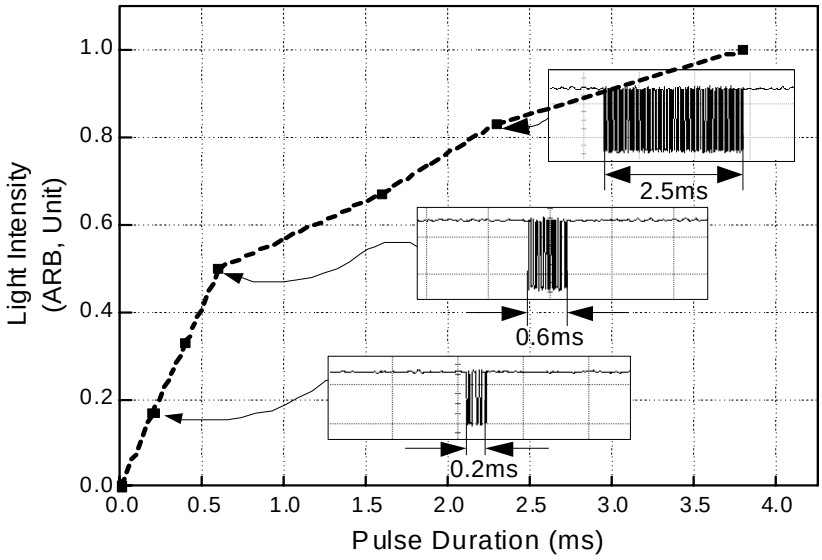
Figure 4.5. Frequency variation of the proposed oscillator

The performance of the proposed oscillator is shown in Fig 4.5. The graph shows the variation of the output frequency is within 7% in the 1.5-V supply voltage variation and the 90° degree temperature change. The minimum supply voltage for the safe operation of the clock generator is 1.0-V. Without the low voltage cascade structure in the oscillator, it's hard to generate the stable clock signal under 1.3-V supply voltage.

Fig. 4.6. shows the measurement results of the integrated sensors. The measurement of the temperature sensor is done in the range from 0-^{o}C to 80^{o}C and the results are plotted in Fig. 4.6.(a). Its effective resolution is 2-^{o}C and the maximum error from the ideal value is within 4^{o}C. The graph in Fig. 4.6.(b) presents the output pulse duration of the photo sensor according to the relative intensities of the light emitting device. Under the 0.5 ARB of the light intensity, there is the abrupt degradation in the resolution of the sensor. This non linearity is caused by the poor dynamic range of the simple PN diode - non salicided NMOS source junction. More performance improvement will be obtained if the photo diode process is optimized.



(a)



(b)

Figure 4.6. (a) Output code of the temperature sensor

(b) Output pulse duration of the photo sensor

CHAPTER 5

CONCLUSIONS

5.1 Conclusions

This work presents a RF powered transponder with temperature sensor and photo sensor for environmental monitoring. The architecture optimized for the operation in the UHF band has the temperature compensated oscillator and the oversampling synchronizer. Both of the integrated sensors share the major reference signals with the clock generator and adopt the single slope ADC which has the reduced complexity and the lower power consumption. The designed transponder can operate up to 3.4-m from the base station. The frequency variation of the proposed oscillator is less than 7% from the nominal frequency under 1.5-V supply voltage sweep and 90-^{o}C temperature change. The IC is fabricated in 0.25-μm CMOS process. The die area is 0.6- mm x 0.7-mm excluding pads. Total power consumption of the operating blocks is only 5.14-μW during active state.

SUMMARY

무선 인식 기술(RFID)은 최근 들어 그 응용 분야를 넓혀가고 있으며, 인식 거리의 증대를 바탕으로 다수의 무선 인식 장치들 간에 Network을 형성하여, 이를 Home network, Health care, Wireless sensor network 등에 이용하려는 시도들이 진행되고 있다.

본 논문은 기존의 RFID 태그 칩에 온도 센서와 광 센서를 집적시켜, 무선 인식 기술을 주변 환경 감지에 사용할 수 있는 시스템을 제안하였다.

제안된 시스템은 배터리가 없이, 외부로부터 무선으로 AC power를 받고 이를 DC 전원 전압으로 만들어 사용한다. 사용된 전원 전압 발생기는 8-stage dickson voltage multiplier 구조의 charge pump이고, pumping 효율을 증대시키기 위해, schottky diode를 사용했다.

Base station과의 통신방식은 ASK modulation을 채택하였으며, demodulator의 면적 소모를 최소화하기 위하여, 저항 대신 다이오드 type으로 연결된 NMOS pair를 사용하였다.

시스템의 전력 소모를 최소화하기 위하여, 전원 전압과 온도 변화에 의해 영향 받지 않는 Oscillator와 Oversampling synchronizer를 고안하였고, 집적된 센서로 인한 시스템 부하를 줄이기 위해 reference signal들을 clock 발생기와 공유 시켰으며, 간단한 구조를 취하면서도 정밀도 가 높은single slope ADC를 적용하였다.

구현된 시스템의 인식 거리는 base station으로부터 최대 3.4-m 이며, 최소 입력 전력은 0.95-dBm이다. 제안된 oscillator의 출력 주파수는 1.5-V 전원 전압 변동이나 80-^{o}C 온도 변화 하에서도 7-% 이내로 안정화되었다.

시스템은 0.25-μm CMOS 공정을 사용해 설계되었고, 전원 전압 발생기를 위

해 schotty diode 공정을 따로 추가하였다. 전체 전력 소모는 1.5-V 전원 전압 하에서 5.14-μW이고, Pad를 제외한 칩 면적은 0.42-mm^2 이다.

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