Design of Low Power Digital Hearing Aid Chip

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Outline

• Introduction
• Design of Digital Hearing Aid
  – Specifications
  – Building Blocks
• Simulation Results
• Conclusion and Further Work
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• Design of Digital Hearing Aid
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  – Building Blocks
• Simulation Results
• Conclusion and Further Work
Motivation

• Hearing Problem is Serious!
  – 10% of population have difficulties in hearing.
Design Considerations

- Programmability
- Low Power (<500\mu W)
- Small Size (One-chip)
- Low Power Digital Hearing Aid!
## Previous Work

<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td><strong>Power Consumption</strong></td>
<td>2.1mW</td>
<td>2.1mW</td>
<td>400μW @ no signal</td>
</tr>
<tr>
<td><strong>Bandwidth</strong></td>
<td>8kHz</td>
<td>8kHz</td>
<td>10kHz</td>
</tr>
<tr>
<td><strong>Number of Channels</strong></td>
<td>-</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td><strong>Total Harmonic Distortion</strong></td>
<td>-</td>
<td>-45dB</td>
<td>-40dB</td>
</tr>
<tr>
<td><strong>Process</strong></td>
<td>3μm CMOS</td>
<td>0.8μm CMOS</td>
<td>0.6μm CMOS</td>
</tr>
<tr>
<td><strong>Area</strong></td>
<td>35mm$^2$</td>
<td>35mm$^2$</td>
<td>12mm$^2$</td>
</tr>
<tr>
<td><strong>Misc.</strong></td>
<td>4-chips, 10 external passive elements, EEPROM</td>
<td>IR remote control receiver, Telecoil</td>
<td>EEPROM</td>
</tr>
</tbody>
</table>
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• Simulation Results

• Conclusion and Further Work
Specifications

• Power < 500uW
  – Battery lasts for 1 week at least. (16hr/day use)

• Supply Voltage = 1V

[Diagram showing EMF values and lifetime for Zinc-Air Battery]
Specifications (Cont’d)

• Programmable 2 Channel DSP
  – Compensation for ‘ski-slope’ loss

![Gain vs Frequency Graph]

• Acceptable Sound Quality
  – 12-bit Resolution

@ 16kHz Sampling Frequency
Specifications (Cont’d)

• Bandwidth
  – 8kHz

• Total Processing Time < 5ms
  – To avoid confusion with lip-reading
Overall Architectures

[Digital Hearing Aid System]
Preamplifier

- Microphone Specification
  - Differential Output Gain 4.43V/V up to 100dB input
  - For A/D Converter Differential Input 140mV

<table>
<thead>
<tr>
<th>Input [dB SPL]</th>
<th>Output [mV]</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>30~40</td>
<td>0.01 ~ 0.03</td>
<td>Ambient room noise/ Whisper</td>
</tr>
<tr>
<td>50~70</td>
<td>0.1 ~ 1</td>
<td>Conversation</td>
</tr>
<tr>
<td>80~90</td>
<td>3.16 ~ 10</td>
<td>Feature film in theater</td>
</tr>
<tr>
<td>90~110</td>
<td>10 ~ 31.6 (@ 100dB)</td>
<td>Bar with music</td>
</tr>
<tr>
<td>110 ~ 120</td>
<td>100 ~</td>
<td>Rock concert</td>
</tr>
<tr>
<td>130 ~ 140</td>
<td></td>
<td>Painful sound</td>
</tr>
</tbody>
</table>

※ Spec. for Knowles Inc. EM series Microphone
Preamplifier (Cont’d)

- **Opamp. with MOS Resistive Circuit (MRC)**
  - Small Area
  - Ease of Tunability for Future AGC

\[
\begin{align*}
V_{G1} & \quad V_{G2} \\
V'_{G1} & \quad V'_{G2} \\
V_i & \quad V_o
\end{align*}
\]

\[
V_1 \quad V_2 \quad V_3 \quad V_4
\]

\[
R_{MRC} = \frac{1}{K_P \frac{W}{L} (V_{G1} - V_{G2})}
\]
Preamplifier

- THD = -70dB @ 1kHz, 1mV input
- THD = -52dB @ 10mV input
- $\text{Power}_{\text{MAX}} = 35\mu\text{W}$
Analog-to-Digital Converter

- Oversampling A/D Converter
  - 12-bit Resolution A/D Converter
    - SNR > 72dB
  - 1-bit 2nd Order Modulator with 64 Oversampling Ratio ($f_s/2f_0$)
ADC Modulator

Frequency Spectrum for 1kHz 26mV Input

- **SNR**: 72dB (@ 1kHz)
- **Power**: 89uW (Modulator: 82uW, Decimator: 7uW)
Digital Signal Processor

- **Specifications**
  - 2 Channel
    - Compensation for Ski-slope Loss
  - 6 Programmable Parameters
    - P, G0, K, G1, G2, VC
  - Serial Interface & Parameter ROM
Parameter ROM

- **Word Line Decoder**
- **ROM Core**
- **Column Buffer**
- **ROM Select (ROM_SEL)**
- **Ripple Counter**

### Table

<table>
<thead>
<tr>
<th>P</th>
<th>K</th>
<th>G0</th>
<th>G1</th>
<th>G2</th>
<th>VC</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>0000000100000000</td>
<td>1101</td>
<td>0110</td>
<td>0001</td>
<td>1000</td>
</tr>
</tbody>
</table>

- **WL1**
- **BL0**
- **BL1**

### Circuit Diagram

- **ROM Cell**
- **Column Buffer**
DSP Frequency Response

- **P = 3, G0 = 1/64**
- **G1 = 32**
- **G2 = 8**
  - **VC = 1**

- **P0 = 1/64, G1 = 32**
- **P1 = 3, G0 = 1/64**
  - **G1 = 32**
  - **G2 = 8**

- **G0**
  - **P = 3, G0 = 1/64**
    - **G1 = 32**
    - **G2 = 8**

- **G0, G1, G2**
  - **G0 = 1/64**
  - **G1 = 32**
  - **G2 = 8**

Graphs showing frequency response for different settings.
Digital-to-Analog Converter

- Oversampling D/A Converter
  - 12-bit Resolution D/A Converter
    - SNR > 72dB
  - 1-bit 2\textsuperscript{nd} Order Modulator with 128 OSR
Filter Coefficient Optimization

Filter Coeff. “31”

2’s Comp. CSD

0 1 1 1 1 1
# of P.P. = 5
# of INV = 0

1 0 0 0 0 1
# of P.P. = 2
# of INV = 1

WINNER

Filter Coeff. “3”

2’s Comp. CSD

0 1 1
# of P.P. = 2
# of INV = 0

1 0 1
# of P.P. = 2
# of INV = 1

WINNER

CSD Not Always Superior to 2’s Comp.
Decision Algorithm

Filter Coeff. Representation

- 2’s Comp.
- CSD

Comparison
1. Less P.P. (Adder)
2. Less Inverter

Sharing
Same Coeff.

19% Power Reduction Compared to CSD
(28% to 2’s Comp.)
DAC

- **SNR:** 80dB @1kHz
- **Power:** 65uW

Frequency Spectrum for 1kHz 26mV Input
Receiver Driver

- **H-Bridge**
  - High Efficiency
  - Low Power Dissipation
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Total Simulation Results

- SNR: 70dB @ 1kHz
- THD: -45dB
Total Simulation Results (Cont’d)

Output Amplitude (dB) vs. Frequency (Hz)

-14, -11, -2, -17 dB

Vin = 1mV  \( (P=3, \ G_0=\frac{1}{2}, \ G_1=32, \ G_2=8, \ V_C=1, \ K=1) \)
Total Processing Time

Input (4kHz)

Output

860usec (< 5msec)
Power Consumption

<table>
<thead>
<tr>
<th>Blocks</th>
<th>Power (uW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preamplifier</td>
<td>35</td>
</tr>
<tr>
<td>ADC</td>
<td>89</td>
</tr>
<tr>
<td>DSP</td>
<td>11</td>
</tr>
<tr>
<td>DAC</td>
<td>65</td>
</tr>
<tr>
<td>H-Bridge</td>
<td>40</td>
</tr>
<tr>
<td>Ring Oscillator</td>
<td>35</td>
</tr>
<tr>
<td>Total</td>
<td>275uW</td>
</tr>
</tbody>
</table>

Total Power: 275uW

Power Dissipation

- Ring Osc. 12.73%
- Preamp 12.73%
- H-Bridge 14.55%
- DAC 23.64%
- DSP 4.00%
- ADC 32.36%
Power Comparison

Power (uW)

Centre Swiss  Philips  TI  This Work

0  500  1000  1500  2000  2500

Philips and Centre Swiss have significantly higher power consumption compared to TI and This Work.
Summary of Performance

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd</td>
<td>1V</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>275uW</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>8kHz</td>
</tr>
<tr>
<td>Number of Channels</td>
<td>2</td>
</tr>
<tr>
<td>Maximum Input Signal</td>
<td>~30mV</td>
</tr>
<tr>
<td>SNR A/D (@1kHz)</td>
<td>72dB</td>
</tr>
<tr>
<td>SNR D/A (@1kHz)</td>
<td>80dB</td>
</tr>
<tr>
<td>SNR Audio Path (@1kHz)</td>
<td>70dB</td>
</tr>
<tr>
<td>THD Audio Path (@1kHz, 23mV input)</td>
<td>-45dB</td>
</tr>
<tr>
<td>Temperature Range</td>
<td>0-100 ℃</td>
</tr>
<tr>
<td>Low Threshold 0.18um CMOS Process</td>
<td></td>
</tr>
</tbody>
</table>

![Diagram of semiconductor system](image)
Outline

• Target
• Building Blocks
• Simulation Results
• Conclusion and Further Work
Conclusion

• A 1V 275uW Digital Hearing Aid Chip is Designed.
  – Preamplifier with MRC
    • THD = -70dB @ 1kHz, 1mV input
  – 1-bit 2\textsuperscript{nd} Order ADC
    • OSR=64, SNR=72dB
  – Programmable 2 channel DSP
    • 6 Programmable Parameters
    • Serial Interface & Parameter ROM
  – 1-bit 2\textsuperscript{nd} Order DAC
    • OSR=128, SNR=80dB
    • Coefficient Optimization of Interpolation Filter
  – H-Bridge
Further Work

• Implementation
• Quality Improvement
• H-Earphone (Healthy Earphone)
  – Hearing aid with additional function
    • Noise cancellation, etc…
Supplementary
Delta-Sigma Modulator

1st integrator

2nd integrator

Comparator (1-bit ADC)

1-bit DAC
Decimation Filter

\[ H(z) = \prod_{i=0}^{4} (1 + z^{-2^i})^3 \]
Block Diagram

- Serial Interface
- Coefficient ROM
- Digital Signal Processor
  - FIR Band Split Filter
  - High-Band Channel
  - Low-Band Channel
  - Volume Control

- Input signals:
  - ROM_SEL, LE, DATA, CK
  - DSP_IN [15:0]
  - CK (32kHz)

- Output signals:
  - DSP_OUT [15:0]
Two-Band DSP Algorithm

Diagram:
- DSP Input
- Band Split Filter
- K
- G0
- G1
- G2
- DSP Output
- VC
- P
Serial Interface

P[0:1] → 2-Bit Register → LE

K[0:15] → 16-Bit Register → LE

G₀[0:3] → 4-Bit Register → LE

G₁[0:3] → 4-Bit Register → LE

G₂[0:3] → 4-Bit Register → LE

VC[0:3] → 4-Bit Register → LE

DATA → 16-Bit Shift Register → LE

CK → 4-Bit Shift Register → LE

2-Bit Register

4-Bit Register

16-Bit Register

4-Bit Register

4-Bit Register

4-Bit Register

4-Bit Register
## DSP Performance Summary

<table>
<thead>
<tr>
<th>I/O Type</th>
<th>2’s Complement 16-bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Frequency</td>
<td>32 kHz</td>
</tr>
<tr>
<td>Channel</td>
<td>2</td>
</tr>
<tr>
<td>Filter Type</td>
<td>FIR Filter</td>
</tr>
</tbody>
</table>

### Programmable Coefficients

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Band Split (P)</td>
<td>2-bit</td>
</tr>
<tr>
<td>High-Band Knee Point (K)</td>
<td>16-bit</td>
</tr>
<tr>
<td>Low-Band Gain (G₀)</td>
<td>4-bit</td>
</tr>
<tr>
<td>High-Band Low-Level Gain (G₁)</td>
<td>4-bit</td>
</tr>
<tr>
<td>High-Band Compression Ratio (G₂)</td>
<td>4-bit</td>
</tr>
<tr>
<td>Volume Control (VC)</td>
<td>4-bit</td>
</tr>
</tbody>
</table>

### Power Dissipation

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>DSP</td>
<td>10 μW</td>
</tr>
<tr>
<td>Serial Interface</td>
<td>1 μW</td>
</tr>
<tr>
<td>Active Area</td>
<td>0.3 x 0.3 mm²</td>
</tr>
</tbody>
</table>
Multiplication with Adders & Shifters

- 2’s Complement vs. Canonical Signed Digit (CSD)

<table>
<thead>
<tr>
<th>Integer</th>
<th>2’s Complement</th>
<th>CSD</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>011</td>
<td>101</td>
</tr>
</tbody>
</table>

Implementation of ‘X * 3’ using (a) 2’s Complement (b) CSD
Ring Oscillator

- **CLK**
  - 2.048MHz, 1.024MHz, 512kHz, 256kHz, 128kHz, 64kHz, 32kHz