

$$\frac{(x-d)^2}{a^2} + \frac{y^2}{b^2} = 1 \quad (5)$$

In polar co-ordinates, and after some simple manipulation, eqn. 5 can be written as

$$r^2 \left(\frac{\cos^2(\varphi)}{a^2} + \frac{\sin^2(\varphi)}{b^2} \right) - r \left(\frac{2d \cos(\varphi)}{a^2} \right) + \frac{d^2}{a^2} - 1 = 0 \quad (6)$$

The above equation is, as expected, a quadratic polynomial, since for each angle φ (within the range $0 < \varphi < \varphi_{max}$) there are two radii, $r_1 = |OD|$ and $r_2 = |OC|$. Solving eqn. 6 with respect to r :

$$r_{1,2}(\varphi) = \frac{b^2 d \cos(\varphi) \mp \sqrt{b^4 d^2 \cos^2(\varphi) - [a^2 b^4 \cos^2(\varphi) + a^4 b^2 \sin^2(\varphi)] \left(\frac{d^2}{a^2} - 1 \right)}}{b^2 \cos^2(\varphi) + a^2 \sin^2(\varphi)} \quad (7)$$

In the numerator of eqn. 7, the minus sign corresponds to $r_1(\varphi)$ and the plus to $r_2(\varphi)$. An area bounded by a function $r_1(\varphi)$ and $r_2(\varphi)$ in polar co-ordinates is given by

$$A(\varphi) = \frac{1}{2} \int_0^\varphi [r_2^2(\zeta) - r_1^2(\zeta)] d\zeta \quad (8)$$

Inserting eqn. 7 into eqn. 8 and the result into eqn. 4, the CDF of the AoA is given by the following integral:

$$F_\varphi(\varphi) = \int_0^\varphi \frac{4b^2 d \cos(\zeta) \sqrt{b^4 d^2 \cos^2(\zeta) - (a^2 b^4 \cos^2(\zeta) + a^4 b^2 \sin^2(\zeta)) \left(\frac{d^2}{a^2} - 1 \right)}}{ab\pi (b^2 \cos^2(\zeta) + a^2 \sin^2(\zeta))^2} d\zeta \quad (9)$$

From eqn. 9, and with $F = a/d$ and $E = b/a$, the PDF of φ can be calculated as

$$f_\varphi(\varphi) = \begin{cases} \frac{1}{\Omega} \frac{\cos(\varphi) \sqrt{\cos^2(\varphi) - (\cos^2(\varphi) + E^{-2} \sin^2(\varphi))(1-F^2)}}{(E^2 \cos^2(\varphi) + \sin^2(\varphi))^2} & \text{for } -\varphi_{max} < \varphi < \varphi_{max} \\ 0 & \text{elsewhere} \end{cases} \quad (10)$$

where Ω can be calculated from $\int_{-\varphi_{max}}^{\varphi_{max}} f_\varphi(\varphi) d\varphi = 1$, ($1/\Omega = 2b^3 d^2 / (a^2 \pi)$). Since the PDF of the AoA is an even function, it has been extended in eqn. 10 to the whole angular range by simply dividing the constant $1/\Omega$ by 2.

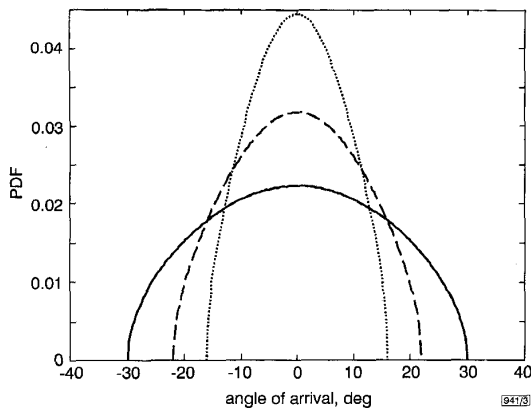


Fig. 3 PDF examples of AoA for circular and elliptical ($E = 0.5$ and $E = 0.7$) cases with $F = 0.5$

- circular cluster $F = R/d = 0.5$
- - - elliptical cluster $E = 0.7, F = 0.5$
- elliptical cluster $E = 0.5, F = 0.5$

In the case of a circle, eqn. 10 reduces to the following equation:

$$f_\varphi(\varphi) = \begin{cases} \frac{1}{\Omega} \cos(\varphi) \sqrt{\cos^2(\varphi) + F^2 - 1} & \text{for } -\phi_{c,max} < \varphi < \phi_{c,max} \\ 0 & \text{elsewhere} \end{cases} \quad (11)$$

Fig. 3 shows examples for the PDF of the angle of arrival when a circular scattering cluster ($F = 0.5$), and elliptical clusters ($E = 0.7$, $E = 0.5$), are considered.

Acknowledgment: The authors wish to thank the Fujitsu Europe Telecom R&D Centre Ltd. for sponsoring the work presented in this Letter.

© IEE 1998

31 July 1998

Electronics Letters Online No: 19981264

R.J. Piechocki, G.V. Tsoulos and J.P. McGeehan (*Centre for Communications Research, University of Bristol, Merchant Venturers Building, Bristol BS8 1UB, United Kingdom*)

References

- 1 LEE, W.C.Y.: 'Effects on correlation between two mobile radio base-station antennas', *IEEE Trans. Commun.*, 1973, **COM-11**, pp. 1214-1224
- 2 FUHL, J., MOLISCH, A., and BONEK, E.: 'Unified channel model for mobile radio systems with smart antennas', *IEE Proc., Radar Sonar Navig.*, 1998, **145**, (1), pp. 32-41
- 3 PETRUS, P., REED, J., and RAPPAPORT, T.: 'Geometrically based statistical model for mobile communications'. *IEEE Proc. Global Communications Conf. 1996 (Globecom'96)*, pp. 1197-1201
- 4 SWALES, S.: 'Spectrum efficient cellular base-station antenna architectures'. PhD Thesis, University of Bristol, UK, November 1990
- 5 LIBERTI, J.C., and RAPPAPORT, T.S.: 'A geometrically based model for line-of-sight multipath radio channels'. *IEEE Veh. Technol. Conf. (VTC)*, 1996, pp. 844-848

Boosted charge transfer preamplifier for low power Gbit-scale DRAM

Jong-Shik Kim, Hoi-Jun Yoo and Kwang-Seok Seo

A new charge transfer preamplifier scheme is developed for low power and high density DRAMs. It employs a boosting method with a MOSFET capacitor for a high voltage precharge level and a pulse control signal for a charge transfer switch. The new scheme increases the sensing margin and enhances the sensing speed under 1.5V operation with a small area overhead. It also leads to a wider design window for a charge transfer switch as the supply voltage scales down.

Introduction: The power supply voltage for Gbit-scale DRAMs is being scaled down to $< 1.5V$ [1]. To maintain the circuit speed even at low supply voltage, new circuit architectures for high-speed operation, especially in bit-line sensing, have to be developed [2]. A charge transfer preamplifier (CTP) scheme has been proposed to improve bit line sensing [3, 4]. It can increase the sensing margin and the sensing speed, by utilising the charge transfer from a small sense amplifier (SA) capacitor to a large bit line (BL) capacitor. For successful sensing operation, a CTP must satisfy two requirements: dual precharge voltage levels and tight control of the charge transfer. The former is used to deliver the charge from the SA-capacitor to BL-capacitor, and the latter to maintain the difference between the SA voltage level and BL voltage level after the charge transfer. These prerequisites cause inherent problems in the CTP scheme such as large SA area overhead, large cell array current and difficulty in the control of the charge transfer switch, which may hinder its application to the high density DRAMs.

In this Letter, we propose the boosted charge transfer preamplifier (BCTP) scheme that has small SA area overhead, small cell array current, and greater freedom in the control of charge transfer. These features are achieved by employing a boosting method with a MOSFET capacitor and a pulse control signal for the charge transfer switch. The SPICE simulation results prove that the BCTP scheme has a greater sensing margin and higher sensing speed than does the CTP scheme.

Operation: Fig. 1a shows the circuit schematic diagrams of the BCTP scheme and its control signal waveforms. The circuit structure is similar to that of the cross-coupled SA architecture, but for a boosting MOSFET capacitor in the SA array. The proposed scheme has three new features. The first is the employment of a voltage boosting method with a single precharge circuit to reduce the area overhead of dual precharge circuits. To obtain dual precharge levels, the SA array is precharged to a voltage equal to that of the BL array, and then boosted via a boosting capacitor. With this method, the BCTP can remove the additional cell array current required in the conventional dual precharge scheme. Secondly, a MOSFET capacitor (C_{SA}) is used as a boosting capacitor.

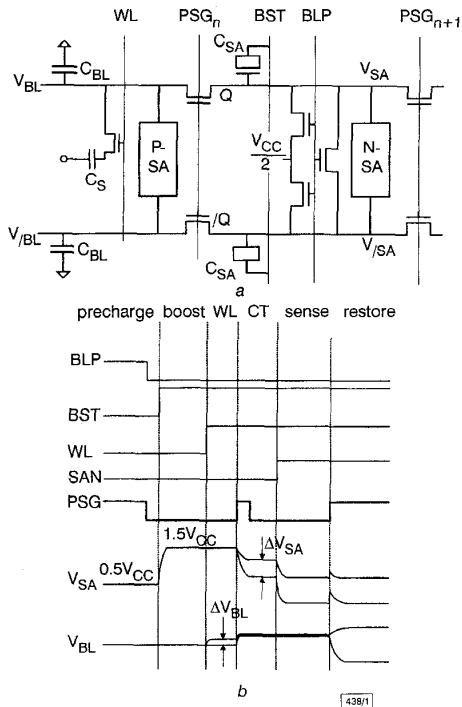


Fig. 1 Schematic diagrams of boosted charge transfer preamplifier architecture

a Circuits
b Voltage waveforms

Owing to the nonlinear C-V characteristics of the MOSFET capacitor, C_{SA} has a large capacitance during the precharge period, and becomes small after the charge transfer action. Large C_{SA} during the precharge period leads to a large stored charge, and small C_{SA} during the sensing period lead to an increase in the sensing margin. The third is to use a pulse control signal in order to make control of the charge transfer easier. The BCTP scheme has three design parameters for charge transfer; the channel length, the channel width of the MOSFET as the charge transfer switch (Q) and the pulse time width of the control signal for the Qs, where the only parameter in the CTP scheme is the DC voltage level.

Initially, both the BL and SA array are precharged to half- V_{CC} level by turning on the Qs. At this precharge step, C_{SA} has a large inversion capacitance. After the Qs are turned off, the boosting signal (BST) rises from ground to V_{CC} to raise the SA-node voltages (V_{SA} and V_{ISA}) up to $1.5 \times V_{CC}$. The charge shared signal (ΔV_{BL}) is developed at BL and /BL when a selected word line (WL) connects a cell to BL. The charge transfer period then begins. The control signal for the Qs (PSG) activates and maintains its level for time τ , to transfer the charge stored in C_{SA} to the bit-line capacitor (C_{BL}). The transferred amount of charge can be controlled with the channel length, the width of Qs and the τ of PSG. As the charge is transferred, V_{SA} and V_{ISA} decrease and a large voltage difference (ΔV_{SA}) is produced between SA and /SA, compared with ΔV_{BL} . Since the voltage difference between the gate and the junction of C_{SA} becomes reduced during the charge transfer, C_{SA} develops a small depletion capacitance, leading to an

increase in ΔV_{SA} . The sense amplifier senses ΔV_{SA} when the Qs are turned off. Sensing speed is increased because BL is isolated from SA. The restoring operation starts by turning on the Qs again with the activating pull-up sense amplifier (p-SA).

The sensing margin at the SA-node can be expressed as eqn. 1

$$\Delta V_{SA} = (I_{SA} - I_{/SA}) \times \tau \times 1/C_{SA} \quad (1)$$

where τ is the pulsewidth of the PSG, and I_{SA} and $I_{/SA}$ are the current through Q and /Q, respectively. For the maximum ΔV_{SA} , a large value of $I_{SA} - I_{/SA}$ and small C_{SA} are needed. To satisfy these requirements, V_{SA} during the sensing period should be between $V_{CC} - V_T$ and $V_{CC} + V_T$. The upper limit, $V_{CC} + V_T$, represents the condition in which the MOSFET capacitor is in the depletion mode. When $V_{SA} \leq V_{CC} + V_T$, C_{SA} has a small depletion capacitance resulting in large ΔV_{SA} . The lower limit, $V_{CC} - V_T$, represents the condition in which the Qs operate in saturation. When $V_{SA} \geq V_{CC} - V_T$, the Qs can drive more current because of their operation in the saturation mode, increasing $I_{SA} - I_{/SA}$ or ΔV_{SA} . With the aforementioned conditions for ΔV_{SA} and an assumption that Qs are in the saturation mode, the optimum design window for the Qs can be expressed as

$$\frac{V_{CC} - V_T}{(V_{CC}/2 - V_T + \Delta V_{BL})^2} \leq \delta \leq \frac{V_{CC} + V_T}{(V_{CC}/2 - V_T + \Delta V_{BL})^2} \quad (2)$$

where δ is a new design parameter which has the three design factors of the channel length (L) and width (W) of Q and τ , expressed as $\mu_N * W/L * \tau$. As V_{CC} is lowered, the design window for δ is increased, due to the non-scaling term V_T . This feature is opposite to that of the CTP scheme, in which the design window of the DC control voltage decreases as V_{CC} decreases. More design parameters and an increasing design window for the Qs for decreasing V_{CC} make the BCTP more suitable for low power DRAMs.

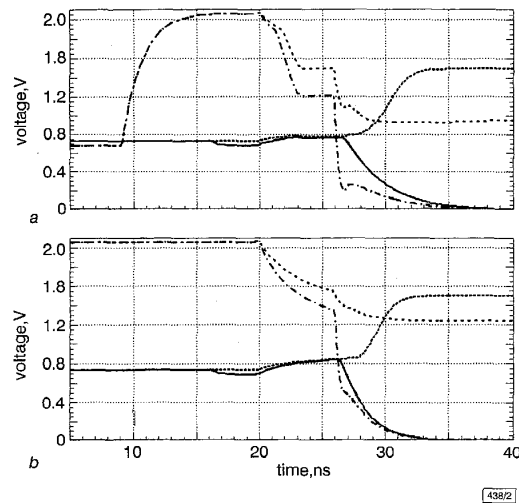


Fig. 2 Simulated voltage waveforms for proposed BCTP and for typical CTP

a Proposed BCTP
b Typical CTP
— V_{BL}
- - - $V_{/BL}$
- · - · V_{SA}
- - - $V_{/SA}$

Simulation results: The voltage waveforms of V_{BL} and V_{SA} in the proposed BCTP scheme have been assessed via SPICE simulation with the model parameters of 0.25 μ m DRAM technology. The power supply voltage was 1.5V, and the threshold voltage V_T were 0.38V for an nMOSFET and -0.55V for a pMOSFET, respectively. Cell capacitance C_S was 30fF and the ratio of bit line capacitance to cell capacitance C_{BL}/C_S was 15. C_{SA} was 30fF in the inversion mode, and 8.7fF in the depletion mode. The channel length and the channel width of the Qs, and pulse time of the PSG were determined for maximum sensing margin, given by eqn. 2. For comparison, the simulation was carried out with a typical CTP architecture that uses two precharge circuits for dual pre-

charge levels and DC voltage level as a control signal for the charge transfer. The precharge voltage for the SA-array was 2.2V, and DC voltage level for Q 1.4V. The other circuit parameters were equal to those of a BCTP circuit.

Fig. 2 shows the simulated voltage waveforms of V_{SA} and V_{BL} in the BCTP architecture. Since C_{BL}/C_S was assumed to be large, ΔV_{BL} has a small value of 43mV. After the charge transfer, a large ΔV_{SA} of 292mV was induced, which is 7 times larger than ΔV_{BL} . The CTP scheme also generated a large ΔV_{SA} of 196mV, a value which, however, is only 67% of that of the BCTP scheme. During the charge transfer, the V_{SA} of the BCTP made a more rapid transition. This is because C_{SA} has a small depletion capacitance when V_{SA} goes down below $V_{CC} + V_T$. The sensing time, defined as the time required for ΔV_{SA} to become 80% of V_{CC} , is also reduced by 0.5ns in the BCTP, compared with that in the CTP scheme.

Conclusion: The BCTP scheme has been developed to obtain a large sensing margin with small area overhead. It improves the sensing margin to be ~150% and reduces the sensing time by 0.5ns compared with the conventional CTP scheme under 1.5V operation. No additional array current flows and its design margin for the charge transfer switch becomes wider as the power supply voltage is scaled down. With these features, the BCTP scheme is found to be a promising sensing scheme for low power, Gbit-scale DRAMs.

© IEE 1998

Electronics Letters Online No: 19981161

7 August 1998

Jong-Shik Kim and Kwang-Seok Seo (Inter-university Semiconductor Research Center, School of Electrical Engineering, Seoul National University, San 56-1, Shinlim-dong, Kwanak-ku, Seoul 151-742, Korea)

E-mail: kjs@taurus.snu.ac.kr

Hoi-Jun Yoo (Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, 373-1, Kusung-dong, Eusung-ku, Taejeon 305-701, Korea)

References

- 1 ITOH, K., NAKAGOME, Y., KIMURA, S., and WATANABE, T.: 'Limitations and challenges of multi-gigabit DRAM circuits'. IEEE Symp. VLSI Circuits Dig. Tech. Papers, 1996, pp. 2-7
- 2 KIM, J.S., CHOI, Y.S., YOO, H.J., and SEO, K.S.: 'A low noise folded bit-line sensing architecture for multi-Gb DRAM with ultra high density $6F^2$ cell', *IEEE J. Solid-State Circuits*, 1998, **SSC-33**, (7), pp. 1096-1102
- 3 HELLER, L.G.: 'Cross-coupled charge-transfer sense amplifier'. ISSCC Dig. Tech. Papers, 1979, pp. 20-21
- 4 TSUKUDE, M., KUGE, S., FUJINO, T., and ARIMOTO, K.: 'A 1.2V to 3.3V wide-voltage-range DRAM with 0.8V array operation'. ISSCC Dig. Tech. Papers, 1997, pp. 66-67

Enhanced electrostatic force generation capability of angled comb finger design used in electrostatic comb-drive actuators

M.A. Rosa, S. Dimitrijevic and H.B. Harrison

A new comb finger design which enhances the operational performance of the commonly used electrostatic comb-drive actuator is presented. The angled comb finger design is discussed and shown experimentally to produce a greater actuating force than conventional rectangular comb fingers. Displacements up to twice as large as that achieved using rectangular comb fingers are shown for the same applied voltage.

Introduction: In microelectromechanical systems (MEMS) research, the most widely used micro-actuator is the electrostatic comb-drive actuator [1]. Based on the use of electrostatic force, applications of the comb-drive actuator have included polysilicon microgrippers [2], scanning probe devices [3], force-balanced accelerometers [4] and an actuation mechanism for rotating devices such as micro gear arrays [5]. Hence, the electrostatic comb-drive has been established as a fundamental building block in a wide variety of devices where mechanical actuation is required. As such,

any incremental improvement in device efficiency would be highly significant.

To date, electrostatic comb-drive actuators have been designed with rectangular or manhattan geometry type comb fingers. However, recent theoretical results have shown that a shaped comb finger design can greatly improve the operation of comb-drive microactuators [6]. Specifically, it has been found that the nonlinear electrostatic actuating force generated by a shaped (non-rectangular) comb finger would serve to cancel the opposing nonlinear restoring spring force of the comb-driver's support beams, thereby greatly increasing the operational range of the device [6].

In this Letter, we describe an angled comb finger design and demonstrate how an increased displacement over that of a rectangular comb finger design can be achieved for a given applied voltage. In fact, the results presented here complement the benefits of a shaped comb finger design which has been reported recently [6], therefore strongly indicating that a departure from the 'rectangular' design approach can lead to practical benefits.

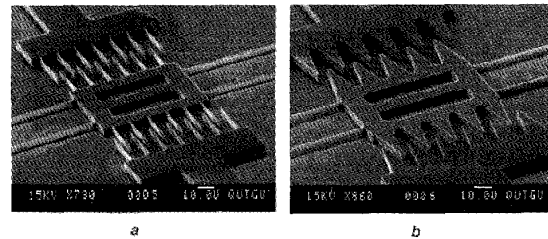


Fig. 1 SEM photographs of manufactured comb drive devices using standard rectangular comb finger design and new angled comb finger design for electrostatic force generation

Devices shown appear to be suffering from device stiction, a temporary effect caused by surface charging in SEM
a Standard rectangular comb finger design
b New angled comb finger design

Angled comb finger design: The actuating force generated via an angled comb finger design (Fig. 1b) can exceed that of a device using a rectangular design (Fig. 1a), since its output force increases parabolically with a diminishing comb finger gap. Despite a parabolic increase in actuating force, collision between opposing comb fingers is avoided due to the larger opposing force imposed by the support beam's spring constant, limiting the maximum achievable displacement. Eqn. 1 illustrates a relationship between comb finger angle θ , allowable clearance (maximum displacement) and comb finger gap width, such that a compromise based on these parameters and the intended application needs to be made before device design can take place.

$$\sin \theta = \frac{\text{gap width}}{\text{clearance}} \quad (1)$$

For example, a decrease in comb finger gap would increase the actuating force; however, the available clearance would decrease, reducing the maximum achievable device displacement unless the comb finger angle was also reduced. Therefore, the device designer could select the largest angle for a specified clearance and gap width, so as to maximise the actuation force.

To verify the benefits of the angled comb finger design, two comparable comb-drive actuators based on the rectangular and angled design approach, respectively, were designed, fabricated and tested. The comb-drive shown in Fig. 1b has a comb finger angle θ of ~8° and, as with the device shown in Fig. 1a, a clearance, gap width and comb finger overlap of 35, 5 and 15 μm , respectively. All test devices were fabricated using (100) BESOI wafers with device layer and BOX layer thicknesses of 4.5 and 2 μm , respectively, and processed using standard micromachining techniques [7, 8].

For an equitable comparison to be made, all comparable device dimensions are identical for both of the devices shown in Fig. 1. Aside from those already mentioned, these include a centre mass length of 98 μm and a support beam length and width of 1000 and 2.5 μm , respectively. Since the cell length of the rectangular and angled comb fingers is 18 and 22 μm , respectively, the comb-drive shown in Fig. 1a has six comb finger cells, while that of Fig. 1b