A 0.7-fJ/Bit/Search 2.2-ns Search Time Hybrid-Type TCAM Architecture

Sungdae Choi, Kyomin Sohn, and Hoi-Jun Yoo

***Abstract*—This paper presents a hybrid-type TCAM architecture which can utilize the benefits of both NOR and NAND-type TCAM cells: high speed and low power. A hidden bank selection scheme is proposed to activate limited amount of cells during the search operation avoiding additional timing penalty. Match line repeaters and sub-match line scheme are used for fast NAND search operation. A test chip with 144-kb TCAM capacity is implemented using 0.1-μm 1.2-V CMOS process to verify the proposed schemes. It shows 2.2 ns of match evaluation time on a 144-bit data search with 0.7 fJ/bit/search energy efficiency.**

***Index Terms*—Content-addressable memory (CAM), hidden bank selection (HBS), high speed, hybrid type, low power, match line repeater (MLRPT).**

I. Introduction

THE content-addressable memory (CAM) is one of the most favorite devices for high-performance data search in network search engine [1] or cache memory [2]. However, conventional CAM consumes too much power, preventing the implementation and the usage of large scale CAM in a single chip. Various CAM cells have been proposed [3] and all of them can be classified into two types, NOR and NAND, whether they are dynamic or static CAMs. Fig. 1 illustrates the structures of NOR and NAND-type CAM cells.

In the NOR type of Fig. 1(a), the comparison results of each CAM cell data with an input data determine on or off of the transistor attached to the match line. When the operation of the CAM begins, all of the transistors attached to the match line are turned off and the match line becomes precharged. As a search data is input to the CAM, the cell compares the stored value with the input value. When two values are different, the comparison result turns on the transistor discharging the match line. When two values are the same, the pass transistor remains off and the match line holds its precharged voltage. In NOR type, every comparison result of each individual cell affects the voltage level of the match line simultaneously generating the matching result fast. However, it consumes too much power as the CAM size increases because all of the match lines except the matched one should be precharged and discharged every search operation.

The match signal of the NAND-type cell in Fig. 1(b), however, should propagate through many pass transistors. Its operation also starts by precharging all of the match nodes. During the match evaluation time, the starter block generates the match signal which is opposite to the precharge level. In each cell, the pass transistor is turned on when the search value is equal to the stored one, and otherwise it is turned off. Only if all of the cells are matched completely, the match signal can arrive at the match line sense amplifier from the starter block. In this type, precharge and discharge of match lines are not required and the relatively lower power operation is possible compared with NOR-type cells. However, the match signal can propagate only after the previous cells complete their operation. That is, the matching operation is evaluated sequentially starting from the first cell to the last cell resulting in slow search operation.

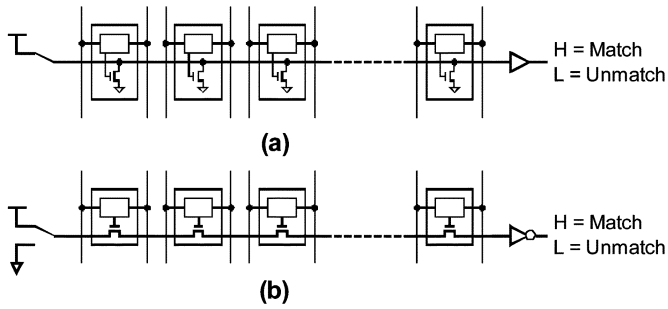

Fig. 1. (a) NOR-type and (b) NAND-type CAM.

Generally, conventional CAM consists of homogeneous cell structure, either NOR or NAND-type cell. And previous works have been focused only on either reducing the power consumption of match line [4] or enhancing the search speed [5]. In this paper a new CAM architecture is presented by utilizing only the benefits of NAND and NOR cells; NOR's high-speed and NAND's low-power characteristics.

This paper is composed as follows. In Section II, details of the proposed hybrid-type TCAM architecture is explained. Section III presents the design schemes used in the NAND-type TCAM cell array. To enhance the search speed of NAND-type TCAM cell, the match line repeater circuit and a new word structure is proposed. Section IV presents the implementation results of a test chip. And the concluding remarks are given in Section V.

II. Hybrid-Type TCAM Architecture

In most of the current router systems, a network processor analyzes its lookup data and rearranges or sorts them in order to support high speed matching algorithms such as longest matching prefix search [6] before the data are stored in its search engine. In this case, most of the data are divided into common data portion, called merged field (MF) in this paper, and its unique data portion, called individual field (IF). We can use these features to devise a hybrid-type TCAM architecture

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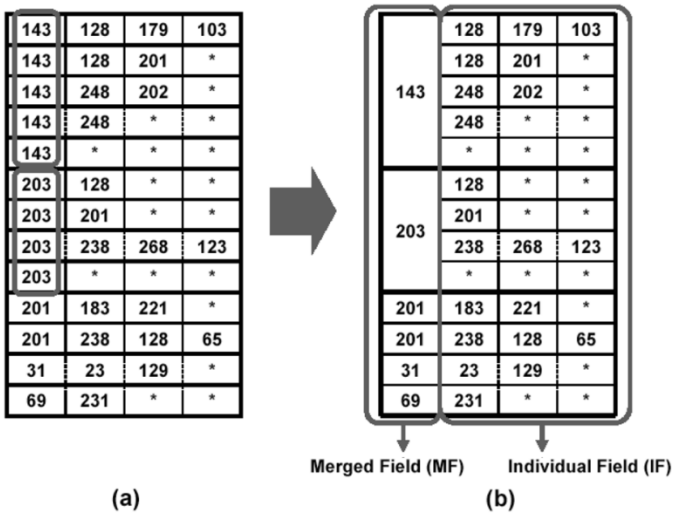


Fig. 2. IPv4 Destination address lookup table.

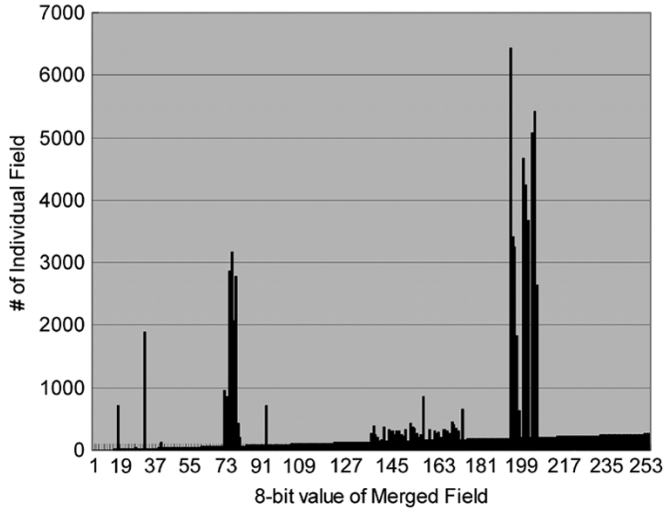


Fig. 3. Distribution of lookup data in IPv4 router.

to reduce both power and search time at the same time while utilizing only the benefits of both NOR and NAND-type CAM cells. That is, a small amount of the common lookup data are stored in the NOR-type CAM and the remaining large portion of data are stored in the NAND-type CAM.

A. Characteristics of Lookup Data

Fig. 2(a) shows the contents of an exemplary lookup table which is assumed to store IPv4 destination IP addresses. To support the classless interdomain routing (CIDR) [6], the data are sorted and stored in the CAM. Dividing them into the first 8-bit Merged Field (MF), and remaining 24-bit Individual Field (IF), many lookup data are found to share the common MF such as 143 or 203 in Fig. 2(b). And the real data distributions used in the routers of the Internet Service Providers (ISP) [7] also show the same appearance. One of the data distribution with 70 781 lookup entries is shown in Fig. 3. The x-axis indicates the value of 8-bit MF data ranging from 0 to 255 and the y-axis indicates the number of the IF data per 8-bit MF. Notice that only 50 MF values can cover 95% of entire data when 8-bit is allocated to

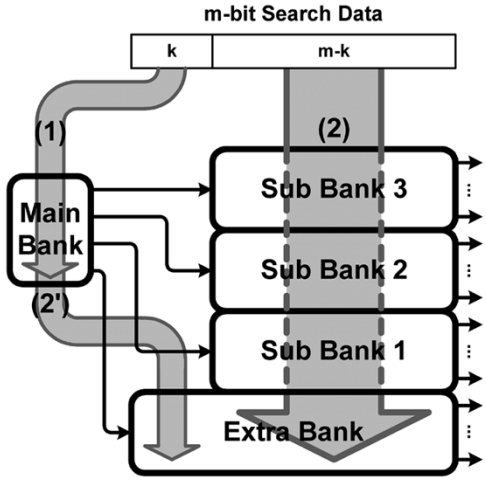


Fig. 4. Block diagram of hybrid-type TCAM architecture.

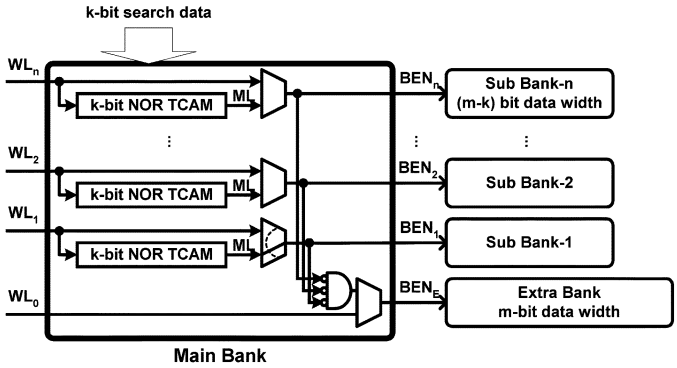


Fig. 5. Main bank.

MF. The number of MF values can be changed with the variation of the bit width of MF and IF. If the IF data of the common MF are located in the same bank or in the same cell array, we can activate only the bank and can reduce its power consumption while supporting full parallel search operation. Although a bit-serial architecture [8] is proposed for low power search operation, it still suffers from low searching speed.

B. Hybrid Type TCAM Architecture

Fig. 4 shows the organization of the hybrid-type TCAM architecture. It has three different types of banks: the main bank, the sub-bank, and the extra bank. The main bank stores k-bit MF data out of m-bit data and the number of its word lines is equal to the number of sub-banks which store $m-k$ bit IF data. The match result of each word line in the main bank is used to activate the corresponding sub-bank. If some data do not have any common MF with other data, the extra bank stores them without dividing them into MF and IF. Area saving can be expected with this architecture. Assuming that a CAM of $B \times m \times W$ where B is the number of the banks, m is the bit width of a bank, and W is the number of words in a bank. If our architecture is applied to this CAM, the total amount of the cells is given by (1):

$$\text{Total number of cells} = m \times W + (B-1) \times ((m-k) \times W) + (B-1) \times k. \quad (1)$$

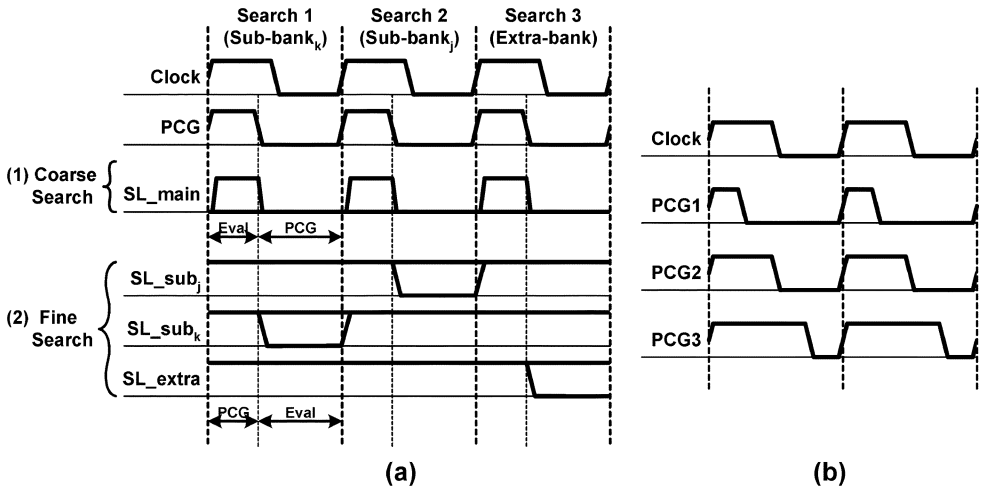


Fig. 6. Timing diagram of hidden bank selection scheme.

where k is the bit width of MF. In this equation, it is clear that the area of this architecture approximately becomes only $(m-k)/m$ of the area of the conventional architecture.

The search operation starts looking at the contents of the main bank. Fig. 5 shows the block diagram of the main bank. When input data is matched with stored one, a corresponding sub-bank is activated and the rest of the search is continued only within that sub-bank. Otherwise, the extra bank is activated and the search operation is performed within the extra bank while the remaining banks are turned off. Since the main bank stores a small amount of data, it can be made of NOR-type TCAM cells for fast search operation while the sub-bank and extra bank are implemented by NAND-type TCAM cells for low power search operation.

The write operation is similar to that of the conventional memory although the architecture is quite different from each other. In the Fig. 5, the MSB address, whose bit width is $\log 2\,(\mathrm{wl})$ and wl is the amount of the word lines of the main bank, is used to decode the word line of the main bank. The remaining bits of the address are used to select the word line of the sub-bank. When an input address arrives, a word line of the main bank and the corresponding bank enable signal (BEN) are activated. If the input address indicates a sub-bank, the word line of the main bank activates both the k-bit NOR TCAM word and the sub-bank, where k-bit data and $(m-k)$ bit data are stored in the designated location, respectively. If the address is that of the extra bank, the word line of the main bank activates the extra bank and the data are written in the extra bank. During the write operation, k-bit data should not be changed if the value of the MSB address is not changed, and this is managed by the control part of the CAM.

A hidden bank selection (HBS) scheme is adopted to compensate the additional time required for the main bank search in advance. The CAM cell requires both precharge time and evaluation time to generate its match result. In the proposed hidden bank selection scheme, the precharge and evaluation times of the main and the sub/extra banks can be overlapped with each other as shown in Fig. 6(a). The match line in the main bank is precharged during the low level of the PCG signal of the previous clock cycle. During the high level of PCG signal, the match result of the main bank is evaluated while the sub/extra banks are in their precharge time. After the transition of the PCG signal, the precharge of the sub/extra banks is finished and the main bank generates the activation signal for sub/extra banks. With the hidden bank selection scheme, no additional time is required for main bank activation although the main bank and sub/extra bank operate sequentially. Therefore, the search operation can be completed within one clock cycle and the search result is always generated in one clock latency.

Various organizations are possible for the implementation of the proposed hybrid-type TCAM architecture according to the data characteristics and the distribution of MF and IF data. And the duty cycle of PCG signal is also varied. Fig. 6(b) shows three kinds of PCG waveforms. With PCG1, the sub/extra banks secure long evaluation time and the evaluation of main bank should be finished quickly because the evaluation time of main bank is limited. Such operation requires the main bank with NOR-type CAM cells for fast match evaluation and the sub/extra bank with NAND-type CAM cells. This organization is suitable for the search of large bit width with small amount of MF data. When the main bank stores a variety of MF data, it requires large capacity consuming large power if NOR-type cells are used. The data characteristics which require the PCG3 type can be modified and implemented using PCG1 by exchanging the MF and IF.

III. Sub/Extra Bank

Fig. 7 shows the structure of an extra bank with 144-bit I/O width. The only difference between the sub-bank and the extra bank is the data I/O width. That is, m bit for extra bank and $m-k$ bit for sub-bank. The sub/extra banks adopt match line repeater (MLRPT), sub-match lines, 1-bit column decoding and local priority encoding (LPE) schemes to enhance the operation speed of NAND-type cell and to reduce its redundant energy consumption.

A. Match Line Repeater

Although NAND-type cell shows the low power search operation, it still requires long match evaluation time due to the

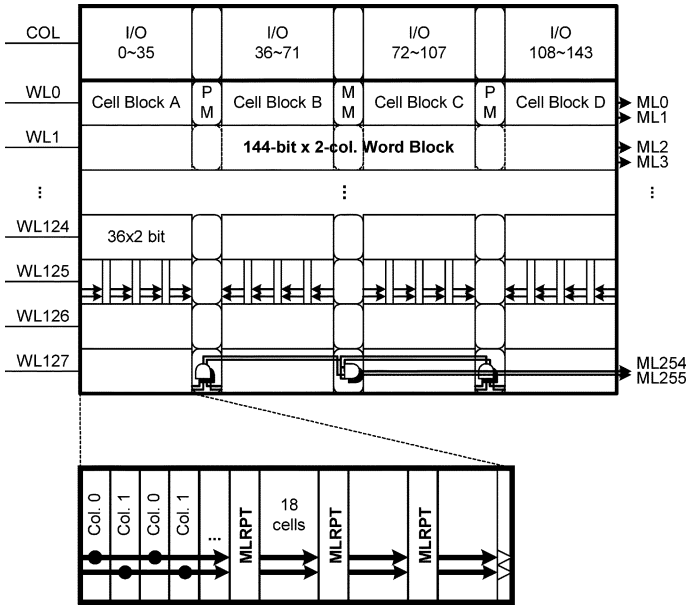


Fig. 7. Sub/extra bank structure.

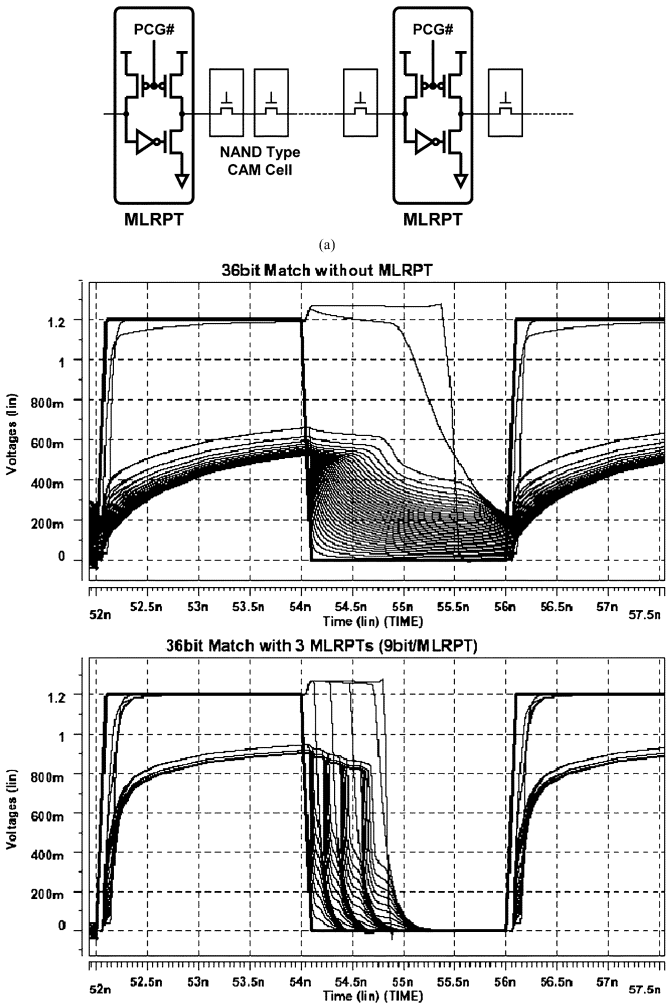


Fig. 8. (a) Match line repeater schematic. (b) Waveform comparison.

propagation delay through the pass transistors. The match evaluation time is proportional to the number of pass transistors or the search data width. As the match signal passes through more and more transistors, the signal propagation along the match line gets slower and its voltage level gets degraded as shown in Fig. 8(b). This results in the increase not only of the signal propagation time but also of precharge time because the precharge signal is also transferred via pass transistors. This is why the NAND-type cell is not adopted in the implementation of the large bit width CAM.

In this work, we place the MLRPT of Fig. 8(a) at every nine pass transistors to speed up the propagation of the match line signal. It is designed with five transistors and consumes only a 1/3 of the NAND-type TCAM cell area. In the precharge phase, two pMOS transistors of MLRPT precharge the left and right match nodes to their high level. In the evaluation phase, the pMOS transistors are turned off and the node is floated. If a match signal with low voltage level is propagated to the input of the MLRPT, the nMOS of MLRPT is turned on and sinks down the charge from the right match node. If it is mismatched, the input and output nodes of MLRPT remain precharged without any additional energy required for next precharge.

The upper waveform of Fig. 8(b) is the waveform of the match line node voltage for 36-bit data search without any MLRPT and the bottom one is the result when three MLRPTs, a MLRPT per nine cells, are included. The precharge level is enhanced sharply and the match evaluation time is reduced by 40%, sacrificing only 3% area overhead.

B. Word Block

A bank consists of many word blocks and I/O drivers. A word block consists of four cell blocks, two partial match blocks (PM) and a main match block as shown in Fig. 7. Each cell block includes 72 NAND-type TCAM cells and 3 MLRPTs to construct a search engine with 144-bit search data width. 288 cells are attached to each word line and they are column-decoded using LSB address when read or write operation is performed.

Although the MLRPT speeds up the match evaluation time and stabilizes the voltage level of the match nodes, the search time using NAND-type cell is still slow because the match evaluation time is proportional to the bit width of the search data. The proposed sub-match line scheme can reduce the search time by dividing the search area. A word is divided into four cell blocks as shown in Fig. 7 and the comparison of the blocks is performed simultaneously for fast search using NAND-type CAM cell. The match results of the cell blocks (A, B) and (C, D) of Fig. 7 are merged in the partial match blocks (PM) and the results of two PMs are merged in the main match block (MM). Fig. 9 shows the schematic diagrams of PM and MM. Partial match lines AB0, AB1, CD0, and CD1 are precharged and evaluated by PMs. (AB0, CD0) and (AB1, CD1) represent the partial match results of column 0 and column 1, respectively. They are merged to generate the final match results MLout0 and MLout1 by MM. When both the column 0 and column 1 are matched, only the match line of column 0 is valid because of the priority policy [9]. The generation of MLout1 is controlled by the value of MLout0 in the MM to suppress unnecessary swing of match

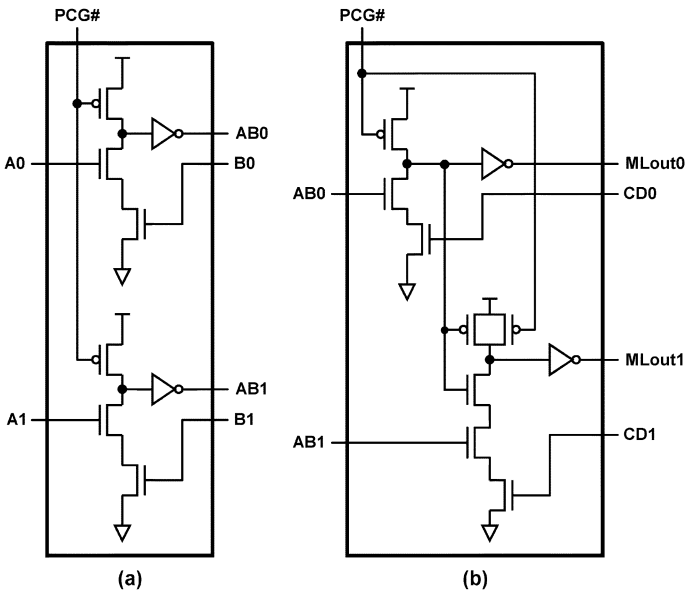


Fig. 9. (a) Partial match block (PM). (b) Main match block (MM).

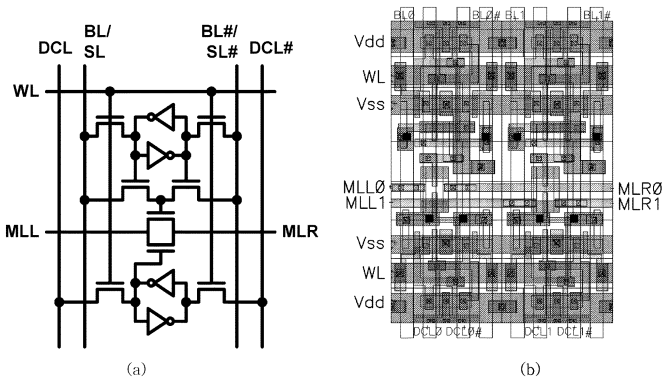


Fig. 10. (a) Schematic of NAND-type TCAM cell. (b) Layout of TCAM cell pair.

line. Therefore, the MM not only generates the final match result but also functions as the local priority encoder (LPE).

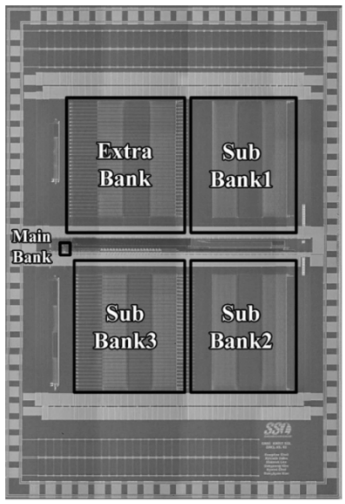
C. Cell Structure

Fig. 10(a) shows the circuit of the NAND-type TCAM cell used in this study. It is designed to read/write the ternary data within one clock cycle. The TCAM cell consists of two 6-Tr SRAM cells and the comparison logic. The upper SRAM cell stores the binary value, "0" or "1", and the value of the bottom SRAM cell indicates whether the TCAM cell stores binary value or "don't care" value [10]. If the bottom cell stores "1", the pass transistor is always turned on and the match lines MLL and MLR remain connected irrespective of the stored values in the upper cell. And it means that the TCAM cell stores "don't care" value. If the value of the bottom cell is "0", the connection of MLL and MLR depends on the comparison result between the values stored in the upper cell and the signal value on the SL pair. Fig. 10(b) shows the layout of the TCAM cell pair. Two CAM cells are laid out in one unit to avoid the conflict between the match lines of each column, ML0 and ML1. The

TABLE I
ENERGY CONSUMPTION OF PROPOSED NAND CELL ARRAY

[fJ/bit/search]

	@ Match	@ Mismatch
Search Line (SL)	1.87 (68%)	1.87 (100%)
Partial Match Block (PM)	0.30 (11%)	0.0005
Main Match Block (MM)	0.16 (5%)	0.001
MLRPT	0.47 (16%)	0.0005
Total	2.80	1.872



Technology		100nm CMOS SRAM
Power Supply		1.2V
Chip Size		2.8mm x 4.2mm
Cell Size		22.4um2 Peri. Rule
Bank	Main Bank	3wl x 8b
	Sub Bank	128wl x 1col x 136b
	Extra Bank	128wl 1col x 144b

Fig. 11. Microphotograph of the test chip.

size of a cell is 2.86 μm $\times$ 7.82 μm and double pitches of the cell can be provided for the I/O driver layout with the help of the 1-bit column decoding. In the read/write operation, the I/O block drives either BL0/SL0, DCL0 pair or BL1/SL1, DCL1 pair, according to the column address. In the search operation, it drives both the BL0/SL0 and BL1/SL1 pairs to find the matched data.

Table I shows the energy consumption of the NAND-type TCAM cell array. It is clear that most of the energy is used to drive the search line. When all words of the bank are fully matched, the bank shows 2.8-fJ/bit/search energy performance. 1.9-fJ/bit/search energy is consumed when all bits are mismatched. If the hybrid architecture consists of three sub-banks and an extra bank, the energy can be saved by 75% because only one bank is always activated during the search operation.

IV. IMPLEMENTATION

To verify the proposed architecture, a test chip is implemented using 100-nm CMOS SRAM technology. Fig. 11 shows the micrograph of the implemented test chip. It consists of one main bank, three sub-banks, and one extra bank. It has 144-kb ternary data capacity using 138 kb + 24 b TCAM cells. The main bank consists of NOR-type TCAM cells and stores three kinds of 8-bit MF data. The data width of the sub-bank is

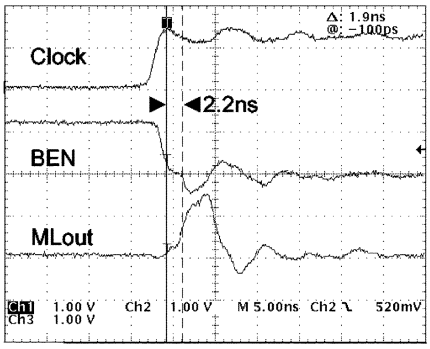


Fig. 12. Measured waveform.

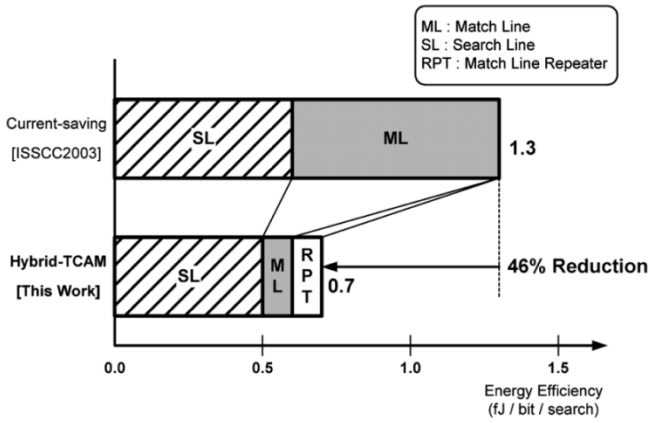


Fig. 13. Energy consumption of the test chip.

136 bit and each sub-bank can store 256 IF data. The extra bank has 128-word × 2-column × 144-bit capacity. The sub-bank and extra bank have the same architecture except their bit widths. When each word of the main bank stores different data, one sub-bank or extra bank is always activated and the energy efficiency per each TCAM cell is reduced to its quarter because there are four sub/extra banks. Therefore, the energy efficiency for search operation is 0.7 fJ/bit/search.

Although additional area overhead for MLRPT, MM and PM is 3%, 0.7% and 0.8%, respectively, 4% area reduction due to three sub-banks compensates the overhead. This is because the MF data are merged and stored in the main bank which has less than 0.1% area of entire CAM. The proposed architecture shows 144-kb TCAM capacity using 138-kb sub/extra banks and 24 b main bank. This means that we can save 6 kb with this architecture. Since the data in each sub-bank share 8-bit MF stored in the main bank, each sub-bank has 256 words, and there are three sub-banks, the information of 24-b main bank amounts to 6-kb data as explained in the (1).

Fig. 12 is the measured waveforms of the test chip. As a search operation starts at the rising edge of the clock, the main bank generates the bank enable (BEN) signal to activate a sub/extra bank, and the search operation continues in the designated bank. After 2.2 ns of evaluation time, the final match output (MLout) is generated. If the 1-ns precharge time of the sub/extra bank is taken into consideration, up to 300-MHz operation can be realized for the test chip.

V. Conclusion

The hybrid-type TCAM architecture is proposed to utilize only the benefits of both NAND-type and NOR-type CAM cells, low power of NAND CAM and high speed of NOR CAM. In addition, various schemes such as hidden bank selection (HBS) scheme, match line repeater (MLRTP) circuit, and sub-match line scheme are proposed to enhance its high speed and low power characteristics. A test chip is implemented to verify the operations of the proposed architecture and schemes. It can access 144-kb ternary information and search 144 bit width data within 1-clock cycle at 300-MHz clock. The proposed architecture activates only the limited number of sub-banks or an extra bank to reduce the search power consumption drastically. And the test chip shows 0.7 fJ/bit/search energy efficiency.

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Dr. Yoo received the 1994 Electronic Industrial Association of Korea Award for his contribution to DRAM technology.