POPeye : A System Analysis Simulator for DRAM Performance Evaluation

Kangmin Lee, Chi-Weon Yoon, Ramchan Woo, Jeong-Hun Kook, Yon-Kyun Im, and Hoi-Jun Yoo

***Abstract*− We implemented POPeye (Probe of Performance + eye), a system analysis simulator to evaluate DRAM performance in a personal computer environment. When running any real-life application programs such as Microsoft Office and Paint Shop Pro on Windows OS, POPeye simulates detailed transactions between a CPU and a memory system. Using this tool, we comparatively analyzed the performance of a DDR-SDRAM, a D-RDRAM, and a DDR-FCRAM.**

***Index Terms*− popeye, simulator, DRAM, Performance, Windows**

I. INTRODUCTION

MOST computer systems are based on a stored program architecture that consists of a CPU, a memory and input/output devices. In order to improve the overall performance in stored program architecture, it is necessary to increase the speed of memory as well as the speed of CPU and the capacity of a memory. Because the memory bandwidth becomes a bottleneck of a system performance, many researches for faster memories are in progress and new high performance memory systems for 3D graphics or image processing are being proposed and developed by many DRAM companies [1 ~ 4].

As a D-RDRAM (Direct-Rambus DRAM), DDR-SDRAM (Double Data Rate-SDRAM), and VCM(Virtual Channel RAM) are getting widely used in the PC and the workstation market, the performance analysis of these two DRAM architectures are a hot issue [5, 6]. Therefore, the exact performance evaluation of the DRAM systems is crucial. The system level performance analysis is also required because the simulation of only the DRAM itself is not enough to evaluate the exact performance of the DRAM in the system.

There are two methods for performance evaluation at system level; a hardware and a software based method, in other words, an emulation and a simulation, respectively. The former gives more reliable results than the latter, because exact system modeling in software is impossible. But a hardware implementation of an entire system costs more money and time. And it has less adaptability to system variation than a software method does. Consequently, the software modeling needs less development cost and time than the hardware method. It also has flexibility in performance analysis of diverse systems which have different concepts of DRAMs, such as a DDR-SDRAM and a D-RDRAM. Moreover, the software simulator can evaluate the performance of a new DRAM architecture before the fabrication of the actual sample chip. But software simulation requires more simulation time and gives less reliable results than hardware simulation. In order to overcome the weak point of the software method, we implemented POPeye (Probe of Performance + eye) which is a system analysis simulator for DRAM performance evaluation in a PC. A memory system of POPeye is modeled at a structural level for more realistic simulation results but the other parts are modeled at a behavioral level for fast simulation [Figure 1]. POPeye is developed for the detailed performance analysis of a DRAM system while a real-life application programs such as Microsoft Word, Excel or Paint-Shop-Pro are running. The distinguished

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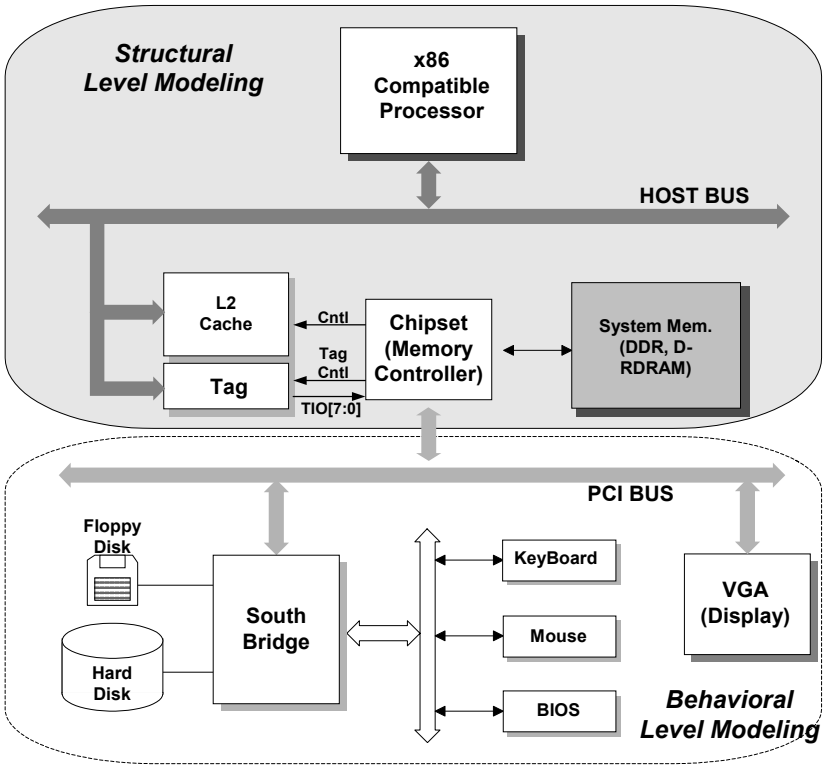

Fig. 1. Target PC System (Virtual PC) of POPeye.

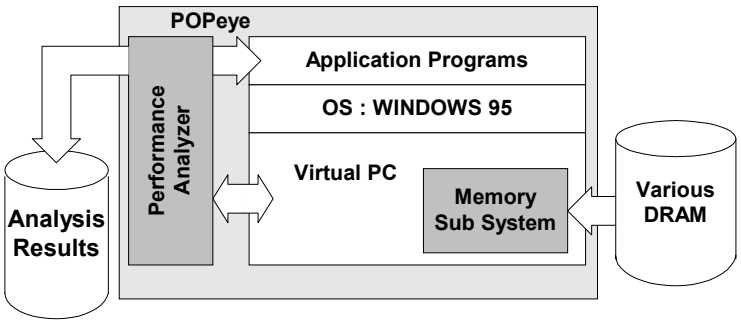

Fig. 2. Configuration of POPeye.

advantage of POPeye is that it can run real-life Windows programs as well as benchmark programs. With the POPeye, we analyzed the performance of a DDR-SDRAM, a D-RDRAM and a DDR-FCRAM in a PC system. Detailed simulation results will be explained in part IV.

II. POPEYE : SYSTEM ANALYSIS TOOL FOR DERAM PERFORMANCE MEASUREMENT

POPeye is a software simulator for the PC's DRAM performance analysis [7]. It consists of two parts: a Virtual PC and a Performance analyzer as shown in Figure 2. Virtual PC is a software model of a desktop PC system which has a Pentium microprocessor, L2 cache, a memory system and peripheral devices such as a keyboard, a mouse, and a VGA display. [Figure 1] The POPeye is implemented with C++ language but also partially with C and assembly language. POPeye was used for a performance evaluation of EDO-DRAM, VC-SDRAM, and VPM before. [7,8] Detailed Configurations are as follows.

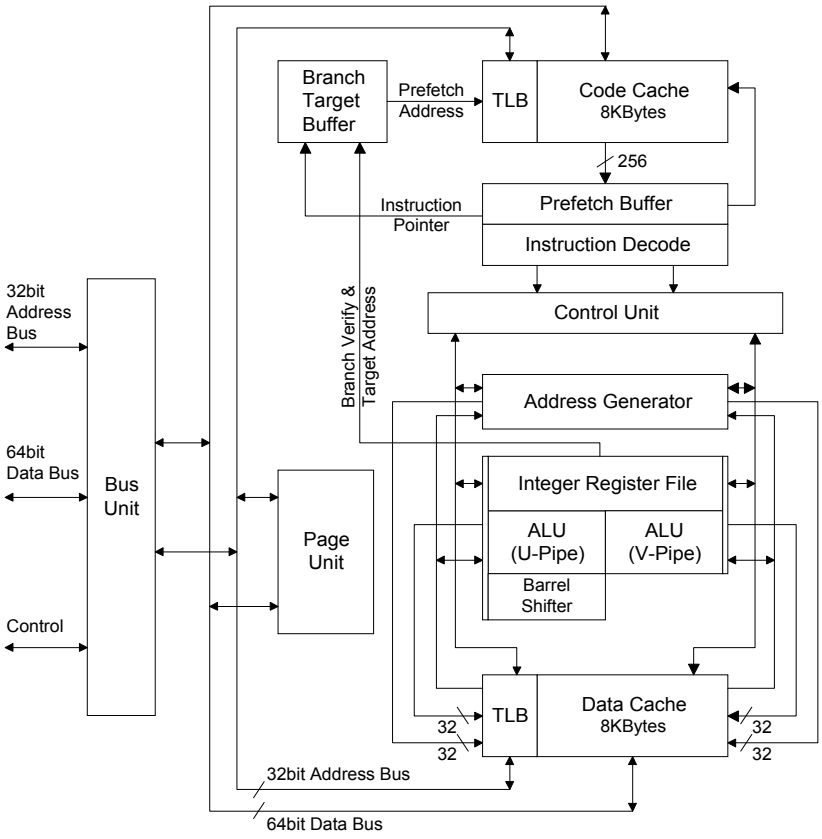

Fig. 3. Block diagram of Pentium Process.

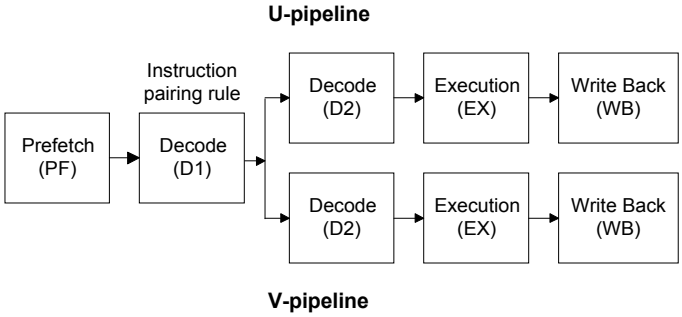

Fig. 4. Integer Pipeline of Pentium Processor.

A. *x86 Processor*

Since Intel developed 8086 Processor in 1978, it has dominated CPU and computer market in the world. Figure 3 shows a block diagram of a Pentium Processor as a target processor model of POPeye.

Pentium Processor is a superscalar processor having 5 stage pipeline and dual integer pipeline. [Figure 4] Therefore it can execute dual integer instruction concurrently. In this architecture, Instruction Stream Scheduling is very important to utilize the dual integer units efficiently. This scheduling is done at D1 stage by instruction pairing rule. [Figure 4] Pentium Processor has two on-chip caches of 8kbyte instruction (or code) and 8kbyte data cache. They consist of 250 lines of size of 32bytes and use 2-way set associative mapping. 8Byte data are transmitted at once through 64bit external data bus interface so it takes 4clock cycle time to refill one line of the cache. Data cache has 8banks and dual read

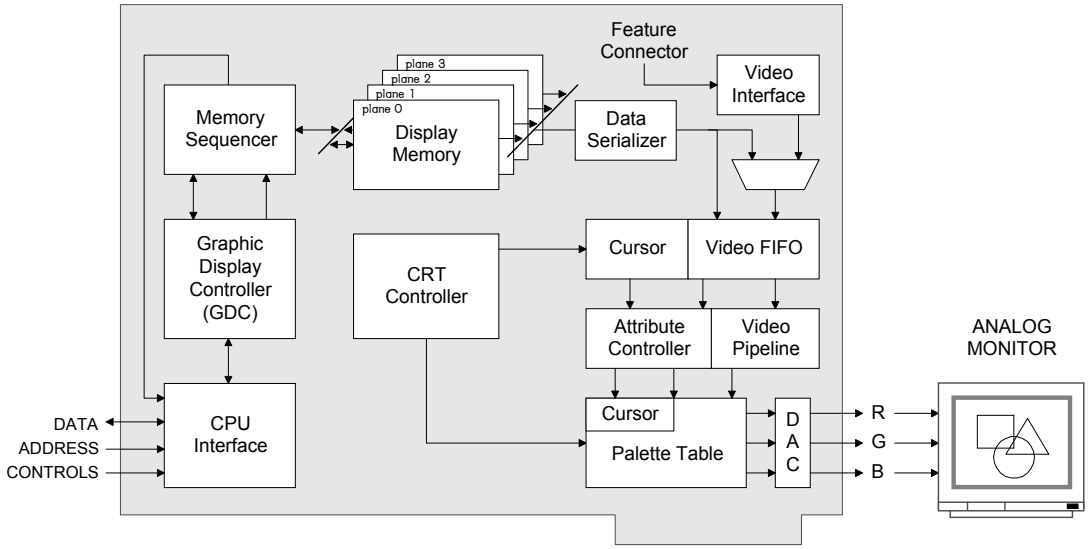

Fig. 5. The structure of VGA Graphic Card.

ports to support dual integer pipeline. A Instruction Prefetcher consists of dual 64byte prefetch buffer and branch prediction buffer(BTB) of 256 entry.

The CPU of Virtual PC modeled Pentium Processor at behavioral level except registers, instruction decode unit and caches which were modeled at structural level to analyze detailed transactions between a memory system.

B. *BIOS*

The BIOS (Basic Input Output Service) is a firmware which makes PC programs do not depend on PC's architectures. The BIOS of real PC is coded by assembly language but that of POPeye is coded by C language as well as Assembly for easy control of Virtual PC's components.

The BIOS of real PC is stored in a ROM and provides several routines and data to the system at boot-up stage. In Virtual PC, however, the BIOS is stored in main memory from F0000h to FFFFFh (Extension BIOS range), so the BIOS access is forwarded to main memory Access of the Extension BIOS range.

C. *L2 Cache*

Most PC systems based on Pentium Processor use SRAM(Static RAM) as external cache and the kind of SRAM is depend on a chipset and a control algorithm. Recently, Synchronous SRAM and Pipelined Burt SRAM are widely used.

The L2 cache controller implemented in POPeye is based on Intel 440BX Chipset whose configurations are as follows

- 1MB PBSRAM
- Direct Mapped, 32byte line size
- Write Back Algorithm
- No Write Allocation Policy (On Write Miss)
- Full Coherency Mechanism between L1 and L2 cache by MESI Protocol

D. *Memory*

In a Virtual PC, memory access from processor is done byte by byte, therefore POPeye can track the memory access trace. The data bus width is actually 64bit, so memory access time of one burst length is considered as one bus cycle in POPeye. Plus, the access of Extended BIOS range is not considered as memory access.

E. *Hard disk and Floppy disk*

A hard disk and a floppy disk are modeled as input and output peripherals in Virtual PC. The implementation can be considered as two way as follows.

- Make a directory in a UNIX system and consider the directory as a root directory of hard disk of Virtual PC. This Method make the transmission of files between UNIX and a Virtual PC very easy. But in this method

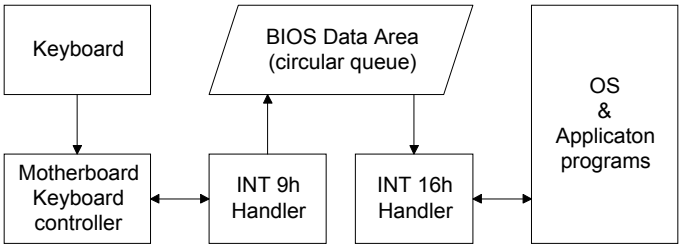

Fig. 6. Conversion Process of keyboard code.

Fig. 7. POPeye simulation example.

DOS file system must be described and it cannot be applicable at the other OS except DOS.

• Consider a file as a hard disk. The information about sectors, tracks, cylinders and header of hard disk is converted to the offset of the file.

The second method is applied in Virtual PC. The way of making the image of disk file at UNIX is as follows

• Hard disk

dd if=/dev/zero of=505M bs=512 count=1032192

• Floppy disk

dd if=/dev/zero of=1.44M bs=512 count=3360

The hard disk has a capacity of 504Mbytes for Windows 95 and Windows Application Programs.

• Total number of sectors of hard disk = Cylinders(1024) x Heads(16) x Sectors/Track(63) = 1032192.

• Total number of sectors of floppy disk = Cylinders(80) x Heads(2) x Sectors/Track(21) = 3360.

These image files of hard disk and floppy disk can be accessed in UNIX system by 'MTOOLS' which is software for data conversion between UNIX file system and DOS file system.

F. *VGA (Video Graphic Array)*

VGA is a 256 color graphic card. Figure 5 shows a

data process in VGA graphic card. Data from processor stored in Display Memory after several operations in Graphic Display Controller. Then, those are converted to analog signals of proper color in the attribute controller through a data serializer. Memory sequencer and CRT controller generate timing signals.

In Virtual PC of POPeye, VGA handler is modeled at behavioral level and the BIOS related to VGA control is from open sources of Elpin System [www.elpin.com]. VGA BIOS is called frequently so that it is located in main memory for the faster access. 64bit data can be transmitted at once from a main memory while 8bit data do from a ROM. Therefore Video BIOS is assigned from C0000h to C7fffh of main memory.

G. *Keyboard*

Figure 6 shows the conversion process from keyboard inputs to ASCII codes by BIOS routines (INT 9h, INT16h).

H. *Mouse*

Virtual PC's mouse point position is calculated by adding the distance from the initial point when it comes in the simulation window to the current position to the initial position. Widows OS manages a mouse directly so that the modeling of INT 33h is not enough to handle a mouse.

We modeled an x86 processor that is compatible with a Pentium microprocessor at instruction level [9], so the virtual PC can directly execute real-life application programs based on Windows OS without any modification. The processor of POPeye was modeled at the mixed level between the structural level and the behavioral level. Especially, the parts that are related to memory were modeled at detailed structural-level because we need the detailed transaction information of the DRAM system. The size and mapping type of L1 cache, BTB (Branch Target Buffer) and TLB (Transition Look aside Buffer) can be modified according to the specific architectures. The memory system consists of a L2 cache, a chipset (memory controller), and a main memory (DDR-SDRAM, D-RDRAM, and DDR-FCRAM). The size and mapping type of L2 cache are also variable.

While the virtual PC simulates the real PC and runs real-life application programs in a workstation, the performance analyzer collects detailed transaction information about DRAM access. Figure 7 shows POPeye simulating a virtual PC on Windows OS on my workstation environment.

Table 1 Virtual PC's Configuration.

CPU	166MHz x86 Compatible Processor
L1 instruction / data Cache	• 8Kbytes / each • 2way Set Associative Mapping • 32Byte Line Size
L2 Cache	• 1Mbytes • Direct Mapping, 32 Byte Line Size
Main Memory	DDR-SDRAM or D-RDRAM or DDR-FCRAM

Table 2 Specifications of DRAMs [10, 11, 12].

		DDR-SDRAM	**D-RDRAM**	**DDR-FCRAM**
Module Size		128Mbytes	128Mbytes	128Mbytes
Chips/module		8	8	8
Banks/chip		4	32	4
Chipset based on		Intel 440BX	Intel 820	Intel 440BX
I/O pins		64	16	64
Data/address		64bit	128bit	64bit
Burst Length		4	2	4
Clock speed		133MHz	400MHz	133MHz
CAS Latency		2	2	2
Latency	**tRC**	65ns	80ns	30ns
	tRAC	30ns	45ns	22.5ns
max. throughput		2.1GB/s	1.6GB/s	2.1GB/s

Table 3 Read and write access ratios of different applications.

Application nogram	**Write access**	**Read access**
Windows 95 Boot-up	47.6%	52.4%
Paint Shop Pro 4.0	32.5%	67.5%
Microsoft Excel 7.0	35.6%	64.4%

Table 1 shows our configuration of Virtual PC which consists of 166MHz x86 compatible microprocessor, 16KB instruction and data L1 caches with 2way set associative mapping and 1MB direct mapping L2 cache. Main Memory can be anyone of DDR-SDRAM, D-RDRAM, and DDR-FCRAM.

III. Modeling Of A DDR-SDRAM, A D-RDRAM, And A DDR-FCRAM

We modeled a DDR-SDRAM, a D-RDRAM, and a DDR-FCRAM in clock cycle level with C++ language. Table 2 shows Detailed Specification of DRAM systems. [10,11,12]

128Mbyte DDR-SDRAM module consists of eight 128Mbit DDR-SDRAM (16Mbit x 8bit) chips. Each DDR-SDRAM has 4 banks. We modeled a DDR-SDRAM chipset based on the Intel 440BX chipset that supports SDR (Single Data Rate)-SDRAM [13]. The modules have the maximum bandwidth of 2.1 Gbyte/sec (=133MHz x 2 (Double Data Rate) x 64bit(I/O pins)) with 64bit bus at 133MHz.

128Mbyte D-RDRAM module consists of eight 128Mbit RDRAM (256Kb x 16bit x 32banks) chips. Each RDRAM has 32 banks. The modules have the maximum bandwidth of 1.6 Gbyte/sec (=Dualoct (16Bytes) x 400MHz / 4 (4 t_{cycle})). We modeled a RDRAM controller (chipset) based on the Intel 820 chipset [14]. 128Mbyte DDR-SDRAM module has same configuration as 128Mbyte DDR-SDRAM module except it's latency.

IV. Simulation Results

We run three applications on a POPeye simulator: Windows 95 Boot-up, Paint Shop Pro 4.0 and Microsoft Excel 7.0. These programs have different memory access patterns.

Table 3 shows read and write access ratios of three applications. Paint Shop Pro 4.0 needs more read access than other applications and Windows Boot-up needs more write access than other applications. This result is from POPeye simulation.

Figure 8 shows memory access pattern for DDR-SDRAM and DDR-FCRAM. Page hit ratio (Same Bank & Same Row access) is approximately 50% and Page Miss ratio (Same Bank & Different Row access) is about 30 ~ 40%. Bank interleaving ratio is approximately 10%. MS-Excel program makes largest Page hit ratio and smallest Page miss ratio.

We compared the performance of a D-RDRAM and a DDR-FCRAM with DDR-SDRAM. A performance index is the reciprocal of the execution time. The execution time for each application is a product of the number of total clock cycle for each application and clock cycle time as shown in following equation.

The clock speed of a DDR-SDRAM, a D-RDRAM, and a DDR-FCRAM system is assumed to 133MHz, 400MHz, and 133MHz, respectively, which is shown at commodity DRAMs

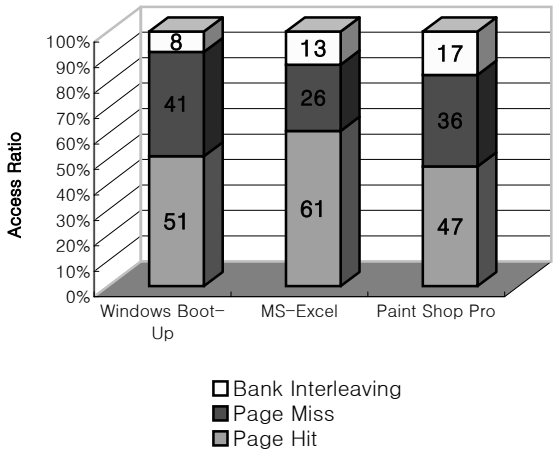

Fig. 8. Memory access pattern for DDR-SDRAM and DDR-FCRAM.

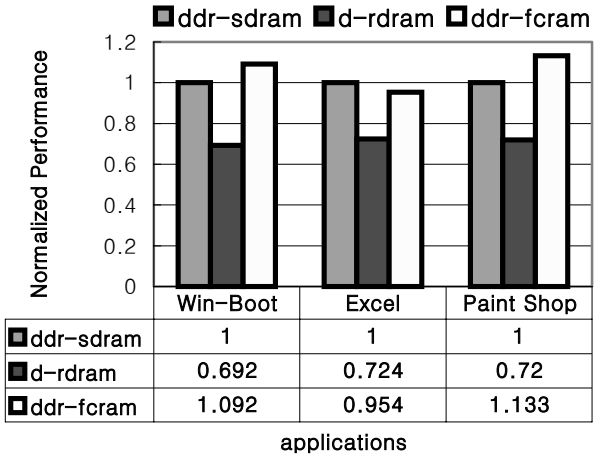

Fig. 9. Normalized performance comparison of DDR-SDRAM, D-RDRAM, and DDR-FCRAM.

Figure 9 shows the normalized performance of a 128Mbyte DDR-SDRAM, a 128Mbyte D-RDRAM, and a 128Mbyte DDR-FCRAM for three different applications: Windows Boot up, Paint Shop Pro 4.0 and Microsoft Excel 7.0.

In all applications, DDR-SDRAM outperforms D-RDRAM about 30%, because a DDR-SDRAM needs shorter latency and has higher throughput than D-RDRAM does. See Table 2.

And DDR-FCRAM outperforms DDR-SDRAM averagely 10% at Windows Boot-up and Paint-Shop-Pro. However, the performance of a DDR-SDRAM is higher than that of DDR-FCRAM 5.6% when Excel program is running because of high page hit ratio exceeding 60% as shown in figure 8.

Because a DDR-FCRAM uses auto-precharge operation, the latency (tRAC) is always constant at page hit or at page miss. However, because DDR-SDRAM doesn't use auto-precharge operation, DDR-SDRAM doesn't need row active command at page hit situation. Therefore DDR-SDRAM is faster than DDR-FCRAM at the application which shows high page hit ratio like a MS-Excel program. See figure 8.

V. CONCLUSION

We implemented POPeye, a system analysis simulator for DRAM performance evaluation in a PC environment. POPeye's processor is modeled to be compatible with Intel Pentium Processor and the other peripherals are based on Intel 440BX chipset.

Software Simulator like POPeye can provide an identical system environment to variable memory systems more easily than hardware emulator can. Moreover, to implement hardware emulator means you have to know the DRAM controller in very detail. But the detailed information of DRAM controller or the Chipset is classified strictly by the company's policies.

Most advantage of POPeye simulator is that it can execute real-life Windows applications. When running real-life application programs such as Microsoft Office or Paint Shop Pro on Windows 95, POPeye simulates detailed transactions between a CPU and a memory system. Using this tool, we comparatively analyzed the performance of a DDR-SDRAM, a D-RDRAM, and a DDR-FCRAM.

A DDR-SDRAM always outperforms D-RDRAM approximately 30% because the latency of a DDR-SDRAM is shorter than that of a D-RDRAM and also the maximum throughput of a DDR-SDRAM is higher than that of a D-RDRAM.

Plus, DDR-FCRAM outperforms DDR-SDRAM about 10% except when MS-Excel program is running. The performance of a DDR-SDRAM is higher than that of a DDR-FCRAM when the page hit ratio exceeds 60%.

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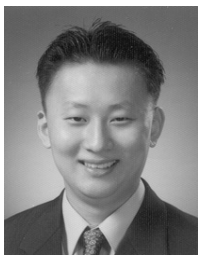

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Dr. Yoo received the 1994 Electronic Industrial Association of Korea Award for his contribution to DRAM technology.