1-Gb/s 80-dBΩ Fully Differential CMOS Transimpedance Amplifier in Multichip on Oxide Technology for Optical Interconnects

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***Abstract*—A 1-Gb/s differential transimpedance amplifier (TIA) is realized in a 0.25-μm standard CMOS technology, incorporating the regulated cascode input configuration. The TIA chip is then integrated with a p-i-n photodiode on an oxidized phosphorous-silicon (OPS) substrate by employing the multi-chip-on-oxide (MCO) technology. The MCO TIA demonstrates 80-dBΩ transimpedance gain, 670-MHz bandwidth for 1-pF photodiode capacitance, 0.54-μA average input noise current, −17-dBm sensitivity for 10^{-12} bit-error rate (BER), and 27-mW power dissipation from a single 2.5-V supply. It also shows negligible switching noise effect from an embedded VCO on the OPS substrate. Furthermore, a four-channel MCO TIA array is implemented for optical interconnects, resulting in less than −40-dB crosstalk between adjacent channels.**

***Index Terms*—Multichip-on-oxide (MCO), optical interconnects, oxidized phosphorous-silicon (OPS), regulated cascode, switching noise, transimpedance amplifier (TIA).**

I. Introduction

SYSTEM-ON-CHIP (SoC) enables integration of high-speed analog and digital circuits in a single chip, providing low-power and low-cost solutions.However, it exhibits inherent substrate coupling noise between high-fidelity analog circuits and noisy digital logic. As the operating frequency (or bit rate) increases, the substrate noise becomes very severe and significantly deteriorates the system signal-to-noise ratio (SNR) or bit-error rate (BER). Gigabit optical receivers are a typical example.

Fig. 1 illustrates an optical receiver system, which consists of a transimpedance amplifier (TIA), a post-amplifier, a clock and data recovery circuit with an embedded voltage-controlled oscillator (VCO), and a digital demultiplexer. Among these blocks, the front-end analog TIA is the most critical and sensitive element in terms of noise. Therefore, the design mandates careful optimization not only to minimize the amplifier noise itself, but also to reduce the switching noises from digital circuitry coupled through common substrate.

In general, differential configurations provide better immunity to common-mode noises, such as power supply noise or substrate coupling noise, than single-ended. However, a number of design challenges exist in the differential configurations, particularly for optical front-end TIA designs. First, a dummy capacitor, which is often added to the negative input to balance the photodiode capacitance [1], is not cost or size effective, especially when considering the applications of parallel optical interconnects. Second, the chip layout requires very careful matching in order to minimize the offset. Third, differential circuits dissipate almost twice the power and yield nearly 3 dB worse noise than single-ended. Nevertheless, differential configurations are adopted in this work since the need of a dummy capacitor can be efficiently avoided by incorporating the current-mode regulated cascode (RGC) circuit technique [2]–[4]. Also, a multichip-on-oxide (MCO) technique is employed as a multichip module (MCM) in order to relax the substrate coupling noise effect.

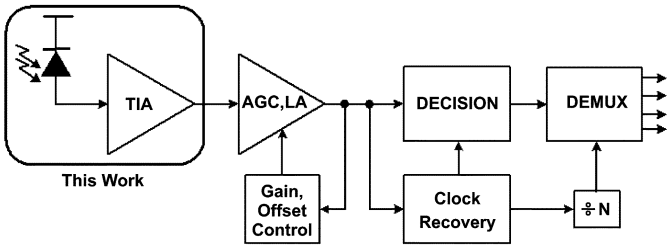

Fig. 1. Overview of optical receiver system.

Section II describes the mechanism of the RGC input and the design of a differential RGC TIA. The measured results of the RGC TIA in the MCO technology and the digital switching noise effect on the analog TIA are discussed in Section III.

II. Differential Regulated Cascode TIA

It is well known that tradeoffs between bandwidth and photodiode capacitance are inevitable in a conventional common-source TIA. Even though common-gate (CG) input configuration helps a TIA to relax the tradeoffs, it cannot yet effectively isolate the large photodiode capacitance from the bandwidth determination because of small g_m of the input transistor. Meanwhile, the RGC input configuration reported in [2]–[4] enhances the input g_m significantly due to the local feedback mechanism, so that the RGC TIA can achieve better isolation of the photodiode capacitance than other configurations. Namely, the RGC circuit enables the TIA to avoid the need of a dummy input capacitor due to the virtual-ground input impedance, thus facilitating the realization of an optical interconnect system in a single chip. Also, the virtual ground input reduces the noise coupling from $V_{\rm DD}$ through the photodiode into the TIA so much that there is no longer a need to balance it out. Furthermore, proper sizing of the local feedback stage reduces the dominant high-frequency noise contribution of the RGC TIA without deteriorating the stability [4].

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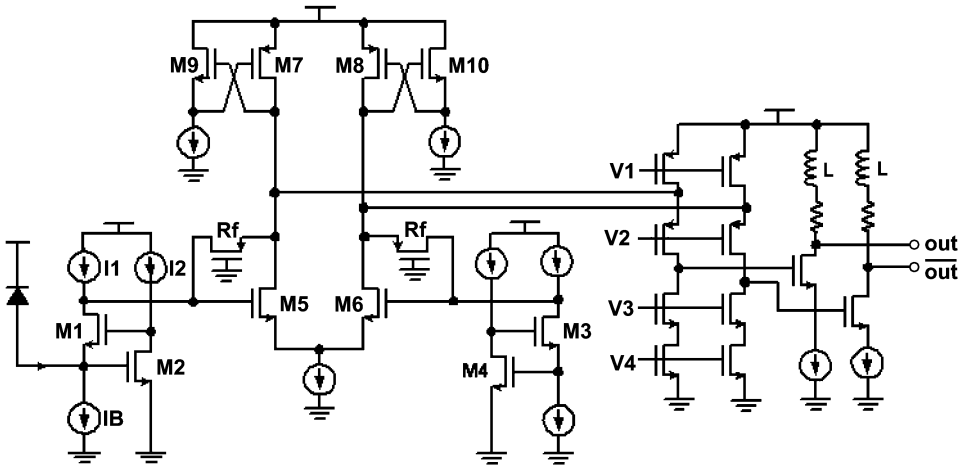


Fig. 2. Schematic diagram of a differential regulated cascode TIA.

Fig. 2 shows the schematic diagram of a differential RGC TIA, which comprises the RGC input stage, the second voltage-gain stage with threshold-voltage loss compensation (TLC) loads [5], and the output buffer with shunt-peaking inductor loads. In the TLC loads, each pMOS M_7 and M_8 is cross-connected to source followers M_9 and M_{10}, respectively. Thereby, the threshold-voltage V_{th} loss of the pMOS loads is compensated and the output voltage at drains can swing up to V_{DD}. If $V_{GS9,10} \approx V_{\mathrm{th}7,8}$, the pMOS loads operating in ohmic region result in small signal resistance of $1/g_{m7,8}$ [5].

The feedback resistor $\mathrm{R_f}$ is applied to the drain of M_1 owing to the efficient current buffer operation of the RGC input [4]. It is also fed back from the drain of M_5, which helps to achieve large transconductance (g_{m5}) at low supply voltages and to acquire broadband and low crosstalk characteristics by reducing the node impedance [6]. The short feedback loop would reduce the group-delay variation and thus improve the jitter characteristic of the amplifier. The $\mathrm{R_f}$ is implemented by a linear-mode pMOS in this work.

The output buffer consists of a dc level-shifter and a current-mode-logic (CML) with shunt-peaking inductor loads. The level shifter is designed as a folded-cascode amplifier not only to shift the dc levels but also to boost the voltage gain further. Since the level-shifter may reduce the bandwidth, inductive peaking technique is incorporated at the CML output stage in order to compensate the possible reduction of the bandwidth [7].

This work shares the basic configuration with the previous single-ended RGC TIA in [4], and thus, the -3-dB bandwidth is approximately given by

$$f_{-3\,\mathrm{dB}} \cong \frac{(1+g_{m5}/g_{o7})}{2\pi R_f[C_{d1}+C_{g5}+C_f(1+g_{m5}/g_{o7})]} = \frac{1}{2\pi R_f\left[\left(\dfrac{C_{d1}+C_{gs5}}{1+g_{m5}/g_{o7}}\right)+C_{gd5}+C_f\right]} \quad (1)$$

where C_{d1} is the drain capacitance of M_1, C_{g5} is the gate capacitance of M_5, i.e., $C_{g5} \approx C_{gs5} + C_{gd5}(1+g_{m5}/g_{o7})$, C_{f} is the parasitic capacitance of the feedback resistor, and g_{o7} is the output conductance of M_7.

Noise analysis shows that the equivalent noise current spectral density is approximately given by

$$\begin{aligned}\overline{i_{\mathrm{eq}}^2} &\cong 4kT\Gamma g_{m,Rf} + 4kT\Gamma(g_{m,IB}+g_{m,I1}) \\ &\quad + \frac{4kT\Gamma(g_{m2}+g_{m,I2})\omega^2(C_{\mathrm{in}}+C_{gs2}+C_{sb1}+C_{d,IB})^2}{(g_{m2}+g_{o,I2})^2} \\ &\quad + \frac{4kT\Gamma(g_{m1}+g_{m,Rf}+g_{m,I1})\omega^2(C_{gs1}+C_{gd2})^2}{g_{m1}^2} \\ &\quad + \frac{4kT\Gamma(g_{m5}+g_{m7})\omega^2(C_f+C_{g5}+C_{d1})^2}{g_{m5}^2} \end{aligned} \quad (2)$$

where k is the Boltzmann constant, T is the absolute temperature, Γ is the noise factor of the MOSFET, C_{in} is the input parasitic capacitance including photodiode capacitance, ESD protection diode capacitance, and bond-pad parasitic capacitance, i.e., $C_{\mathrm{in}} = C_{pd}+C_{\mathrm{ESD}}+C_{\mathrm{pad}}$, C_{sb1} is the source–bulk capacitance of M_1, and $C_{\mathrm{d,IB}}$ is the drain capacitance of the current source I_{B}.

The minimum noise current of the TIA is obtained by satisfying three conditions: 1) $C_{gs2} \cong C_{\mathrm{in}} + C_{\mathrm{sb1}} + C_{d,\mathrm{IB}}$; 2) $C_{gs1} \cong C_{gd2}$; and 3) $C_{g5} \cong C_{d1} + C_f$. Here, the gate widths of M_1, M_2, and M_5 are designed to be 45 μm, 100 μm, and 50 μm, respectively. Yet, further optimization is necessary to achieve proper power allocation between the RGC input stage and the second voltage-gain stage, thereby improving the sensitivity and bandwidth performance.

III. Measured Results of Differential RGC TIA

Test chips of the differential RGC TIA were implemented in a 0.25-μm standard CMOS technology with a single poly and five metal layers. The core area occupies 0.13×0.16 mm^2. ESD protection diodes with parasitic capacitance of 0.7 pF are integrated in all pads. The TIA chip is then integrated with a 250×350 μm^2 GaAs p-i-n photodiode and a couple of planar spiral inductors on an oxidized phosphorous-silicon (OPS) substrate by incorporating the MCO technology.

The MCO technique enhances the electrical isolation characteristics between noise-susceptible analog circuits and noisy

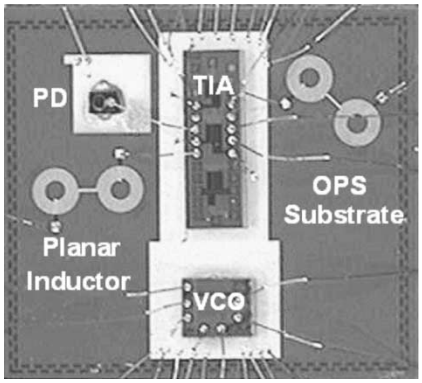


Fig. 3. Microphotograph of the MCO TIA.

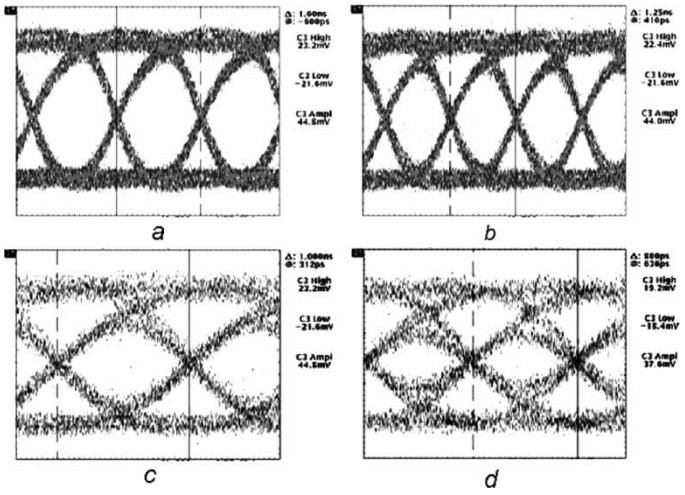


Fig. 4. Measured optical eye diagrams of the MCO TIA for $2^{31}-1$ PRBS with different bit rates: (a) 622 Mb/s; (b) 800 Mb/s; (c) 1 Gb/s; and (d) 1.25 Gb/s.

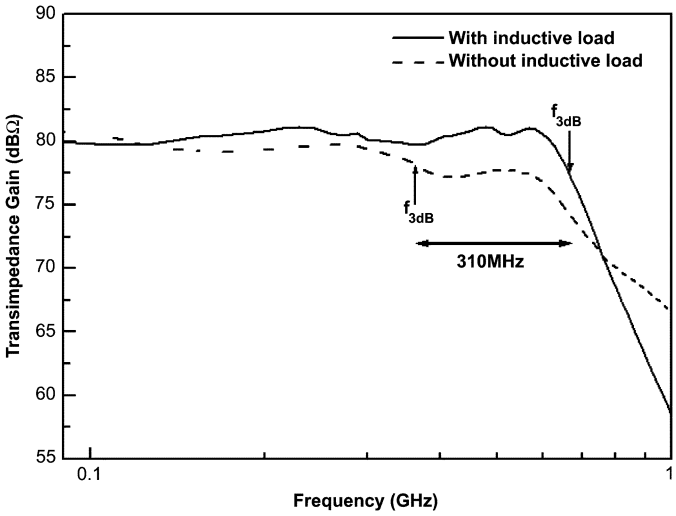


Fig. 5. Electrically measured frequency response of the RGC TIA.

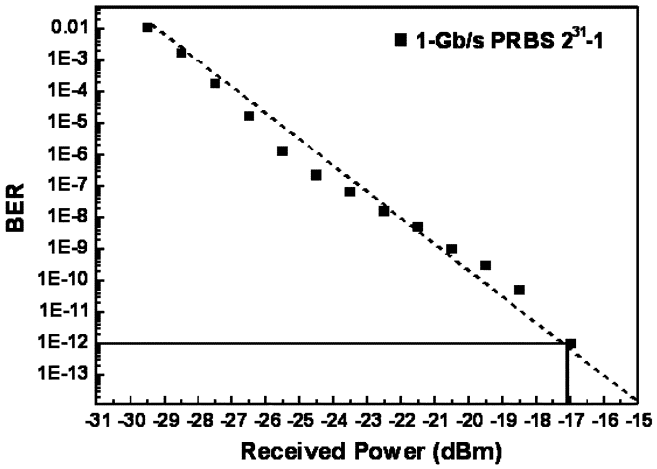


Fig. 6. Measured optical sensitivity of the MCO TIA for 1-Gb/s $2^{31}-1$ PRBS.

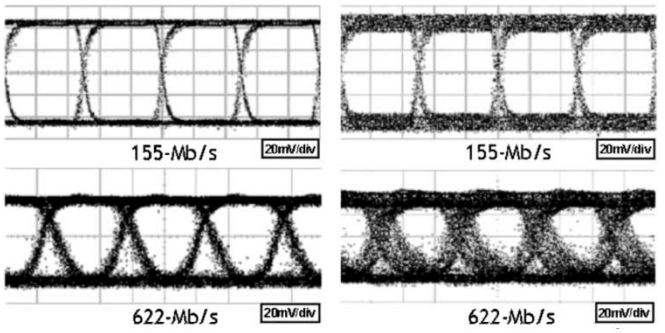
digital logic, and hence, results in significant reduction of substrate coupling noise [8]. It also provides good thermal conductivity. Fig. 3 shows the microphotograph of the fabricated MCO TIA (occupying the area of 5×5 mm^2).

For optical measurements, a low-cost 850-nm VCSEL diode and the p-i-n photodiode are utilized as a light source and an optical detector, respectively. The photodiode yields the responsivity of 0.6 A/W at 850 nm with parasitic capacitance of 1 pF and parasitic resistance of 25 Ω. Fig. 4 shows the measured optical eye diagrams of the MCO TIA at different data rates of 622-Mb/s, 800-Mb/s, 1-Gb/s, and 1.25-Gb/s $2^{31}-1$ PRBS. It is clearly seen that wide eye openings are obtained up to 1-Gb/s operations.The maximum voltage swing is measured to be 200 m$V_{\rm pp}$ in a single-ended output. The peak-to-peak jitter is measured to be less than 176 ps.

Electrical measurements were also conducted to measure the frequency response of the differential RGC TIA. To facilitate the measurements, the TIA chip was mounted on an FR-4 PC-board test fixture with the equivalent circuit of a 1-pF photodiode [3]. Then, the test module was measured in the frequency range of 10 MHz–1 GHz using an HP8753ES network analyzer with a test power level of -15 dBm. Fig. 5 depicts the measured data, demonstrating 80-dBΩ transimpedance gain and 670-MHz bandwidth for 1-pF photodiode capacitance. The bandwidth shrinks to 360 MHz with no shunt peaking inductor loads.

The equivalent input noise current spectral density of the differential RGC TIA is measured by using an HP8650A spectrum analyzer and a wide-band low-noise amplifier (LNA) in the frequency range of 10 MHz–700 MHz. The average noise current of 0.54 μA is achieved, which corresponds to the sensitivity of -21 dBm for a BER of 10^{-12} with the extinction ratio of 9 dB. However, the optical sensitivity of the MCO TIA is measured to be -17 dBm for 10^{-12} BER with 1-Gb/s $2^{31}-1$ PRBS, as shown in Fig. 6. This 4-dB discrepancy may be attributed to the sensitivity of the wide-band LNA, the coupling loss between fiber and the p-i-n photodiode, and the unwanted lights from surrounding environment.

The digital switching noise effect on the sensitive analog TIA is also examined. For this purpose, a VCO was integrated with the differential RGC TIA on both an OPS substrate and a silicon substrate, because the VCO is one of the main sources of switching noise and jitter degradation in optical receiver systems. The VCO was designed as a three-stage self-biased ring oscillator [9]. Then, the substrate coupling noise effect was investigated from the output eye diagrams of both TIAs.



(a) (b)

Fig. 7. Measured digital switching noise effect on the eye diagrams of the RGC TIA on (a) MCO OPS substrate and on (b) SoC silicon substrate with VCO switched on at different data rates of 155 and 622 Mb/s.

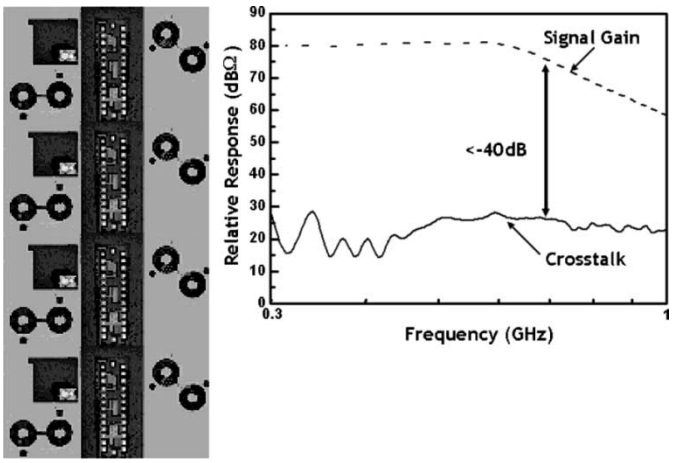


Fig. 8. Microphotograph of the four-channel RGC TIA array on OPS substrate and its measured electrical crosstalk between adjacent channels.

Fig. 7 shows the measured eye diagrams when the VCO is switched on at different data rates of 155 Mb/s and 622 Mb/s. It is clearly seen that little degradation of the eye diagrams is detected in the MCO TIA, whereas the performance of the high-speed mixed-mode SoC is considerably deteriorated due to the high conductivity of silicon substrate. These results confirm that the MCO technology can effectively mitigate the substrate coupling noise in high-speed mixed-mode circuits. DC measurements show that the MCO TIA module dissipates 27 mW from a single 2.5-V supply.

Furthermore, a four-channel MCO TIA array was implemented on an OPS substrate for the applications of parallel optical interconnects. Fig. 8 shows the chip microphotograph of the array, where each channel incorporates the differential RGC TIA. Electrical measurements reveal that the MCO TIA array achieves less than −40-dB crosstalk between adjacent channels within the bandwidth. The performance of the MCO TIA is summarized in Table I.

TABLE I
PERFORMANCE SUMMARY OF THE MCO TIA

Supply voltage	2.5V
Power dissipation	27mW
Bandwidth (-3dB)	670MHz
Photodiode capacitance	1pF
Optical sensitivity for 10^{-12} BER	-17dBm
Transimpedance gain	80dBΩ (differential)
Max. output voltage swing (single-ended)	$200mV_{pp}$
Chip area	$0.13x0.16mm^2$ (RGC TIA core) $5x5mm^2$ (MCO TIA)
Technology	0.25μm standard CMOS

IV. CONCLUSION

A 1-Gb/s fully differential RGC TIA has been implemented in a 0.25-μm standard CMOS technology for parallel optical interconnects. Employing the MCO technology, the TIA chip is integrated with a p-i-n photodiode and planar inductors on an OPS substrate. The MCO TIA achieves the transimpedance gain of 80 dBΩ, the sensitivity of −17 dBm for the BER of 10^{-12}, the interchannel crosstalk of less than −40 dB, and negligible digital switching noise effect. The MCO TIA module dissipates 27 mW from a single 2.5-V supply.

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