A 0.24-nJ/b Wireless Body-Area-Network Transceiver With Scalable Double-FSK Modulation

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***Abstract*—An energy-efficient wireless body-area-network (WBAN) transceiver is implemented in 0.18-μm CMOS technology with 1-V supply voltage. For the low energy consumption, the body channel communication (BCC) PHY is utilized with the theoretical results of Maxwell's equation analysis behind the BCC. Based on the channel analysis, the resonance matching (RM) and contact impedance sensing (CIS) techniques are proposed to enhance the quality of the body channel. A double-FSK modulation scheme is adopted with high scalability to fulfill the IEEE 802.15.6 Task Group specifications. In addition, a low-power double-FSK transceiver is implemented by five circuit techniques: 1) a reconfigurable LNA with CIS; 2) a current-reuse wideband demodulator; 3) a divider-based local oscillator (LO) generation with duty-cycle correction in the receiver; 4) a reconfigurable driver with RM; and 5) a divider-based digital double-FSK modulator in the transmitter. As a result, fully WBAN compatible receiver and transmitter consume 2.4 and 2 mW, respectively, at a data rate of 10 Mb/s, corresponding to energy consumption of 0.24 nJ per received bit and 0.2 nJ per transmitted bit.**

***Index Terms*—Body-area network (BAN), body-channel communication (BCC), channel analysis, current-reuse, double-FSK, duty cycle correction, energy-efficient, FSK, FSK demodulator, FSK modulator, low energy, low power, transceiver, wireless body-area network (WBAN).**

I. Introduction

WIRELESS body-area networks (WBANs) are an emerging technology that can combine healthcare and consumer electronic applications around the human body. By continuously connecting and sharing the information around the human body, WBANs are expected to bring new convenient usages and application services to mobile devices. Since the WBAN is the network around the human body, there are stringent requirements associated with WBAN transceivers such as energy efficiency, interference rejection, low cost, quality-of-service (QoS) scalability, network coexistence, safety, and so on, according to IEEE 802.15.6 Task Group for WBAN standardization [1]. Three physical layers (PHYs) are mainly considered in the WBAN standardization: ultra-wideband (UWB) PHY, narrowband (NB) PHY, and body-channel communication (BCC) PHY. The BCC, which uses the human body as a communication channel, has advantages over UWB and NB because of high conductivity of the human body compared with that of air. In addition, not only most of the signal from the transmitter is confined to the body area without interference from external RF devices, but also the communication frequency can be lowered by using electrode without the need of large size antenna. These reduce the power consumption of BCC transceivers [2] compared with the conventional RF approaches [3]–[5], as shown in Fig. 1, which depicts the power consumption and the data rate of UWB, NB (Bluetooth and Zigbee), and BCC transceivers in recent publications. In addition, due to the energy absorption in the human tissue, UWB and NB signals around the human body significantly suffer from huge path loss, and their channel characteristics strictly depend on the locations in the human body [6]. Therefore, the BCC is one of the most promising energy-efficient candidates to WBAN PHY.

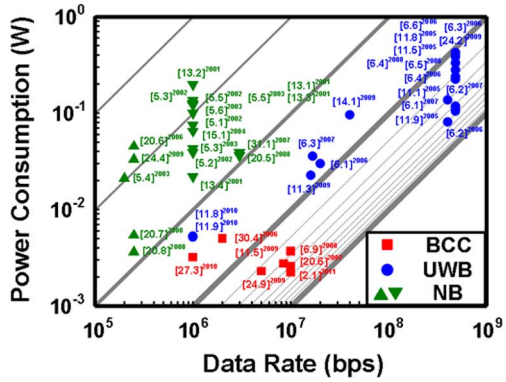

Fig. 1. Energy efficiency of the UWB, NB, and BCC transceivers.

There have been various studies to investigate the mechanism of sending and receiving data through human body and to model the channel for the BCC [7]–[9]. From these channel characterizations, each channel model is adequately employed to implement the BCC transceiver [10]–[14]. For example, first-prototyped direct digital wideband signaling (WBS) transceiver [10] is based on the simple phenomenological circuit model [7]. By adopting the improved empirical circuit model [8], a direct-sequence spread spectrum (DSSS) pulse-position modulation (PPM) transceiver [11] and adaptive frequency hopping (AFH) frequency-shift keying (FSK) transceiver [12], [13] are implemented with the low energy consumption. In addition, a correlation-based direct digital transceiver [14] depends on the phenomenological statistical behavior model [9]. However, previous BCC transceivers were not optimized for WBAN because

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the only phenomenological circuit/behavior models were used for the body-channel analysis, which means there was not a clear understanding of the on-body electric signal transmission mechanism. Moreover, they were unable to satisfy WBAN requirements such as energy efficiency, scalability of QoS, interference mitigation, and network co-existence simultaneously.

In order to provide a clear understanding of the transmission mechanism, from the general solution of Maxwell's equation analyzed in [15], we can obtain the electric field intensity near the human body as follows:

$$|E|_{\mathrm{BCC}} \approx a_1 \cdot |E|_{\text{quasi-static}} + a_2 \cdot |E|_{\text{surface wave}} = a_1 \cdot \frac{2}{k} \cdot \frac{1}{r^3} + a_2 \cdot 2k \cdot e^{-a_s kr} \cdot \frac{1}{r} \quad (1)$$

where a_1, a_2, and a_s are coefficients, the wave number is $k = 2\pi/\lambda$, and λ is the corresponding wavelength of the operating frequency. Consequently, the mechanism of BCC can be divided into two parts: the quasi-static near-field coupling of the first term and the surface wave far-field propagation of the second term. The intensity of the electric field is a function of communication distance and wavenumber. As the wavenumber k or frequency f and the distance r increase, the surface wave propagation term has significant effect on the overall electric field intensity whereas the quasi-static coupling term is negligible and vice versa.

In this paper, we propose a BCC transceiver that not only consumes the lowest energy but also fulfills the IEEE 802.15.6 Task Group specifications. It is possible by the theoretical analysis of physics behind the BCC which leads to the optimization of electric signal transmission through the human body. Based on (1), resonance matching (RM) and contact impedance sensing (CIS) are proposed for the sake of power reduction of the transceiver. In addition, for the full satisfaction of WBAN requirements, we adopt a double-FSK modulation scheme in combination with low-power circuit techniques such as a reconfigurable LNA/driver, current-reuse wideband demodulation, divider-based LO generation with duty-cycle corrector, and a divider-based modulator. Thanks to these features, a fully WBAN compatible receiver and transmitter consume 2.4 and 2 mW, respectively, at a data rate of 10 Mb/s, which corresponds to energy consumption of 0.24 nJ per received bit and 0.2 nJ per transmitted bit.

The remainder of this paper is organized as follows. Section II explains the energy-efficient WBAN transceiver design in terms of system-level techniques. After that, Section III describes the overall transceiver architecture with circuit-level techniques. Detailed designs of the building blocks are explained in Section IV. The implementation results will be shown in Section V. Finally, Section VI concludes the paper.

II. Energy-Efficient WBAN Transceiver Design

A. Resonance Matching (RM)

Based on the signal propagation mechanism of the BCC [15], channel enhancement method can be obtained. The signal transmission mechanism of BCC can be divided into

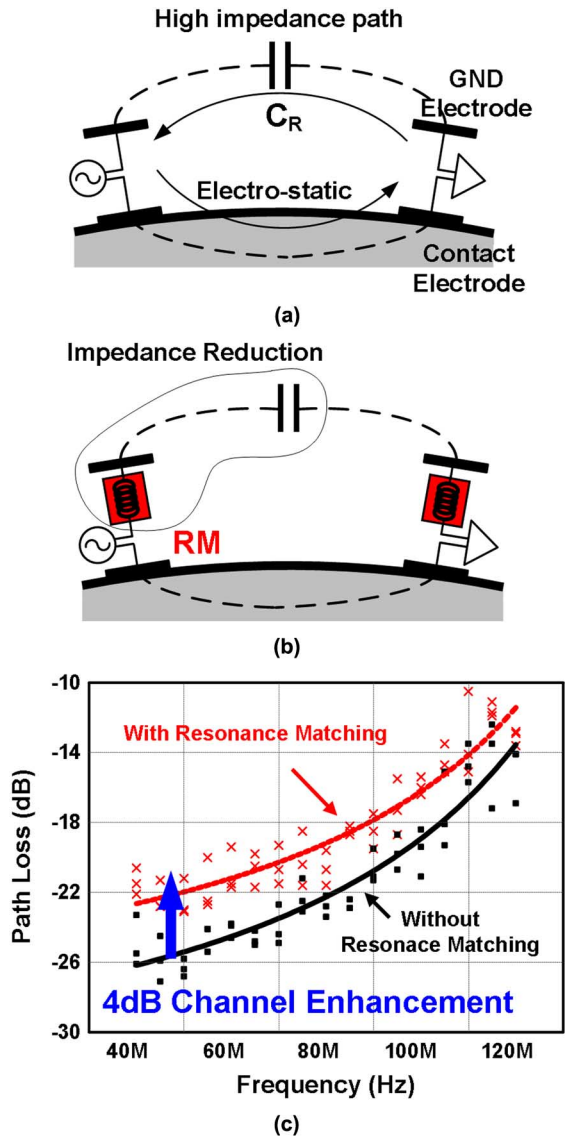


Fig. 2. Enhancing quasi-static coupling mechanism. (a) Quasi-static coupling mechanism. (b) RM technique. (c) Channel enhancement by RM.

quasi-static coupling and surface wave propagation as explained in Section I. At a frequency less than tens of megahertz whose wave length is much larger than the size of the human body, the electric field around the human body is almost constant with time, which means that its phase is nearly uniform everywhere on the body. In this condition, the time-varying electric field around the human body can be regarded as a quasi-static field. The quasi-static assumption simplifies the analysis by only considering the voltage and current on the human body. The human body can be approximated as a conducting wire in this frequency range, and a complete closed loop should be formed for the signal transmission. Therefore, the return signal is transferred onto the human body through capacitive near-field coupling mechanism. Since the closed-loop signal path of the electric field is provided by electrostatic coupling between GND electrodes of transmitter and receiver, the body channel has been modeled with the capacitor circuits, as shown in Fig. 2(a). The signal path loss is mainly determined

by the capacitive impedance because the small capacitance of C_R has the highest impedance value compared with the contact impedance. In order to enhance the quasi-static coupling mechanism, RM, inserting a resonating series inductor between GND electrodes of transmitter and receiver, is proposed as represented in Fig. 2(b). Around the resonance frequency formed by RM network and C_R, the impedance between transmitter and receiver can be significantly reduced. Fig. 2(c) shows the measured path loss by shorting the contact electrodes between the transmitter and receiver with and without the RM technique. The RM gives 4-dB channel enhancement. Therefore, a high signal-to-noise ratio (SNR) can be achieved in RX with the same transmitter's power consumption, which reduces circuit power consumption of the transmitter for the same SNR at the receiver input.

B. Contact Impedance Sensing

The surface-wave propagation mechanism starts to predominate over quasi-static mechanism in frequencies higher than tens of megahertz. In this frequency range, the electric signal attenuates as the signal propagates through the surface of the human body as shown in Fig. 3(a). There are lots of factors that can affect the channel response between the transmitter and receiver. Among them, the most influential factor is the distance between contact electrode and the human body, which is even more influential than the distance between the transmitter and receiver. Since most of the surface wave signal is confined to the surface of the body [15], we should consider the distance or impedance between the contact electrode and the human body as shown in Fig. 3(c). Fig. 3(c) plots the measurement results of channel variation in terms of the contact impedance variation using a circular electrode with 1.5-cm diameter. The indexes of resistive and capacitive impedance in the right part of Fig. 3(c) mean that the electrode is contacted to and apart from the human body, respectively. The contact impedance between the electrode and the human body varies its value dynamically, and even 30-dB overall signal path loss variation is observed when the electrode is in contact with or apart from the body. Such a dynamic variation makes the receiver consume significant power because the receiver should additionally satisfy not only the high-linearity requirement in case 1 but also the high-sensitivity requirement in case 2 of Fig. 3(c), at once. To compensate for channel quality degradation, and to mitigate the additional linearity and sensitivity requirement caused by the contact impedance variation, we employ the CIS technique as shown in Fig. 3(b). By means of detecting the impedance variation between the electrode and the human body, CIS automatically determines the operation mode of the receiver for better power efficiency. As a result, the receiver does not have to satisfy the high-linearity and high-noise performances simultaneously, which significantly reduces the circuit power dissipated by the receiver.

C. Double-FSK Modulation

From bio-signal (e.g., ECG, EEG, and EMG) sensing to video/medical imaging applications, WBAN requires high scalability of QoS, data rate, BER, and network coexistence with low energy consumption and low system cost. For example, in a 16-channel EEG sensing application, when a 12-bit

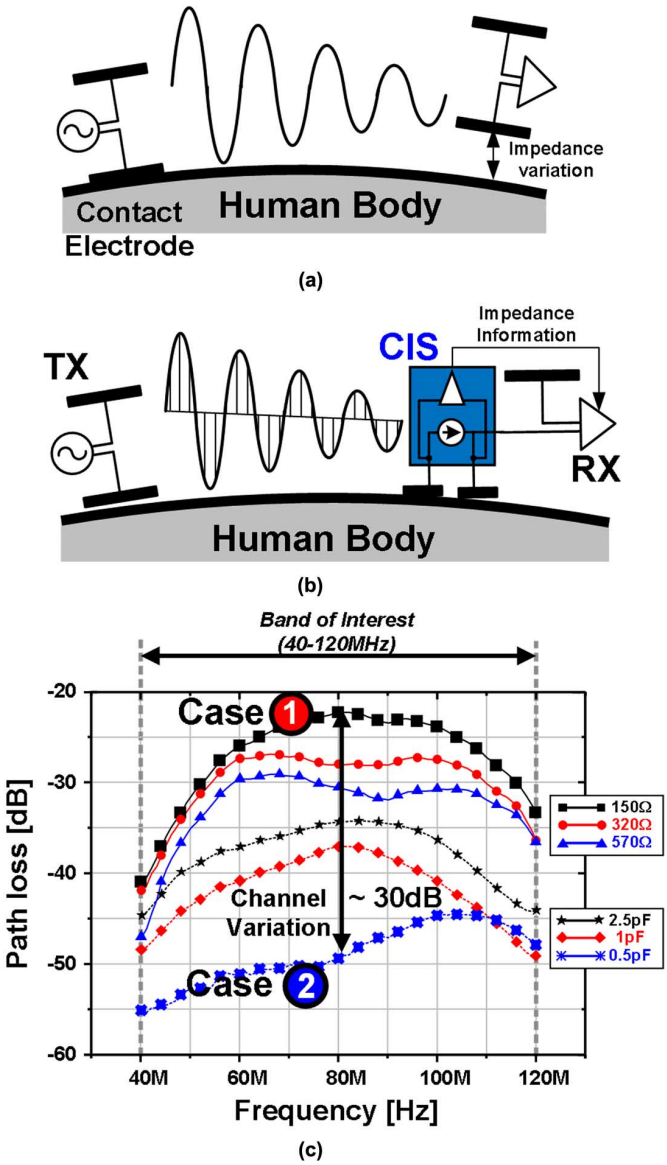


Fig. 3. Enhancing surface-wave propagation mechanism. (a) Surface-wave propagation mechanism. (b) CIS technique. (c) Channel quality degradation due to the contact impedance variation.

ADC with 300-Hz sampling is used, the data rate of 57.6 kb/s and BER of less than 10^{-10} should be supported with a network coexistence of 16. On the other hand, for the video/medical imaging application, 10-Mb/s transmission with 10^{-3} BER is required without the need for network coexistence. To fulfill the IEEE 802.15.6 Task Group specifications of the data rate (10 kb/s–10 Mb/s), BER (10^{-10}–10^{-3}), and network coexistence (1–15) [1], a scalable double-FSK modulation scheme is adopted. It is based on UWB-FM [16] and an analog version of DSSS. Fig. 4 shows the block diagram of the double-FSK transmitter. The subband FSK modulator modulates data with a low modulation index. Then, it is transformed to a high-modulation-index wideband signal by a wideband modulator. A ratio between modulation indices plays a role in spreading gain of DSSS. Multiple users may share the same wideband signal, but distinguish themselves via different subcarrier frequencies in the subband. The number of users, spreading gain, and each

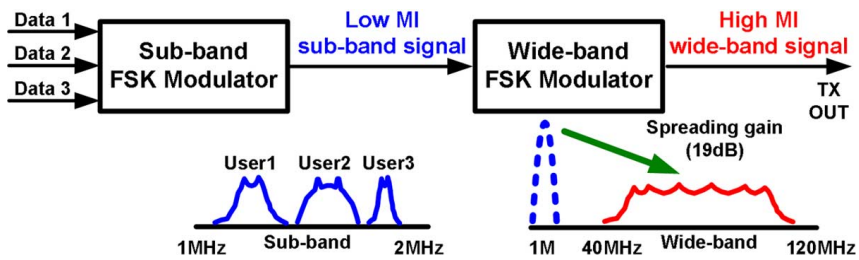


Fig. 4. Double-FSK modulation.

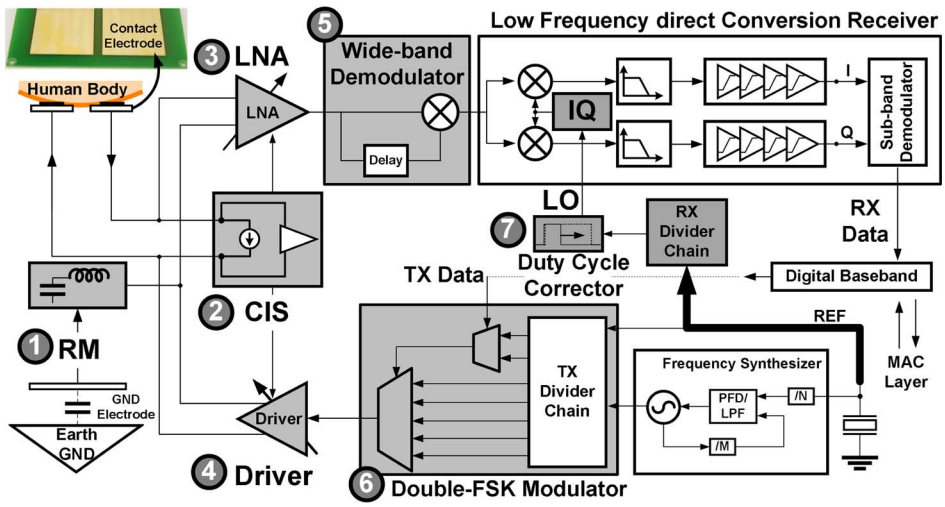


Fig. 5. Overall transceiver architecture.

user's data rate in WBAN can be determined by the choice of the subcarrier, subband frequency, and modulation index of each user. For instance, a low bandwidth of subband permits high spreading gain, whereas a high bandwidth of subband with low-subcarrier modulation index (i.e., low data rate for each user) allows a larger number of users. It is possible to utilize a wideband frequency source with very high scalability. Consequently, by adopting double-FSK modulation, we can satisfy WBAN requirements such as interference rejection, network coexistence, QoS scalability, and safety simultaneously.

In summary, the low-energy WBAN transceiver is designed on the base of the BCC PHY with complete channel analysis. From the analysis, RM for reducing capacitive path impedance and CIS for reducing contact impedance variation are proposed for the power reduction of transmitter and receiver, respectively. In addition, the double-FSK modulation scheme fully satisfies the WBAN requirements.

III. Transceiver Architecture

Fig. 5 shows the overall architecture of the double-FSK transceiver. The BCC uses a 40–120-MHz frequency band for the data transmission while the CIS utilizes a chopper-stabilized ac current–injection source of 1.25 MHz to monitor the differential contact impedance between the contact electrode and the human body. The RM is connected with a GND electrode. On the transmitter side, from the frequency synthesizer and divider chain, the subband FSK modulator modulates the TX data, followed by a wideband FSK modulator that drives the electrodes by the transmitter driver. On the receiver side, from the LNA which amplifies the received signal from the electrodes, the wideband demodulator converts the wideband carrier signal into a subband FSK signal that is demodulated by low-frequency direct-conversion receiver circuits which contain the subband demodulator. Combined with RM and CIS, the double-FSK transceiver has seven low-power circuit techniques: reconfigurable differential LNA/driver, current-reuse wideband demodulator, divider-based digital double-FSK modulator, and divider-based LO generation with duty-cycle corrector.

First, for the power-efficient front-end interface with receiver LNA and transmitter driver, 1) the RM technique reduces the capacitive impedance between GND electrode and Earth ground and 2) the CIS technique reduces the contact impedance variation between the contact electrode and the human body. From the impedance information from CIS, the low-power reconfigurable differential 3) LNA and 4) driver enable transceiver to operate in the better power efficiency.

Second, the wideband demodulator is one of the most important parts of the receiver chain because it should avoid the FM capture effect [17] of multiple frequency-modulated (FM) signals and then simultaneously demodulate multiple FM input signals even though the received signal has a negative SNR. Therefore, the fixed-time-delay FSK demodulator is adopted with frequency-to-phase conversion principle [18]. It is composed of two power-hungry blocks, fixed-delay unit and multiplier. By sharing the bias-current of these two building blocks, 5) current-reuse wideband demodulator decreases its power consumption.

Third, for the low power consumption and high scalability, 6) divider-based double-FSK modulator which consists

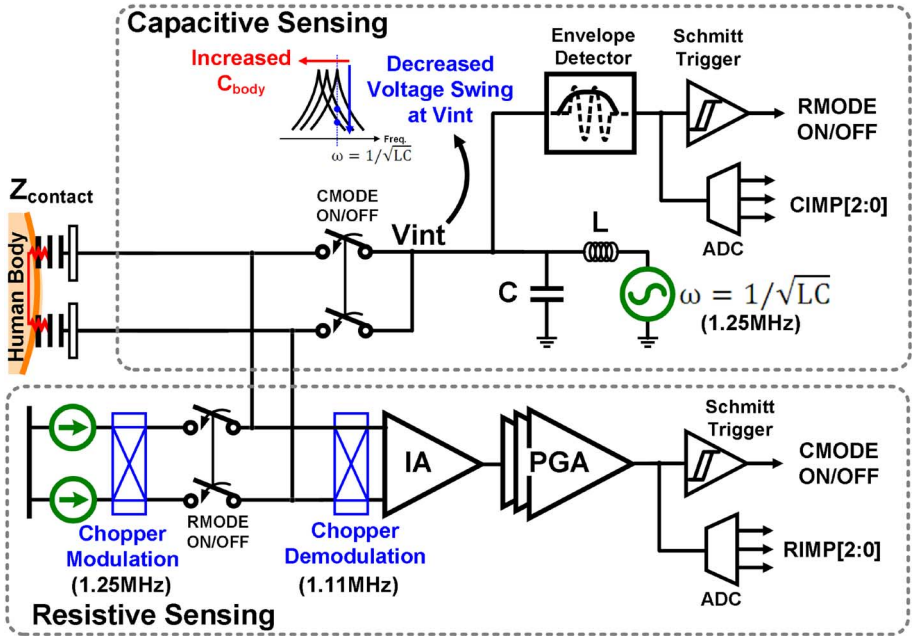


Fig. 6. CIS circuit.

of subband modulator followed by wideband modulator is implemented with simple digital logic gates without any power-consuming analog VCO.

Finally, 7) duty-cycle corrector (DCC) with divider chain replaces the high power frequency synthesizer for the LO generation. The reference clock source (REF) is divided to obtain a LO signal for the low-frequency direct-conversion receiver. It is possible because the subband signal, which is demodulated by wideband demodulator, is located in a low-frequency band below 20 MHz. Meanwhile, the output of divider chain should have an exact 50% duty cycle to generate an accurate I/Q signals. However, the LO signal generated by programmable divider such as pulse-swallow divider cannot guarantee 50% duty cycle. Therefore, the low power DCC circuit is adopted with programmable divider chain for I/Q signal generation without the help of frequency synthesizer.

IV. Transceiver Implementation

A. CIS Circuit

The architecture of CIS circuit is shown in Fig. 6, which is composed of capacitive sensing and resistive sensing part. The capacitive sensing detects the noncontact distance between the human body and the contact electrode. On the other hand, the resistive sensing monitors the resistive contact impedance between the electrode and human body when the electrode is in contact with the human body. The capacitive sensing uses an *LC* network with a frequency source to detect the variation of capacitive impedance from the human body to adjust the transceiver operation modes and to activate the resistive sensing mode. Likewise, the resistive sensing injects the ac current to the differential contact electrodes to evaluate the resistive contact impedance, and to turn the capacitive sensing on.

Since the contact impedance (Z_{contact}) between the human body and the electrode varies as the frequency increases, the measurement of contact impedance should be covered over the frequency range of BCC data transmission, 40–120 MHz, for the accurate impedance value and mode control. Therefore, the ac current injection source in the resistive sensing and the voltage source in the capacitive sensing need to inject the signal into human body by means of frequency near 40–120 MHz. However, these injected signals may play a role as the severe interferer to the BCC data transmission. To isolate the frequency of injection signal from 40 to 120 MHz, we measure the frequency response of the contact impedance, and it is found that if the frequency of the injection signal is higher than 1 MHz, the contact impedance value can be guaranteed to be within the margins of 3% error, compared with impedance in the frequency of the data transmission. Consequently, the injection frequency of 1.25 MHz is utilized to monitor the contact impedance.

By utilizing 1.25 MHz as the injection frequency, the voltage source with *LC* network ($L = 5\ \mu\mathrm{H}, C = 3.2$ nF, or $1/2\pi\sqrt{LC} = 1.25$ MHz) generates the voltage pulse in the capacitive sensing. The resonance frequency of the *LC* network is affected by the capacitance between the human body and the electrode. If the capacitance between the human body and electrode increases, the voltage swing at Vint node decreases because the resonance frequency of $L(C + C_{\mathrm{contact}})$ decreases. The envelope detector senses the amplitude information of the Vint node, and then ADC outputs the 3-bit digital code according to capacitive impedance value. In the resistive sensing, a chopper-modulated ac current injection source of 1.25 MHz is utilized with a chopper-demodulated frequency of 1.11 MHz to shift the signal frequency to 140 kHz for the low-power operation. Followed by instrument amplifier (IA) of 24-dB voltage gain and programmable gain amplifier (PGA) which has voltage gains of 10, 14, 17, and 20 dB with 2-bit gain control, the ADC outputs the 3-bit digital code equivalent to the resistive impedance value. The capacitive sensing and

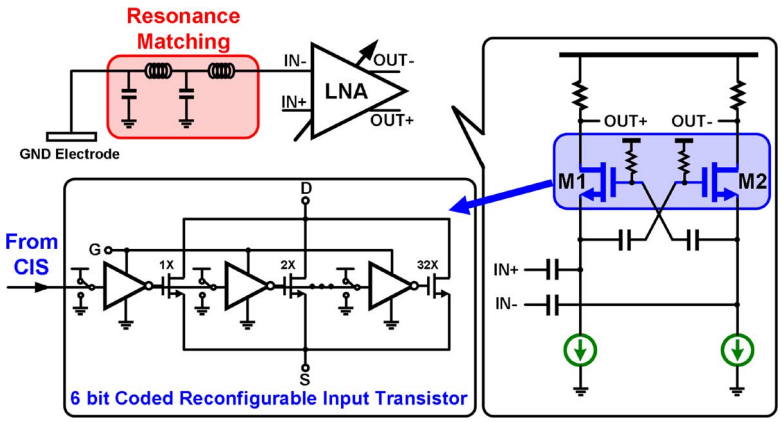


Fig. 7. Reconfigurable LNA.

resistive sensing can detect the capacitance up to 2 nF, and the resistive impedance with a resolution of 87.5 Ω in the range of 100–800 Ω, respectively, both consuming only 20 μW.

B. Reconfigurable LNA and Driver With RM and CIS

Fig. 7 shows the fully differential reconfigurable LNA in the receiver. As a resonance matching, the dual-resonance network at GND electrode is matched over the wide frequency range of 40–120 MHz. The capacitively cross-coupled common-gate LNA reduces the noise factor and increases the effective transconductance of the input transistor with decreased power consumption compared with the conventional common-gate and common-source LNA [19]. Moreover, it provides low impedance to the series RM network and balances the signal gain between differential inputs. For the high reconfigurability with the 6-bit impedance information from CIS, the noise figure, input-referred 1-dB compression point, and voltage gain of LNA can be adjusted by controlling the size of M1 and M2 with constant bias-current sources. The reconfigurable input transistor should be carefully designed because the signal goes through all of the gate, drain, and source nodes of the M1 and M2. To configure the programmable transistor sizes of M1 and M2, additional reconfigurable inverters whose pull-up path is connected with the gates of the M1 and M2, are added, so that the control signal from CIS cannot have influence on the gate, drain, and source nodes of M1 and M2. The noise figure, 1-dB compression point, and voltage gain of LNA can be varied from 3 to 16 dB, from -18 to -6 dBm and from 13 to 22 dB, respectively, with the power consumption of 0.6 mW. It is noted that the LNA dissipates at least 2 mW to satisfy both the noise figure of 3 dB and the 1-dB compression point of -6 dBm, simultaneously. Thanks to CIS, the LNA does not have to fulfill both the high-linearity and high-noise performance. As a result, the power consumption of LNA can be reduced from 2 to 0.6 mW with 70% saving.

The reconfigurable inverter-based transmitter driver with RM network is depicted in Fig. 8. The inverter-based driver provides high impedance to the parallel RM network. The five bit-coded inverter varies its output power to drive the GND electrode by the control code from CIS. The output voltage swing at 50-Ω load can be controlled from 1 to 6 V for the better power efficiency. With the help of the RM, 4-dB channel enhancement can be achieved with the power reduction of driver from 0.6 to 0.2 mW.

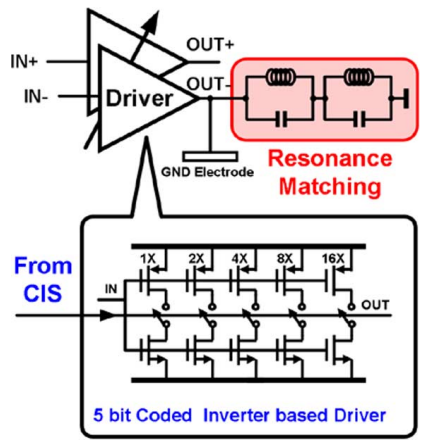


Fig. 8. Reconfigurable driver.

C. Current-Reuse Wideband Demodulator

The fixed-time-delay wideband demodulator is shown in Fig. 9(a). The wideband FSK signal is transformed into a phase-modulated signal by all pass filter (APF). The delayed signal is then fed to the one input of a Gilbert multiplier, where it is multiplied with the nondelayed signal of the other input, yielding the low-frequency subband signal at the output. The output signal of the demodulator has the maximum correlation with the input frequency when the delay time is fixed to the quarter-period $(T/4)$ of the center frequency $(1/T)$ in the wideband signal, where T is the time period of 80 MHz. The group delay (τ) in the delay path is implemented by lattice APF with a phase shift of 90° at the center frequency of 80 MHz. The current-driven lattice APF in Fig. 9(a) has a transfer function as follows:

$$\frac{V_{\mathrm{APF}}}{I_{\mathrm{APF}}}(s) = -2R_{\mathrm{tune}}\frac{s^2-\omega_0^2}{s^2+\dfrac{4\omega_0}{Q}s+\omega_0^2} \tag{2}$$

$$\omega_0 = 1/\sqrt{L_{\mathrm{APF}}(C_{\mathrm{APF}}\|C_{\mathrm{tune}})} \tag{3}$$

$$Q = \omega_0 L_{\mathrm{APF}}/R_{\mathrm{tune}} \tag{4}$$

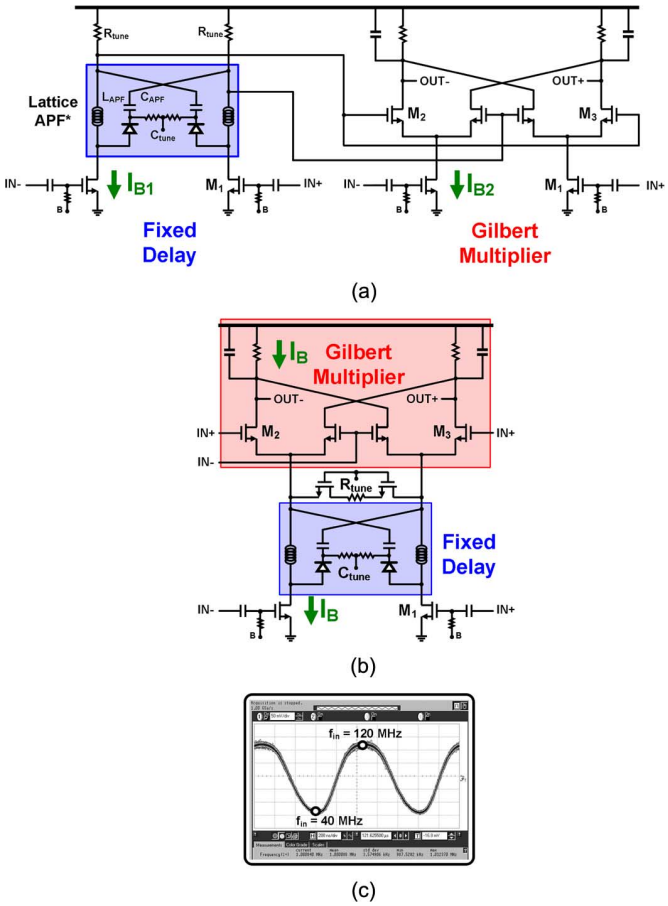


Fig. 9. Wideband FSK demodulator. (a) Fixed-time-delay demodulator. (b) Current-reuse demodulator. (c) Output of the demodulator with 40–120-MHz FM input signal.

$$\tau = \mathrm{Q}/2\omega_0 = L_{\mathrm{APF}}/2R_{\mathrm{tune}}. \tag{5}$$

For the demodulation, the phase shift at the ω_0 from (2) is $-90°$. With the L_{APF} of 270 nH, the C_{tune} and R_{tune} determines the ω_0 and Q-factor of the APF, respectively. To realize the 3.125-ns delay time [1/(4·80 M)], $\mathrm{R_{tune}}$ of 43 Ω is exploited. In the implementation, to avoid frequency offset from the center frequency of 80 MHz in demodulation, the frequency at the phase shift of 90° can be modified by controlling the variable capacitor, C_{tune}. Similarly, to ensure a linear group delay in the operating frequency range with different Q-factor of APF, a variable resistor R_{tune} is used. The bias current I_{B1} should ensure that the filter is effectively current-driven by an input transistor (M1). Furthermore, for the noise and linearity performance of the Gilbert multiplier with preserved gain in the operating frequency, the bias current I_{B2} should be sufficiently large. Due to the wide and high operating frequency of 40–120 MHz, compared with other building blocks, the fixed-delay unit and Gilbert multiplier consume lots of power [20].

To reduce the power consumed by these two blocks, current-reuse wideband demodulator is proposed as shown in Fig. 9(b). The bias current of I_{B} is shared between the Gilbert multiplier and fixed-delay unit by cascoding the APF and multiplier without cascading. Since the multiplier is cascoded with APF through the inductor, there is no additional voltage drop which affects the linearity performance of the demodulator. As a result, the power consumption of demodulator can be reduced by half. The measurement waveform of Fig. 9(c) shows the output of the demodulator with 1-Mb/s 40–120-MHz FM input signal which is generated by external RF signal generator.

D. Divider-Based Double-FSK Modulator

The schematic diagram of double-FSK modulator is shown in Fig. 10. In the conventional modulator in Fig. 10(a), a triangular FSK subband signal (data 0: f0 and data 1: f1) generated by direct digital synthesizer (DDS) modulates the control voltage of VCO in order to output the wideband signal (40–120 MHz). However, the free-running VCO and the output voltage swing of DDS should be regularly calibrated to ensure the correct center frequency of the modulated signal. To get rid of power-consuming wideband VCO and DDS, divider-based double-FSK modulator composed of MUXs and retiming D-flip flops is presented in Fig. 10(b) with the timing diagram. The proposed modulator is implemented with simple digital logic gates without disturbing the VCO control voltage. Hence, the low-power consumption with high QoS scalability can be achieved. From using the frequency synthesizer as a reference, a bit rate of transmitted data, subband carrier frequencies (f0, f1), and wideband frequencies (f40, f60, f80, f100, f120) are provided by a divider chain with a mode control signal. The divider-based double-FSK modulator supports a total of 104 operation modes with data rates from 1 kb/s to 10 Mb/s and the network-coexistence from 1 to 15. Since one TX means one user, the simultaneous FSK modulations of multiple network-coexistence can be achieved by multiple TXs on the human body whereas the simultaneous FSK demodulation is possible by wideband RX demodulator. The mode control logic is implemented with on-chip read-only-memory (ROM). The double-FSK modulator with programmable transmitter divider, digital logic, and ROM consumes a total of 0.6 mW.

E. Duty-Cycle Corrector

To ensure 50% duty cycle, the complementary charge-pump-based DCC circuit is implemented as shown in Fig. 11. The output signal of the programmable divider such as a pulse swallow divider makes the $\mathrm{t_1}$ and $\mathrm{t_2}$ different as represented in Fig. 11. From the mismatch between $\mathrm{t_1}$ and $\mathrm{t_2}$, the complementary charge-pumps detect the imbalance between $\mathrm{t_{out1}}$ and $\mathrm{t_{out2}}$ and convert it into the average voltage V_{P} and V_{N}, which compensate the current of I_{P} and I_{N}, respectively. In the duty cycle correction circuit, during the time period of $\mathrm{t_1}$, I_{P} current flow out from V_{E} node through C_{par}, whereas during the time period of $\mathrm{t_2}$, I_{N} current charges the C_{par} at V_{E} node. Consequently, the voltage of V_{E} node can be expressed as follows:

$$V_{\mathrm{E}} = \frac{1}{C_{\mathrm{par}}}(-\mathrm{t_1}I_{\mathrm{P}} + \mathrm{t_2}I_{\mathrm{N}}) \tag{6}$$

For example, suppose that initially the voltage of V_{P} and V_{N} is the same value, therefore the current I_{P} and I_{N} is also equal. According to (6), the voltage of V_{E} decreases during short time period of t_1, and then it increases for time period of t_2. Therefore, in $\mathrm{CLK_{OUT}}$ signal, the time period of t_{out2} is longer than t_{out1},

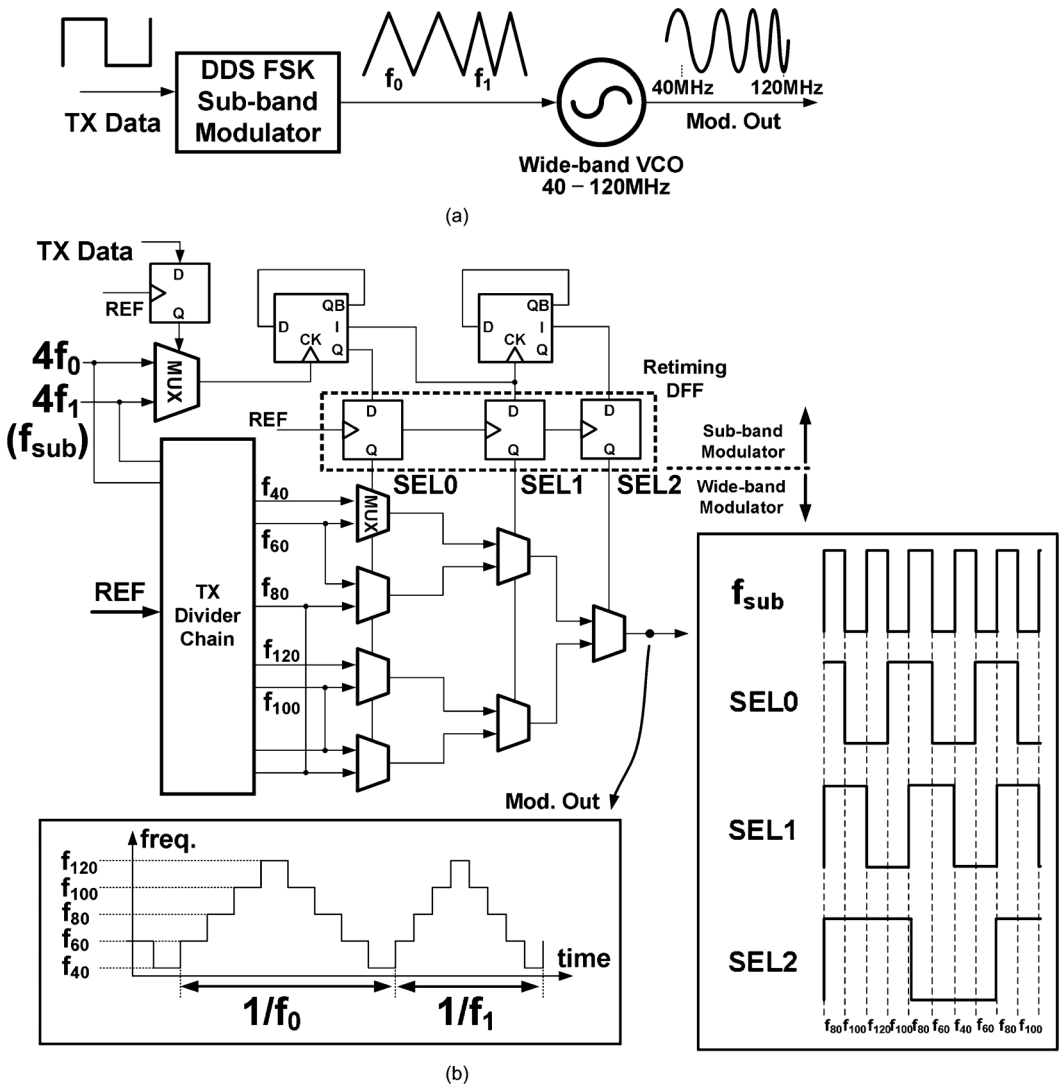


Fig. 10. Double-FSK modulator. (a) Conventional modulator. (b) Divider-based modulator.

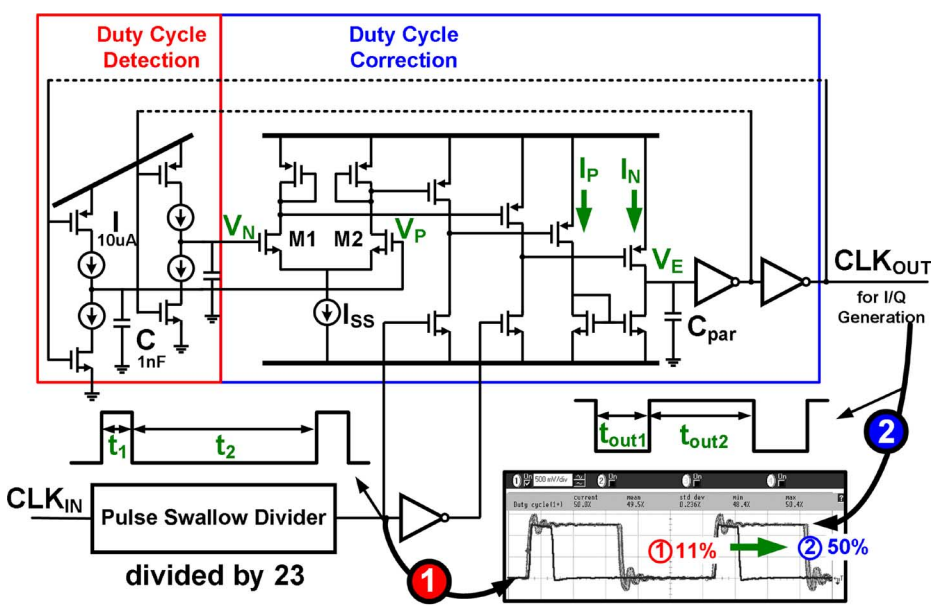


Fig. 11. Charge-pump based duty cycle corrector.

which decreases the voltage of $V_{\rm P}$ and increases the voltage of $V_{\rm N}$. It leads to increased/decreased $I_{\rm P}/{\rm I_N}$. From the negative feedback loop, in the steady state, the time period of $t_{\rm out1}$ and $t_{\rm out2}$ is regulated to be equal by proper $I_{\rm P}$ and $I_{\rm N}$.

The loop dynamics are determined by the loop gain of the duty cycle correction circuit, the current of the charge-pumps, and the capacitance of averaging filter. To suppress the mismatch between $t_{\rm out1}$ and $t_{\rm out2}$, the loop gain of the DCC circuit should be increased enough by the high transconductance of transistors (M1, M2, etc.) and high charge-pump current with small averaging capacitance. In particular, since the output amplitude of the duty cycle detection circuit should be within the proper input common-mode range of the duty cycle correction circuit, the following equation should be satisfied among the charge-pump current (I), averaging capacitor (C), and frequency of the operating signal ($1/T$):

$$I_{\rm SS} + V_{\rm GS1} < \frac{IT}{C} < V_{\rm DD}. \tag{7}$$

In regard to (7), the charge-pump current and the averaging capacitor are set to 10 μA and 1 nF, respectively, in the entire operating frequency range. The measurement waveform shows that when divided-by-23 mode is applied to $\rm CLK_{IN}$ signal, the 11% duty cycle signal is corrected to the 50% duty cycle $\rm CLK_{OUT}$ signal within 0.2 ms. The DCC circuit makes it possible to substitute the power-hungry frequency synthesizer for simple divider chain and DCC. The DCC circuit consumes only 80 μW.

V. Implementation Results

The double-FSK WBAN transceiver is fabricated in 0.18-μm RF CMOS technology, and its chip microphotograph is shown in Fig. 12. The total chip area including pads is 2.5×5.0 mm^2. All circuit operations are measured with a 1-V supply voltage.

Fig. 13 plots the reconfigurable performance of LNA and driver. The noise figure of LNA can be adjusted by 6-bit control code, from 3 to 16 dB, corresponding to a 1-dB compression point from -18 to -6 dBm as shown in Fig. 13(a). The MSB 3 bits and LSB 3 bits of the reconfigurable input transistor of LNA are connected with the control code generated by capacitive sensing and resistive sensing of CIS, respectively. Furthermore, the input impedance of LNA is also varied from 100 to 600 Ω. The measured performance of LNA is affected negligibly by the variation of input impedance of LNA due to the RM network connected with GND electrode. The reconfigurable LNA gives the voltage gain of 13 to 22 dB with a wide frequency range of 10 to 200 MHz. The output voltage of the 5-bit coded inverter is controlled from 1 to 6 V as shown in Fig. 13(b). The MSB 2 bits and LSB 3 bits of the reconfigurable driver are linked with the control code from the capacitive and resistive sensing circuits, respectively. The variable output power of the reconfigurable driver in combination with CIS reduces the dynamic channel variation within 5 dB, which leads to the mitigation of the sensitivity and linearity requirements of the receiver front-end for the better power efficiency.

Fig. 14 shows the measured output spectrum of double-FSK transmitter. The right table shows the operation modes of the BCC transceiver. It supports total 104 operation modes with the data rate from 1 kb/s to 10 Mb/s and the network-coexistence from 1 to 15. Each spectrum represents modulated wideband FSK signal from 4 sub-bands with various data rates of 10 kb/s, 100 kb/s, 1 Mb/s, and 10 Mb/s. The wideband modulator spread

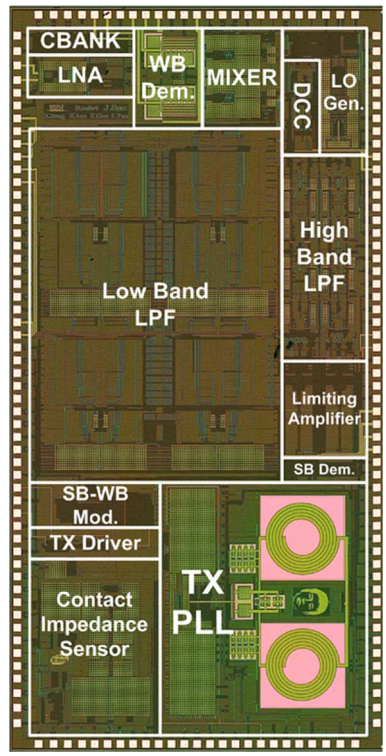


Fig. 12. Chip microphotograph.

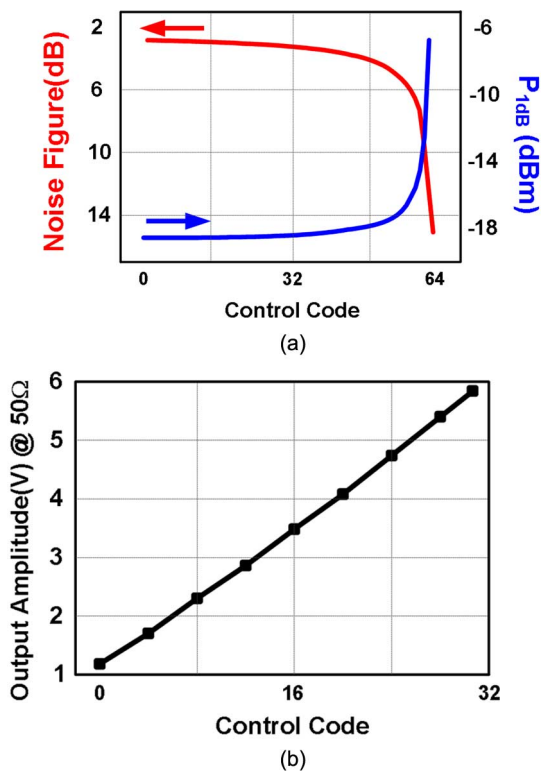
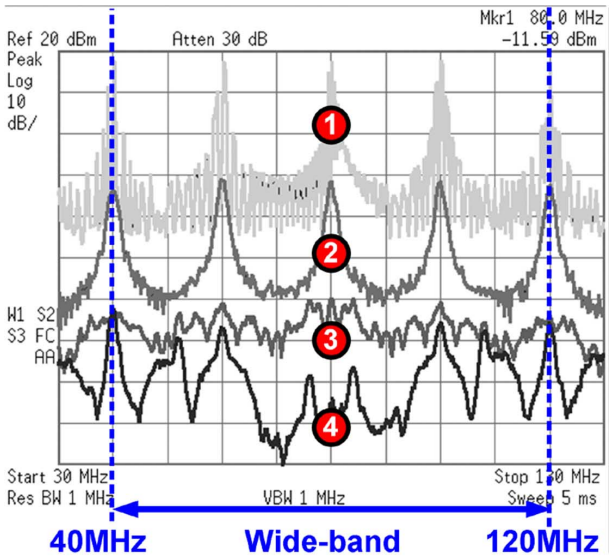


Fig. 13. Reconfigurable performance of LNA and driver. (a) Noise and linearity of LNA. (b) Output swing of driver.



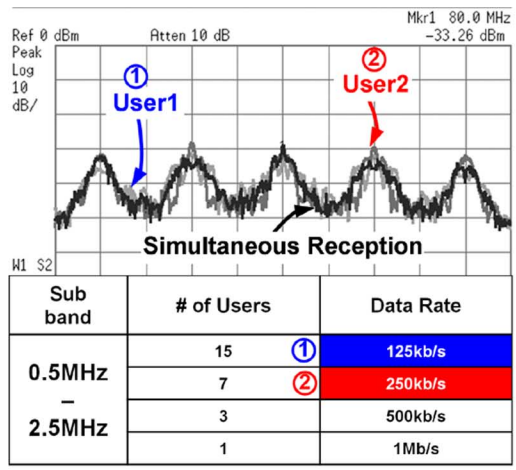
Sub band	# of Users	Data Rate
5kHz – 25kHz	15	1.25kb/s
	7	2.5kb/s
	3	5kb/s
	1 ①	10kb/s
50kHz – 250kHz	15	12.5kb/s
	7	25kb/s
	3	50kb/s
	1 ②	100kb/s
500kHz – 2.5MHz	15	125kb/s
	7	250kb/s
	3	500kb/s
	1 ③	1Mb/s
5MHz – 25MHz	15	1.25Mb/s
	7	2.5Mb/s
	3	5Mb/s
	1 ④	10Mb/s

Fig. 14. Output spectrum of the double-FSK transmitter.

the subband signal into 40–120 MHz with frequencies of 40, 60, 80, 100, and 120 MHz. The output power level is lowered by spreading gain and currently set to −15 dBm. However, the output level can be raised up to 0 dBm to compensate for the channel variation by reconfigurable driver.

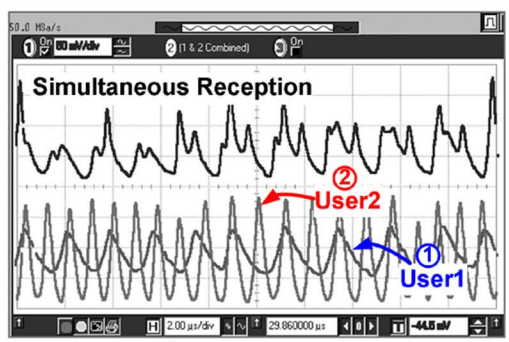
Each subband is distinguished by a wideband FSK demodulator with corresponding subband carrier frequencies. To demonstrate WBAN coexistence in a low-SNR condition, two users that occupy the same subband with different subband carrier frequencies of 0.5 and 1 MHz, and different data rates are applied to the human body simultaneously with −40-dBm input power as shown in Fig. 15. Fig. 15(a) shows the spectrum of the receiver input. The user 1 and user 2 are in the same subband from 0.5 to 2.5 MHz with a data rate of 125 and 250 kb/s as represented in the table. The time-domain waveforms in Fig. 15(b) show the output of the wideband demodulator using the input signals of Fig. 15(a). As expected, demodulation signal contains both frequencies of 0.5 and 1 MHz. However, user 1 may be viewed as a source of interference for user 2, and *vice versa*. Therefore, the sensitivity of the receiver is degraded by the multiaccess interference. In the case of Fig. 15, sensitivity degradation of 4 dB is observed. The multiaccess interference-resilience can be improved by increasing the receiver spreading gain or adopting a different multiple access technique such as time-division multiple access (TDMA) to multiplex different users onto the wideband signal [16].

Fig. 16 shows the receiver's immunity to the narrowband blocker in the 40–120-MHz frequency. For the interference performance measurement, the bit rate is set to 100 kb/s in the subband of 50 kHz to 250 kHz, the input signal power to receiver is set to +6 dB above the sensitivity limit (−60 dBm), and the CW blocker power is swept for each frequency until the BER is degraded to 0.1%. It gives signal-to-interference (SIR) at each frequency, which represents the maximum interferer power level that can be tolerated without blocking the receiver. As plotted in Fig. 16, the receiver is quite immune to blocker in the wide frequency range due to the spreading gain of the double-FSK



Sub band	# of Users	Data Rate
0.5MHz – 2.5MHz	15 ①	125kb/s
	7 ②	250kb/s
	3	500kb/s
	1	1Mb/s

(a)



(b)

Fig. 15. Measurement results of network coexistence. (a) Spectrum of the receiver input. (b) Waveform of the demodulator output.

modulation scheme. The measurement SIR magnitude agrees well with predicted value of $10\log(80\text{M}/0.2\text{M})$ $(=26$ dB) at the frequencies of 40, 60, 80, 100, and 120 MHz. However, on average, the SIR performance is little bit degraded owing to the limitation of the divider-based double-FSK modulator which

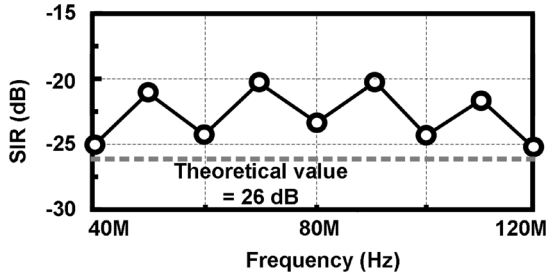


Fig. 16. SIR performance.

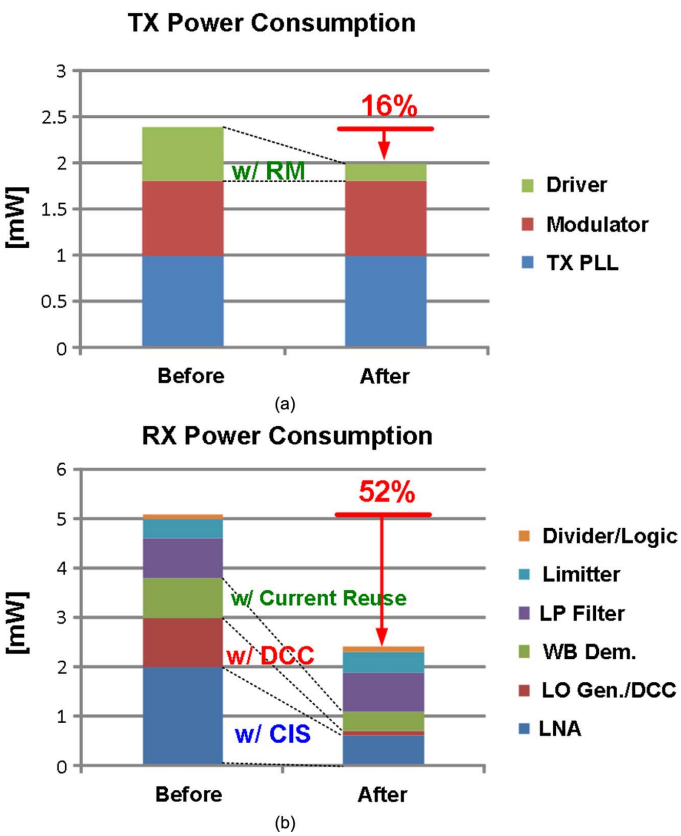


Fig. 17. Power performance. (a) TX power breakdown. (b) RX power breakdown.

generates the finite frequency sources for the wideband signal. On the other hand, the out-of-band interference suppression is further improved by the filtering of the receiver-front end.

A power breakdown of the transceiver is presented in Fig. 17. In the power breakdown of the transmitter of Fig. 17(a), the RM reduces the power consumption of the driver from 0.6 to 0.2 mW. Consequently, the transmitter consumes 2 mW with 16% power reduction. Fig. 17(b) shows the receiver power breakdown. The CIS significantly reduces the power consumption of the LNA from 2 to 0.6 mW. In addition, the current-reuse wideband demodulator and divider-based LO generation with DCC make the power-hungry frequency synthesizer unnecessary. As a result, the power consumption of the receiver can be reduced from 5.1 to 2.4 mW with 52% power saving.

Table I summarizes performance parameters of the WBAN transceiver. The transceiver supports all requirements for

TABLE I
PERFORMANCE SUMMARY

Technology		0.18 μm RF CMOS
Die Area		2.5mm X 5mm
Frequency Band		40 MHz - 120 MHz
Modulation		FSK - FSK (Double FSK)
LNA Gain		13 to 22 dB
Post LNA Amp. Gain		0 to 30 dB
Sensitivity		-66 to -40 dBm
Data Rate		10 Mb/s to 1kb/s
BER @ -62dBm		10^{-5} @ 10Mb/s & 10^{-12} @ 10kb/s
Interference Rejection		6 to 36 dB
# of Co-existence		1 to 15
Supply Voltage		1.0 V
Power Break-down	Transmitter	
	TX PLL	1.0 mW
	Divider/Other	0.8 mW
	Driver	0.2 to 2.0 mW
	Total	2.0 to 3.8 mW
	Receiver	
	LNA	0.6 mW
	Post LNA Amp.	0 to 0.8 mW
	WB Demdulator	0.4 mW
	LP Filter X 2	0.4 X 2 mW
	Limitter X 2	0.2 X 2 mW
	DCC & CAS	0.1 mW
	Divider/Other	0.1 mW
	Total	2.4 to 3.2 mW
Energy/bit		0.24nJ/b

TABLE II
PERFORMANCE COMPARISON

Parameters	ISSCC 2007 [11]	JSSC 2009 [12]	ISSCC 2009 [14]	This Work
Technology	0.18μm CMOS	0.18μm CMOS	0.13μm CMOS	0.18μm CMOS
Supply Voltage	0.9V	1V	1.2V	1V
Modulation	3-Level PPM	AFH FSK	Correlation Direct Digital	Double FSK
Frequency Band	10-70MHz	30-120MHz	1-30MHz	40-120MHz
Data Rate	10kb/s - 10Mb/s	60kb/s - 10Mb/s	8.5Mb/s	1kb/s - 10Mb/s
Sensitivity	-30dBm	-65dBm	-60dBm	-66dBm
# of Coexistence	128	1	1	15
Power Consumption	2.6mW	3.7mW	2.75mW	2.4mW
Energy/bit	0.26nJ/b	0.37nJ/b	0.32nJ/b	0.24nJ/b

WBAN in terms of sensitivity, data rate, QoS scalability, interference rejection, and network coexistence thanks to the scalable double-FSK modulation. The performance comparison with previous works is shown in Table II. The proposed transceiver consumes 2.4 mW with a data rate of 10 Mb/s. Its minimum detectable signal power is −66 dBm, which is 36 dB

better than [11]. The energy consumption is 0.24 nJ/b, which is the most energy-efficient among the reported transceivers in our comparison table.

VI. Conclusion

This paper presents the WBAN transceiver that fulfills all of the IEEE 802.15.6 Task Group specifications. Its low energy consumption of 0.24 nJ/b makes it attractive for future WBAN applications. This is achieved by resonance matching, contact impedance sensing, and a low power scalable double-FSK modulation scheme, based on the theoretical analysis of signal transmission mechanism of the BCC. To enable low-power consumption, circuit techniques such as a reconfigurable LNA/driver, current-reuse wideband demodulator, divider-based LO generation with duty-cycle corrector and a divider-based digital double-FSK modulator are proposed. The 2.5 mm $\times$ 5 mm transceiver is fabricated in 0.18-μm CMOS technology.

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