POPeye:
A Simulator for a DRAM Performance Evaluation

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Abstract

We implemented POPeye (Probe of Performance + eye), a system analysis simulator for DRAM performance evaluation in a personal computer environment. When running real-life application programs such as Microsoft Office and Paint Shop Pro on Windows 95, POPeye simulates detailed transactions between a CPU and a memory system. Using this tool, we comparatively analyzed the performance of a DDR-SDRAM and a D-RDRAM. The simulation results show that the D-RDRAM is faster than the DDR-SDRAM for a sequential memory access pattern in a 128Mbyte memory system. But the DDR-SDRAM system shows higher performance for a random memory access pattern.

I. Introduction

MOST computer systems are based on a stored program architecture that consists of a CPU, a memory and input/output devices. In order to improve the overall performance in stored program architecture, it is necessary to increase the speed of memory as well as the speed of CPU and the capacity of a memory. Because the memory bandwidth becomes a bottleneck of a system performance, many researches for faster memories are in progress and new high performance memory systems for 3D graphics or image processing are being proposed and developed by many DRAM companies [1 ~ 4].

As a D-RDRAM (Direct-Rambus DRAM) and DDR-SDRAM (Double Data Rate–SDRAM) are getting widely used in the PC and the workstation market, the performance analysis of these two DRAM architectures are a hot issue [5, 6]. Therefore, the exact performance evaluation of the DRAM systems is crucial. The system level performance analysis is also required because the simulation of only the DRAM itself is not enough to evaluate the exact performance of the DRAM in the system.

There are two methods for performance evaluation at system level; a hardware and a software based method. The former gives more reliable results than the latter, because exact system modeling in software is impossible. But a hardware implementation of an entire system costs more money and time. And it has less adaptability to system variation than a software method does. Consequently, the software modeling needs less development cost and time than the hardware method. It also has flexibility in performance analysis of diverse systems which have different concepts of DRAMs. Moreover, the software simulator can evaluate the performance of a new DRAM architecture before the fabrication of the actual sample chip. But software simulation requires more simulation time and gives less reliable results than hardware simulation. In order to remedy the weak point of the software method, we implemented POPeye (Probe of Performance + eye) which is a system analysis simulator for DRAM performance evaluation in a PC. A memory system of POPeye is modeled at a structural level for more realistic simulation results but the other parts are modeled at a behavioral level for fast simulation [Figure 1]. POPeye is developed for the detailed performance analysis of a DRAM system at system level. With the POPeye, we analyzed the performance of a DDR-SDRAM and a D-RDRAM in a PC system running on a UNIX environment. Detailed simulation results will be explained in part IV.

II. POPeye: A System Analysis Tool for DRAM Performance Measurement

A. Configuration of POPeye

POPeye is a software simulator for the PC's DRAM performance analysis [7]. It consists of two parts: a Virtual PC and a Performance analyzer as shown in Figure 2. Virtual PC is a software model of a desktop PC system which has a Pentium microprocessor, a memory system and peripheral devices such as a keyboard, a mouse and a VGA display. The POPeye is implemented with C++ language but also partially with C and assembler language.

We modeled an x86 processor that is compatible with a Pentium microprocessor at instruction level [8], so the virtual PC can directly execute real-life application programs based on Windows OS without any modification. The processor of POPeye was modeled at the mixed level between the structural level and the

behavioral level. Especially, the parts that are related to memory were modeled at detailed structural level because we need the detailed transaction information of the DRAM system. The size and mapping type of L1 cache, BTB (Branch Target Buffer) and TLB (Transition Look aside Buffer) can be modified according to the specific architectures. The memory system consists of a L2 cache, a chipset (memory controller) and a main memory (DDR-SDRAM, D-RDRAM). The size and mapping type of L2 cache are also variable.

While the virtual PC simulates the real PC and runs real-life application programs in real time, the performance analyzer collects detailed transaction information about DRAM access. Figure 3 shows POPeye simulating a virtual PC on workstation.

B. Verification of POPeye Analysis

In order to verify the validity of POPeye's results, we measured the average percentage of a processor's stall cycle while the virtual PC was executing several application programs. Assuming the virtual PC with a Pentium Processor @ 133MHz, 512K L2 Cache and 64Mbyte SDRAM, we obtained the results shown in Table 1.

Using the results in Table 1, we calculated the average percentage of a processor's stall cycle with the following formula.

$$\text{Average Stall percentage} = \frac{\sum \text{access cycle x portion - L1 cache access cycle x portion}}{\sum \text{access cycle x portion}} = 18.52\,\%$$

Intel shows a system resource utilization of several application programs in iCOMP Index 2.0 [9]. It states that the average percentage of stall cycle is about 20% and this value is consistent with the POPeye result, 18.52%. This consistency is believed to confirm the accuracy of the POPeye results.

III. Modeling of a DDR-SDRAM and a D-RDRAM

Using the POPeye simulator, we compared the performance of DDR-SDRAM and D-RDRAM which are getting widely used in the PC system.

The virtual PC runs several different applications to obtain various access patterns of the memory system with the simulation parameters shown in Table 2.

128Mbyte DDR-SDRAM modules consist of eight128Mbit DDR-SDRAM (16Mbit x 8). Each DDR-SDRAM has 4 banks. We modeled a DDR-SDRAM chipset based on the Intel 440BX chipset that supports SDR (Single Data Rate)-SDRAM [10]. The modules have the maximum bandwidth of 2.1 Gbyte/sec (=133MHz x 2 (Double Data Rate) x 8 byte (64bit)) with 64bit bus at 133MHz.

128Mbyte D-RDRAM modules consist of eight 128Mbit RDRAM (8M Word x 16bit). Each RDRAM has 32 banks. The modules have the maximum bandwidth of 1.6 Gbyte/sec (=Dualoct (16Bytes) x 800MHz / 8 (4 t_{cycle})). We modeled a RDRAM controller (chipset) based on the Intel 820 chipset [11].

IV. Simulation Results

We run three applications on a POPeye simulator: Windows 95 Boot-up, Paint Shop Pro 4.0 and Microsoft Excel 7.0. These programs have different memory access patterns.

When Windows 95 is booting up, reading access to memory shows more often than writing access. When graphics application programs like Paint Shop Pro is running, its data has more spatial localities than other applications does. More reading access is observed than writing access. A Spread Sheet program like Microsoft Excel needs much computation in a processor, therefore there is less memory access and less spatial localities than graphics application programs. Table 3 shows the ratio of reading and writing access to a memory.

We compared the performance of 128Mbyte DDR-SDRAM with 128Mbyte D-RDRAM. The performance means the reciprocal of the execution time. The execution time is obtained by the product of the number of total clock cycle and clock cycle time as shown in following equation.

$$performance = \frac{1}{CPU\ clock\ cycle \times Clock\ cycle\ time}$$

The clock speed of a DDR-SDRAM and a D-RDRAM system is assumed to 133MHz and 400MHz, respectively.

A D-RDRAM chip has less number of pins than a DDR-SDRAM chip for higher speed and lower power transmission. The throughput of a D-RDRAM is higher than that of a DDR-SDRAM. However, because sharing the pins for address, data and control signals, a D-RDRAM has to transact in packets of the signals and needs decoding logics to interpret the information in the packets. Therefore the latency of D-RDRAM takes longer than that of a DDR-SDRAM [1].

Figure 4 shows the normalized performance of a 128Mbyte DDR-SDRAM and a 128Mbyte D-RDRAM for three different applications: Windows Boot up, Paint Shop Pro 4.0 and Microsoft Excel 7.0. When Windows95 is booting up, the performance of the two memory systems is very similar. When Paint Shop Pro is running, a graphic application program, its memory access pattern is sequential and high spatial localities exist. Therefore the memory throughput is more serious than the

latency. Therefore D-RDRAM showed better performance than a DDR-SDRAM by 21% at graphics applications. In the case of Excel whose memory access pattern is more random than the other applications, the memory latency is more important than the throughput. Therefore the performance of DDR-SDRAM was higher than D-RDRAM by 13%.

V. Conclusion

We implemented POPeye, a system analysis simulator for DRAM performance evaluation in a PC environment. When running real-life application programs such as Microsoft Office and Paint Shop Pro on Windows 95, POPeye simulates detailed transactions between a CPU and a memory system. Using this tool, we comparatively analyzed the performance of a DDR-SDRAM and a D-RDRAM.

The performance of 128Mbyte D-RDRAM is higher than that of 128Mbyte DDR-SDRAM by 21% with a graphic application program, but 128Mbyte DDR-SDRAM is faster than 128Mbyte D-RDRAM by 13% with a spreadsheet program. Because the throughput of a D-RDRAM is higher that that of a DDR-SDRAM, a D-RDRAM system is faster at sequential memory access patterns. But, because the D-RDRAM has longer latency, the DDR-SDRAM system is faster at random memory access patterns.

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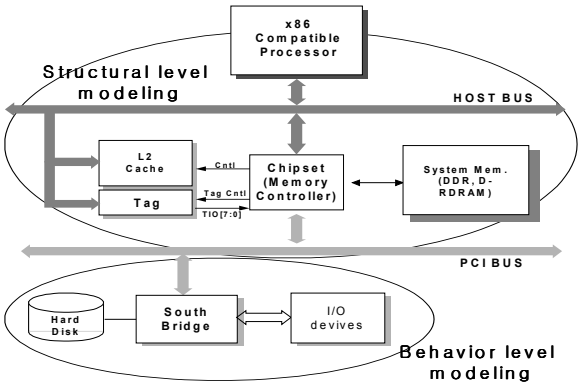

Figure 1 A Target PC System of POPeye

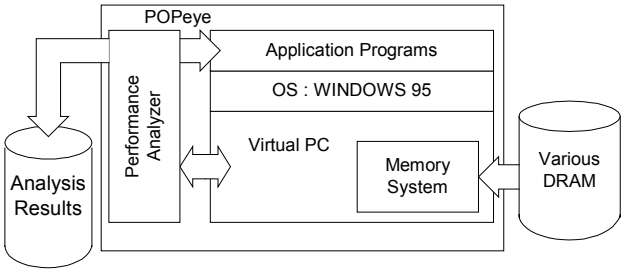

Figure 2 A Configuration of POPeye

Figure 3 A POPeye simulation example.

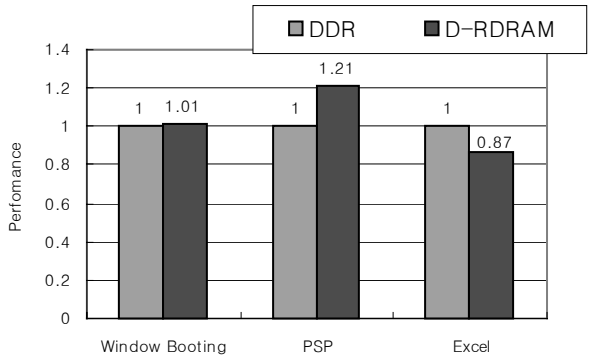

Figure 4 A Normalized Performance comparison between 128Mbyte DDR-SDRAM and 128Mbyte D-RDRAM

	L1 Cache	L2 Cache	Main Memory
Portion of Request to Memory	99.55%	3.90%	0.55%
Average Access Cycle	1.87	7.4	21.36

Table 1 Simulation Results: Memory Access Time

CPU	166MHz x86 Compatible Processor
L1 instruction / data Cache	• 16Kbytes / each • 2way Set Associative Mapping • 32Byte Line Size
L2 Cache	• 1Mbytes • Direct Mapping, 32 Byte Line Size

Table 2 Simulation Parameters

Application program	Write access	Read access
Windows 95 Boot-up	47.6%	52.4%
Paint Shop Pro 4.0	32.5%	67.5%
Microsoft Excel 7.0	35.6%	64.4%

Table 3 Read and write access ratios of different applications simulated by POPeye