Single Chip 3D Rendering Engine Integrating Embedded DRAM Frame Buffer and Hierarchical Octet Tree (HOT) Array Processor with Bandwidth Amplification

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Abstract — A single chip rendering engine that consist of a DRAM frame buffer, a SRAM serial access memory, pixel/edge processor array and 32b RISC core is proposed for the low power 3D-graphics in portable system. The 56mm^2 prototype integrating edge processor, 8 pixel processors, 8 frame buffers and RISC core is fabricated using 0.35μm CMOS Embedded Memory Logic (EML) technology.

I. INTRODUCTION

Recently, portable devices continuously extend their multimedia application areas to the voice and 2D-image processing of videophone and even to the realization of a multimedia system on a chip [1][2]. 3D graphics are also attractive applications that may be included in the portable multimedia terminal such as a PDA or mini-game machine [1][2]. We propose a low power, single chip 3D graphic rendering engine for future portable multimedia system using EML technology.

II. ARCHITECTURE

The proposed rendering engine is based on *2D-Hierarchical Octet Tree (HOT)* array structure which consists of a preprocessing RISC core, bus matching queue, edge processors (EPs), pixel processors (PPs), DRAM frame buffers (FBs) and SRAM serial access memories (SAMs). It has a two-level octet tree structure that is made of single master processor and eight slave processors at each level as shown in Fig. 1. A set of preprocessor and 8 EPs makes the first-octet processing layer. Again, 8 sets of EP and 8 PPs make the second-octet processing layer. These two layers support a two-step parallelism; coarse polygon parallelism at the first layer and fine pixel parallelism at the second layer as shown in Fig. 2. The coarse operation determines the polygon edge information at EPs and transfers it to next layers. The fine pixel operation calculates the inner pixel information at PPs and performs read-modify-write (RMW) memory operation such as α-blending and depth comparison between PP and FB.

The bandwidth amplification is obtained from the bus configuration of 2D-HOT array structure of Fig. 1. First, the 32b RISC preprocessor supplies polygon information and commands to the bus-matching queue through the 32b width bus in every 9 clocks @100MHz or 11.1M Polygon/sec drawing speed. Second, the queue extends the bus width from 32b up to 160b in order to feed them into 8 EPs. Each EP plays as a master of its own 8 PPs connected by 64b bus. There are 8 groups where each group is made of 1 EP and 8 PPs. Each PP directly interfaces with the corresponding FB through the 40b RMW data bus. Finally, 2,560b data can be accessed by 64 RMW pixel processor operations within every memory cycle, 9 clocks including RMW access and pre-charge @ 100MHz or 7.1GB/sec frame buffer access bandwidth. It is the bandwidth amplification and 80 times gain, that is difficult to be implemented in space limited PCB, can be obtained in the HOT architecture. The performance improvement by the proposed scheme is about 70% ~ 10% of the conventional approaches over several objects with different scales as shown in Fig.3. As an object size is reduced, the proposed scheme achieves more performance improvement. This is profitable in potable multimedia terminal such as PDA applications with small screen size.

III. TEST CHIP AND MEASUREMENTS

For the 256 × 256 pixels resolution with the 24b true color double buffer and 16b depth buffer, the frame buffer contains 4Mb DRAM and 6Kb SAM. Full custom designed 1 EP, 8 PPs, 8 FBs and 8 SAMs with the HOT architecture are integrated for the memory coupled logic operation of 3D rendering. For the flexible pre-processing, a 32b RISC core is fabricated on the same die by the logic synthesis based on standard cells. The microphotograph of test chip, 52 mm^2 of rendering engine and 4 mm^2 of 32b RISC core, is shown in the Fig 4. The test chip characteristics are summarized in the Table 1. The measured waveforms including a 100MHz system clock, 25MHz SAM clock, SAM transfer command and pixel output stream is also shown in Fig. 5. After 9 clock cycles for SAM transfer command and additional 6 clock cycles for memory operation, pixel data stream comes out synchronized with SAM clock. For the overall functional test, PCI interface unit, first-in-first-out external memory and simple FPGA controller assembled in the test bench as shown in Fig. 6.

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IV. CONCLUSION

3D rendering engine with 7.1GB/sec memory bandwidth and 11.1M polygon/sec drawing speed @ 100MHz is proposed. The test chip is fabricated using 0.35μm EML process and its operation is demonstrated on test bench. The proposed rendering architecture is suitable for the portable 3D graphic devices such as PDA or mini-game machine that requires a low power, high bandwidth and small board area.

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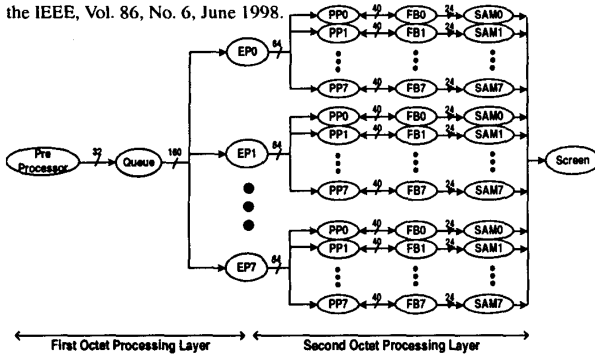

Fig.1 Hierarchical Octet Tree (HOT) Array Structure

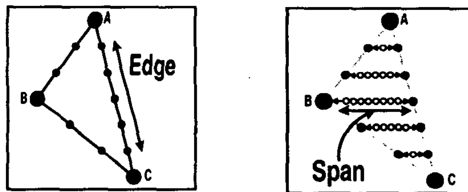

Fig.2 Coarse Parallelism (Left) and Fine Parallelism (Right)

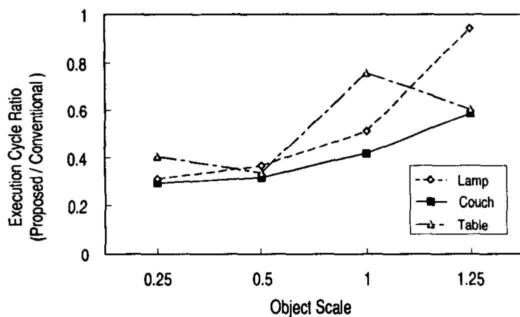

Fig.3 Execution Cycle Ratio of Proposed and Conventional scheme

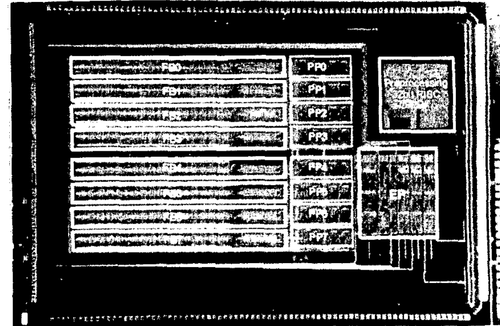

Fig.3 Test Chip Microphotograph

Table 1. Test Chip Characteristics

	EP	PP	FB
Technology	0.35μm CMOS EML, 4polys 3metals		
Area	5.3mm^2	0.9mm^2	3.7mm^2
Clock	100MHz	100MHz	100MHz/33MHz
Voltage	3.3V	3.3V	3.3V/5V
Power	150mW	35mW	20mW
Organization	1EP	8PPs	8FBs/8SAMs
Package	304 RQFP		

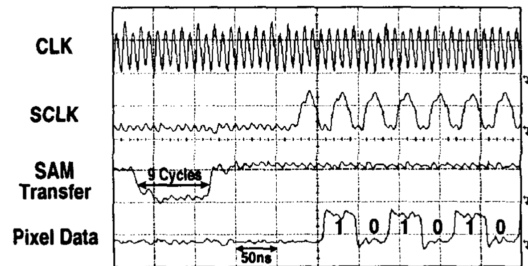

Fig.5 Measured Wave Forms

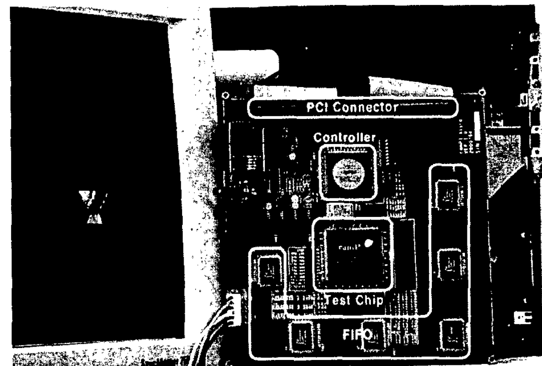

Fig.6 Photograph of Test Board