Gigabit Throughput CMOS ICs for Optical Interconnection Applications

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1. Introduction

Recently, SONET OC-48 has been widely accepted in WAN and OC-192 is about to be installed. In response to these movements, Gigabit Ethernet is widely accepted in MAN and LAN. Compared to long distance applications where expensive technologies such as SiGe and III-V technologies are mainly used, issues on cost and integrability with other digital blocks are more important in short haul network. Low power consumption and technology compatibility are important too.

In this paper, low cost and low power CMOS ICs are studied for the gigabit throughput backbone interconnections. Its technology is compatible with other digital blocks leading to its easy integration in interconnection SOCs compared with the stand-alone transmitter and receiver in long haul applications. The light source is VCSEL which is very suitable for low power interconnections[1]. 5-channel parallel interconnection and 1/8-rate clock and data recovery (CDR) circuit will be described[2, 3]. In addition, a new low cost approach, Multichip on Oxide (MCO) technology will be explained[4].

2. 4-Gb/s CMOS CDR Circuit with 1/8-Rate Clock

Fig. 1 shows block diagram of the 4-Gb/s CDR circuit exploiting a 4-phase 1/8-rate clock technique for low power and low noise operation with relatively low speed circuits.

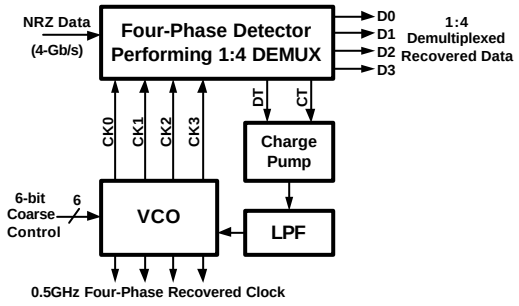


Fig. 1 Block Diagram of the 4-Gb/s CDR.

The VCO of Fig. 2 provides the 50% duty correction operating at 1/8-rate clock. The 4-phase detector performing 1:4 DEMUX accomplishes a linear frequency and phase detection with no systematic phase offset. Test chip was fabricated with 0.25μm CMOS process. The peak-to-peak jitter of the recovered clock is 47ps for a PRBS of 2^{31}-1 as shown in Fig. 3.

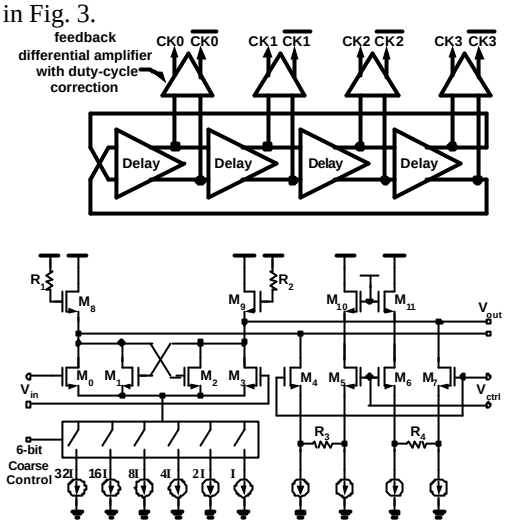


Fig. 2 4-stage VCO with an active inductor loaded delay

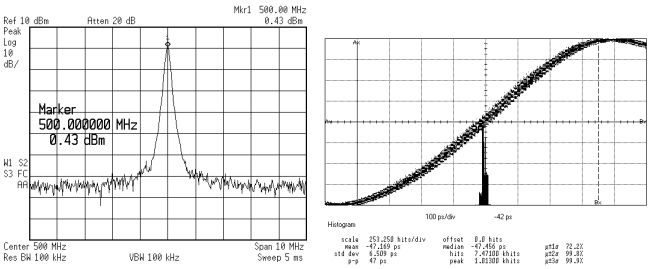
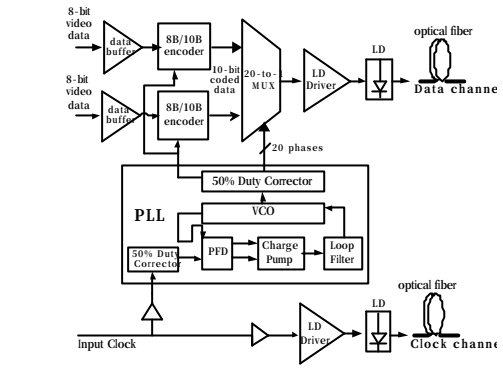


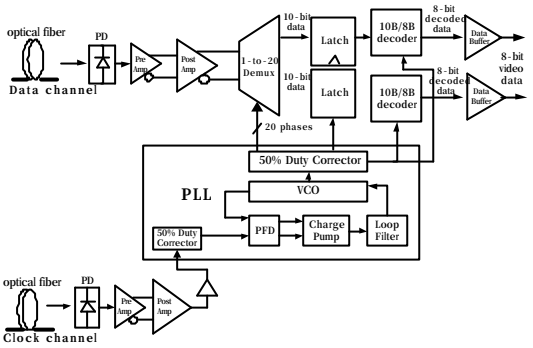
Fig. 3 Spectrum and jitter histogram of the recovered clock

3. 1.25Gbps CMOS 5 Parallel Channels

Fig. 4 shows block diagrams of 5-channel optical transmitter and receiver for short distance video data transmission. The light sources are 850nm VCSEL and 0.25μm standard CMOS process is used. 5 optical fibers lines are used; 3 channels for RGB data, one for control signal and one for clock. The maximum data rate per channel is 2.5Gbps but for fear of the degradation due to crosstalk it is operated at 1.25Gbps. It accepts 16bit external data, two pairs of 8 bits parallel data and then the data are DC balance coded with 2 of 8b/10b encoders. Transition minimizing coding schemes which are used in electrical interconnection are not considered because EMI is no more an issue in fiber link. The 20-to-1 serializer shows the automatic modification of the swing amplitude without any extra swing control circuit by use of the diode connected PMOS load.



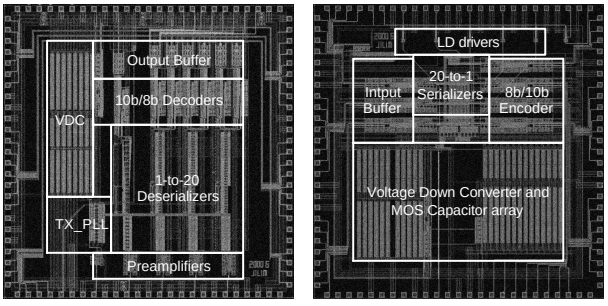
(a)



(b)

Fig. 4 Block Diagrams of the 5-channel CMOS (a) transmitter and (b) receiver

Fig. 5 shows the microphotographs of the transmitter and receiver chips. The receiver uses the fully differential architecture to reduce the effect of substrate noise and supply noise. In addition, an internal voltage down converter(VDC) is adopted to stabilize the voltage supply lines.



(a) (b)

Fig. 5 Microphotographs of (a) receiver and (b) transmitter

Fig. 6 shows images on the LCD monitor of which data is transferred with the fabricated transmitter and receiver.

4. Multichip on Oxide Optical Interconnection

A 1.25Gbps 80dBΩ fully differential TIA is fabricated using 0.25μm CMOS and MCO process as illustrated in Fig. 7. MCO enables low-cost high performance integration of

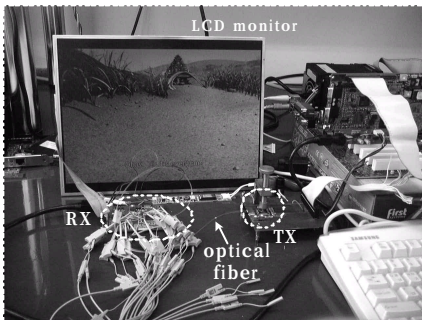


Fig. 6 Their application in digital display

PD, TIA and planar inductors of Q=21.1 for shunt peaking on oxided silicon substrate as shown in Fig.8.

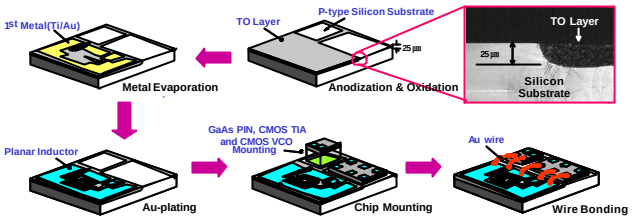


Fig. 7 Fabrication process of MCO and Thick Oxide

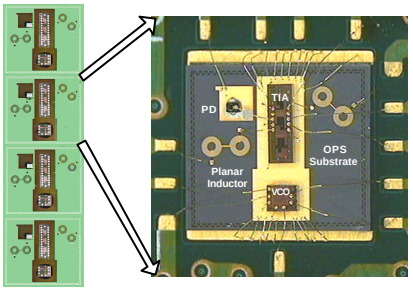


Fig. 8 Microphotograph of four-channel MCM array

5. Conclusions

CMOS solutions for the gigabit throughput optical interconnections are presented. 4Gb/s CDR circuit shows 70mW power consumption with 2.5V supply. The 1.25Gbps 5 channel transmitter and receiver consumes 97mA and 225mA, respectively at 3.3V supply. These ICs are compatible in process technology with other CMOS digital logics leading to their easy SOC integration. A new approach, MCO, for the low cost and high performance system integration is demonstrated. Multifunctional blocks can be integrated on thick oxide without crosstalk noise.

References

[1] Hoi-Jun Yoo, et al, Appl. Phys. Lett. **56**, 1942-1944 (1990)
[2] Jaeseo Lee, et al, ISCAS, **IV**, 702-704 (2001)
[3] Seong-Jun Song, et al., C11, 28th ESSCIRC (2002)
[4] Jaeseo Lee, et al., *ISSCC Dig. Tech. Papers*, 80-81(2002).