Low Power MPEG-4 Video Codec Hardware for Portable Applications

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Outline

– Introduction
  • Motivations

– **Design of Low Power Motion Compensation (MC) Accelerator**
  • Low Power Design Techniques
  • Implementation Results

– **Design of Low Power Motion Estimator (ME)**
  • Low Power Design of Processing Element (PE)
  • Simulation Results

– Conclusions
Portable Multimedia Applications

Various Portable Multimedia Applications

- IMT-2000 Network
- VOD
- Video Conferencing
- Video Mail, etc.

- Internet
- Wireless Channel
- MPEG-4 or H.263
  - VOD
  - Video Conferencing
  - Video Mail, etc.

- Low Power
- High Performance
- mp3
- Recorder
- Voice Mail, etc.

- Wired Channel

MPEG-4 or H.263

Low Power
High Performance

mp3
Recorder
Voice Mail, etc.
Video Codec

- **Low Power Dedicated H/W**
- **Most Computation-Intensive Part in Video Codec**
- **Intensive Memory I/O**
Contributions of This Work

• For Low Power Video Decoding
  - Hardware Acceleration for MC
  - MCA + eDRAM Structure
  - Optimized Architecture for Low Power Consumption

• For Low Power Video Encoding
  - Low Power ME (Systolic Array Structure)
  - Low Power PE for Array-based ME Processor
  - Low Power Operation by Adaptive Bit resolution Reduction
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Motion Compensation (MC) Accelerator

Frame Buffers (Embedded DRAM)

- Frame Buffer #1
- Frame Buffer #2

Datapath (Logic)

- Scanline Buffer
- Pixel Selection
- HPel ALU Array #0 ~ #7
- Pixel Alignment
- Pixel ALU Array #0 ~ #7
- Line Selection
- Pixel Buffer

20MHz

Internal Data Transactions (128b)
Distributed Nine-Tiled Block Mapping
Partial Activation
Partial I/O control

Aggressive Clock Gating
Parallel Pixel Processing
Prediction Error

Ref: (C.W. Yoon, ISSCC2001, JSSC2001)
Frame Buffer Structure

Bank #0
#1
#2

128b I/O

9-Bank

4 Segments

Partial Activation Control

Partial I/O Control
Memory Access Patterns

- **Frame Image**
- **Screen Out** (1 Line)
- **Data Processing** (1 Block)
- **Large Spatial Locality**
- **Center-Biased Nature of Motion Vector Field**

- **Access #N**
- **Access #N +1**
- **Access #N +2**

- **Required Blocks for Reconstruction**
- **Reusable Blocks**

(a) Akiyo

Counts (%)

- X
- Y
Distributed Nine-Tiled Block Mapping: Low Power Technique (1)

- Frame Image
- A Block in A Row
- Distribute to 9 different Banks
- Increasing Re-usability of DRAM Rows
- Minimizing Cell Core Activation in DRAM
Partial Activation Control Scheme

: Low Power Technique (2)

(a) Block Processing

(b) Screen Update
**Power Savings**

**Row Reusability**

- Akiyo: 45%
- MissA: 41%
- Fore: 36%
- Carp: 38%
- Table: 27%

**Power Reduction**

- Up to 31% Power Reduction Compared with 1-Bank Structure

### Conversion

- 1-bank
- Akiyo: 69%
- MissA: 75%
- Fore: 78%
- Carp: 77%
- Table: 82%

**Legend**

- By DNTBM
- By PAC
Implementation Results

<table>
<thead>
<tr>
<th>Frame Buffer #1</th>
<th>Frame Buffer #2</th>
<th>MC Accelerator</th>
<th>DP-SRAM</th>
<th>32b RISC</th>
<th>MPEG-4 Decoder</th>
</tr>
</thead>
</table>

### Area (mm²)
- Logic: 2.3 mm²
- DRAM: 5.25 mm²

### Power Supply
- Logic: 1.5 V
- DRAM: 2.5 V

### Clock Frequency
- Logic: 20 MHz
- DRAM: 20 MHz

### Power
- Logic: 4.6 mW
- DRAM: 11.7 mW

### DRAM Capacity
- 2 x (512bit x 128row x 9bank)

### Target Functionality
- MPEG-4 SP@L1, H.263, H.263+

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Concept of Adaptive Bit-Resolution Control Scheme

\[ SAD(i, j) = \frac{1}{MN} \sum_{k=0}^{M-1} \sum_{l=0}^{N-1} (C_{i,j} - R_{i,j}) \]

Motion Vector Detector

Accumulator

Reduced bit Operation in Hardware

Redundant Transitions in Datapath are Reduced

Common Part in MSBs can be Ignored

Actual Difference can be Found only in LSBs
Bit Resolution Distribution

0~4 LSBs

Power Savings in the datapath can be Maximazed

Akiyo 73%
Miss A 63%
Car. 57%
Fore. 52%
Table 59%
Football 30%
Stefan 38%

Full Search [-16, 15.5]

Miss America

Football

Constant Color & Small Movement

Contains many of fast moving objects
Circuit Implementation

Conventional PE

Subtraction Unit

Absolute Unit

Accumulator

PE with ABRC

Bit Resolution Detector

Resolution Control
Trade-off (1) : Power

Power (Datapath)

Monotonically Decreasing

Power (Control Circuits)

From Additional Control Circuits

16% 18% 20% 22% 33%

4b-4b 4b-2b-2b 2b-2b-4b 1b-1b-1b-1b-1b-1b-1b-1b
Trade-off (2) : Area

Area (%)

Ref PE_structure

7% 10% 16% 16.5% 33%

From Additional Control Circuits

- 4b-4b
- 2b-2b-4b
- 4b-2b-2b
- 2b-2b-2b-2b
- 1b-1b-1b-1b-1b-1b-1b-1b
Power Savings

Full Search [-8, 7.5]

- 34%
- 10%

Too Much Overhead

2b-2b-2b-2b shows the Best Performance

4b-4b can be a good trade-off

P. Savings for Various Algorithms

<table>
<thead>
<tr>
<th>Method</th>
<th>Max</th>
<th>Min.</th>
</tr>
</thead>
<tbody>
<tr>
<td>FS [-16, 15]</td>
<td>39%</td>
<td>15%</td>
</tr>
<tr>
<td><strong>BBGDS [-8.7]</strong></td>
<td>41%</td>
<td><strong>13%</strong></td>
</tr>
<tr>
<td>BBGDS [-16, 15.5]</td>
<td>39%</td>
<td>10%</td>
</tr>
</tbody>
</table>
Conclusions

- Low Power MC Accelerator For Portable Applications
  - *Optimized Architecture in terms of Low Power Consumption*
    - Various Low Power techniques

- Low Power PE for Systolic Array-based ME
  - *Adaptive Bit Resolution Control* according to Operands
    - 10~40% Power Savings in Datapath
    - Without any sacrifice of Calculation accuracy
    - Comparison of Various PE structure
      - PE with 2b Granularity Control scheme shows the best performance
      - PE with 4b Granularity can be a good trade-off