Low Power MPEG-4 Video Codec Hardware for Portable Applications

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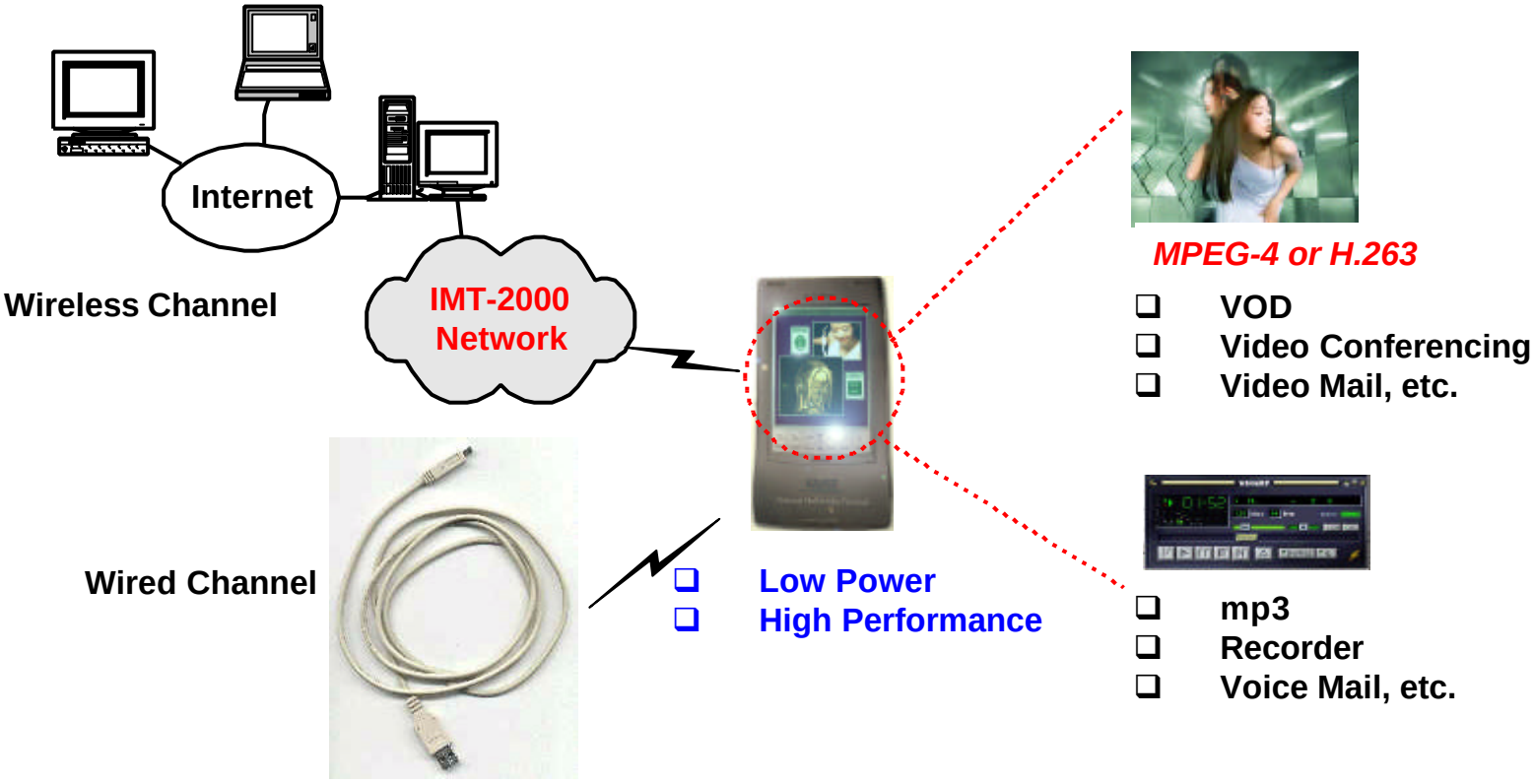
Outline

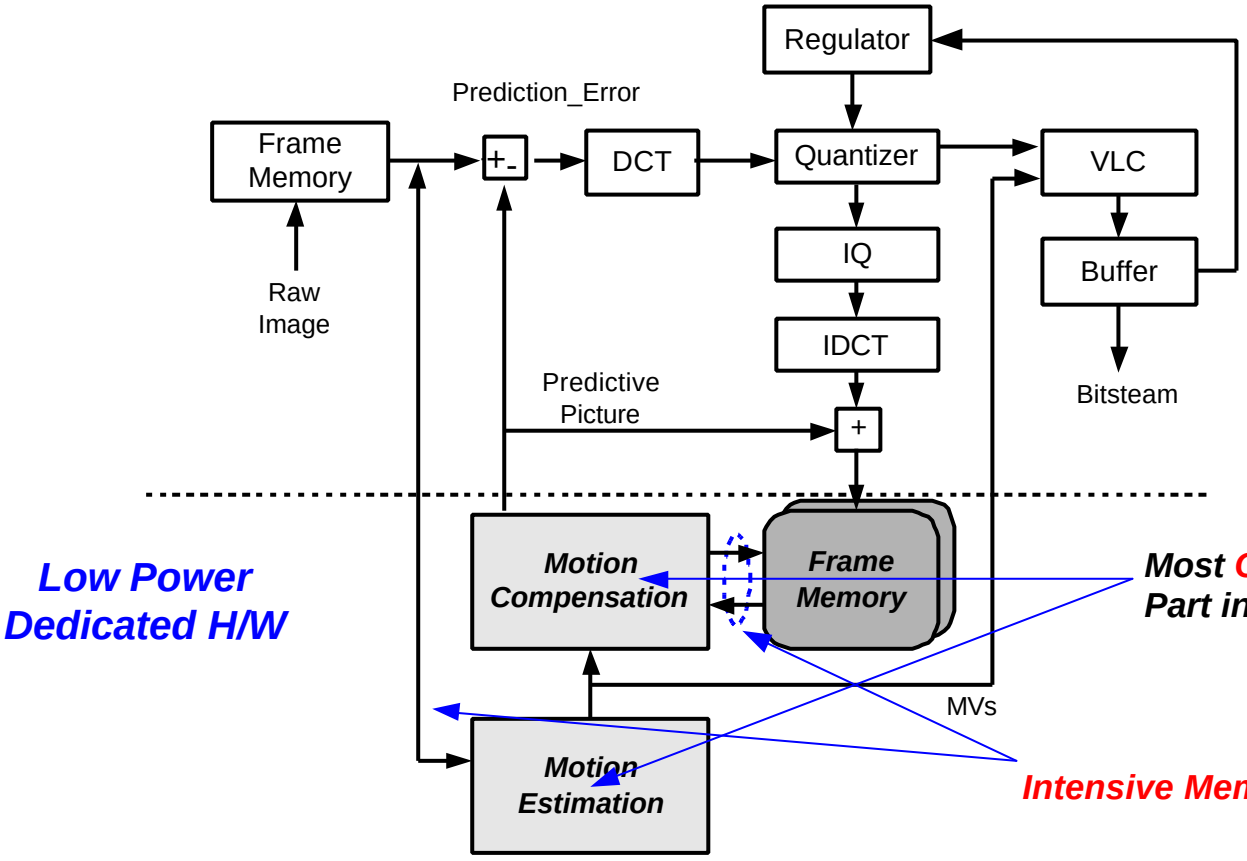
- **Introduction**
  - Motivations
- **Design of Low Power Motion Compensation (MC) Accelerator**
  - Low Power Design Techniques
  - Implementation Results
- **Design of Low Power Motion Estimator (ME)**
  - Low Power Design of Processing Element (PE)
  - Simulation Results
- **Conclusions**

Portable Multimedia Applications

Various Portable Multimedia Applications



Video Codec



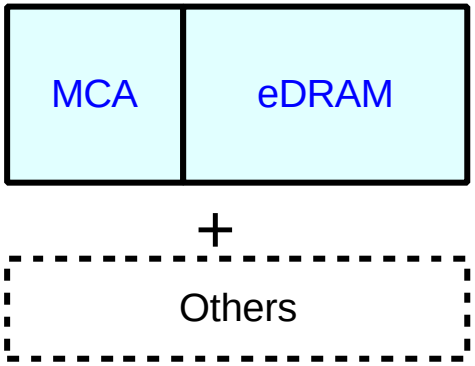
Low Power Dedicated H/W

Most Computation-Intensive Part in Video Codec

Intensive Memory I/O

Contributions of This Work

- For Low Power Video **Decoding**

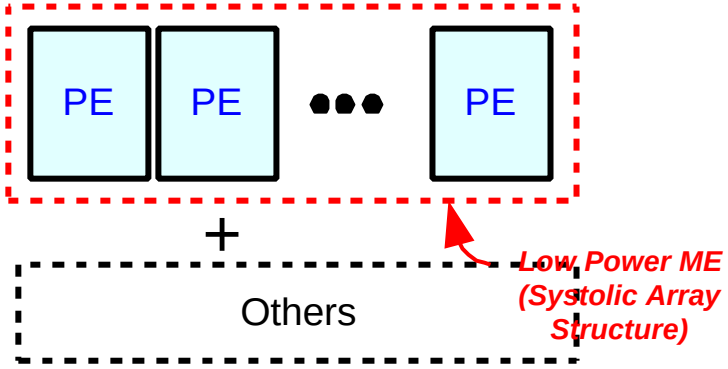


Hardware Acceleration for MC

MCA + eDRAM Structure

Optimized Archictecture for Low Power Consumption

- For Low Power Video **Encoding**



Low Power PE for Array-based ME Processor

Low Power Operation by Adaptive Bit resolution Reduction

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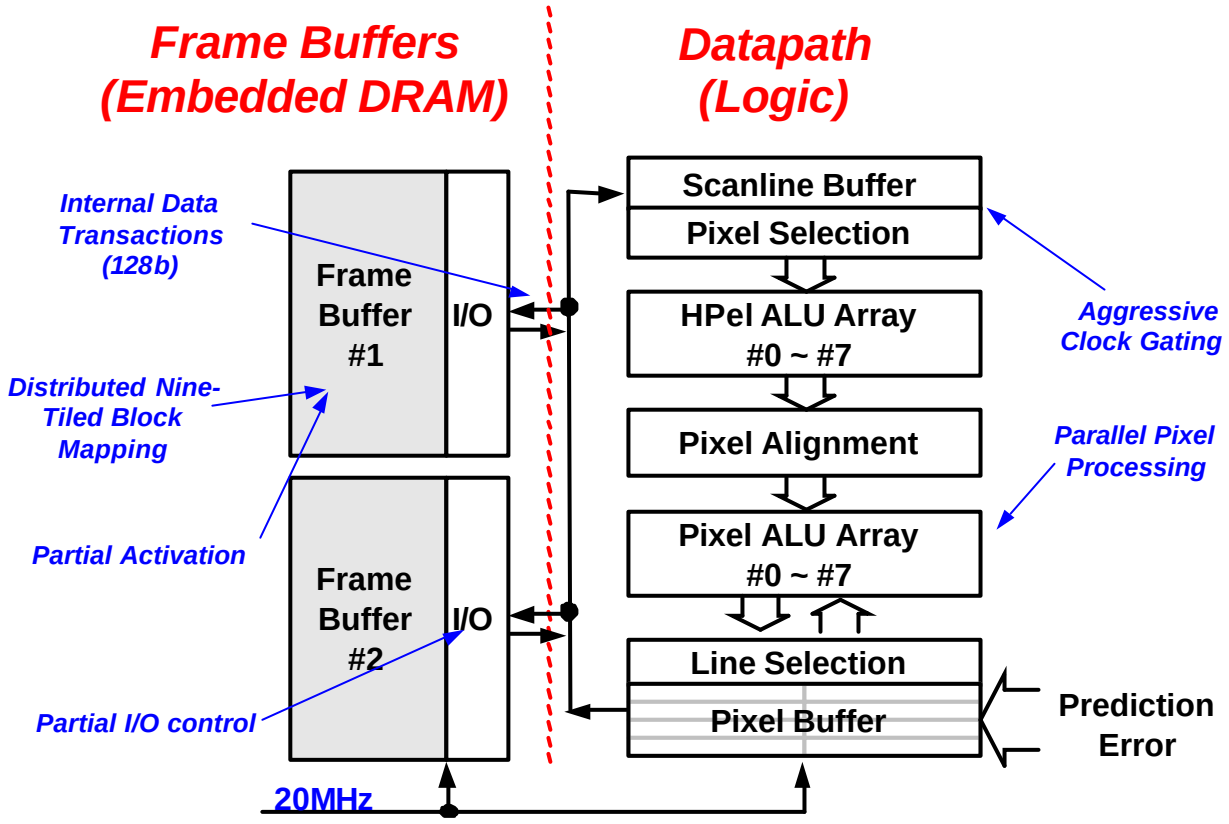
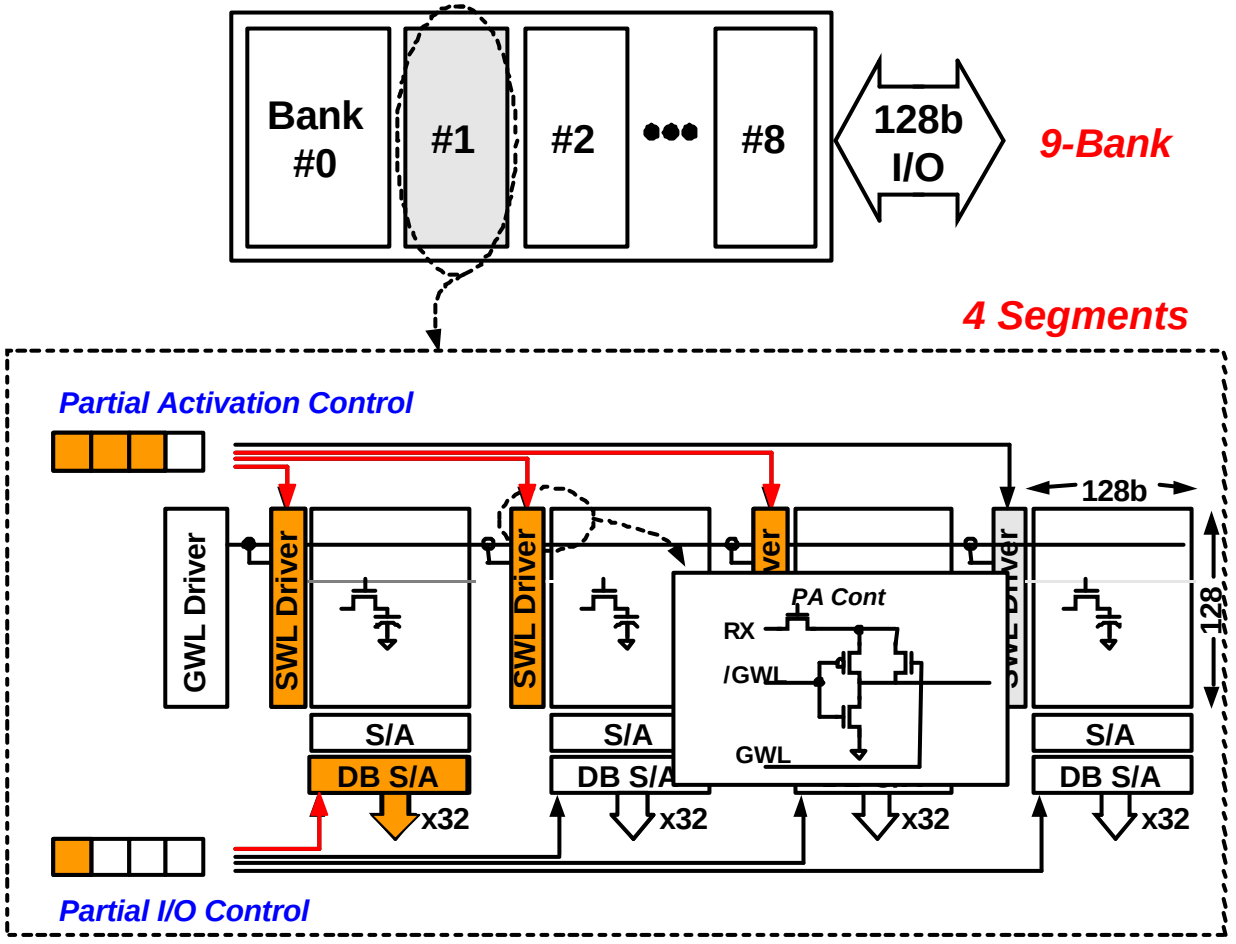
Motion Compensation(MC) Accelerator

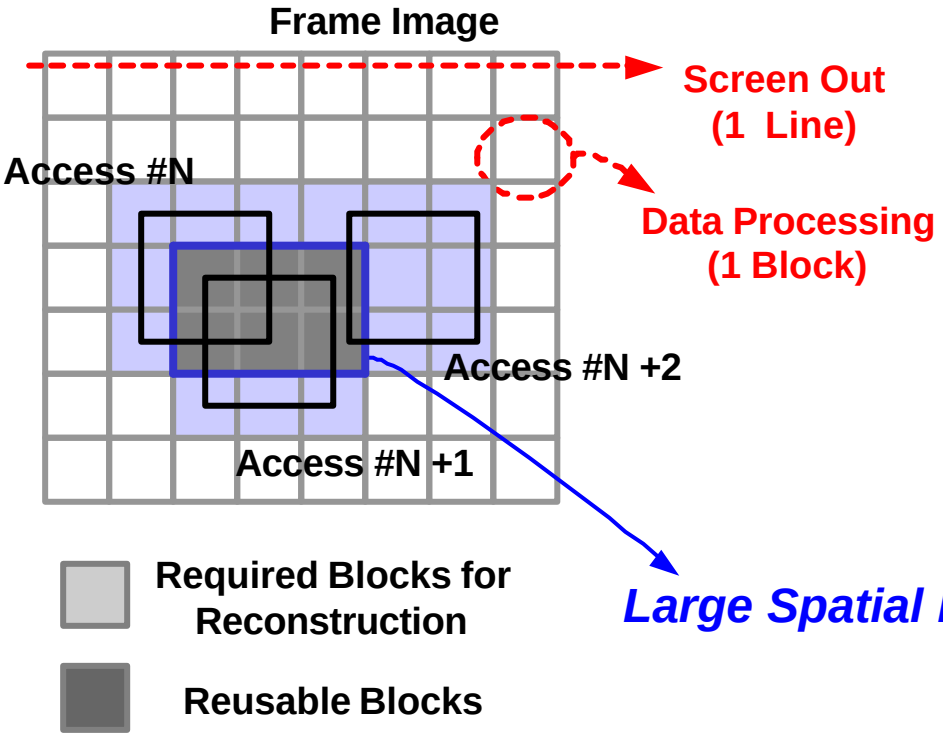


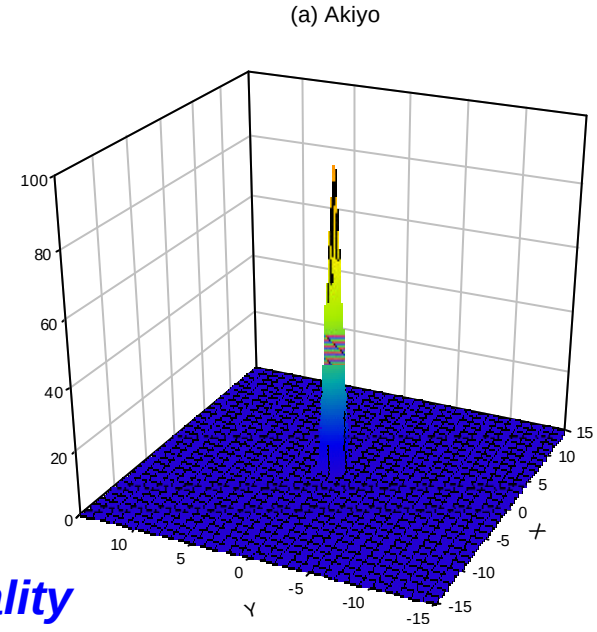
Ref : (C.W.Yoon, ISSCC2001, JSSC2001)

Frame Buffer Structure



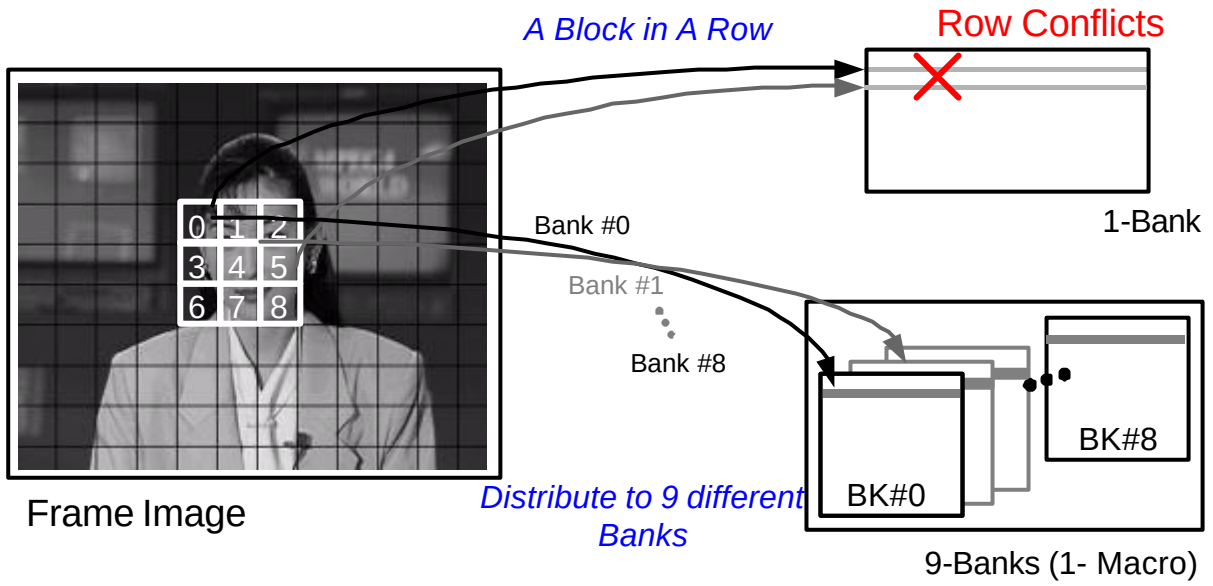
Memory Access Patterns





Center-Biased Nature of
Motion Vector Field

Distributed Nine-Tiled Block Mapping
: Low Power Technique (1)

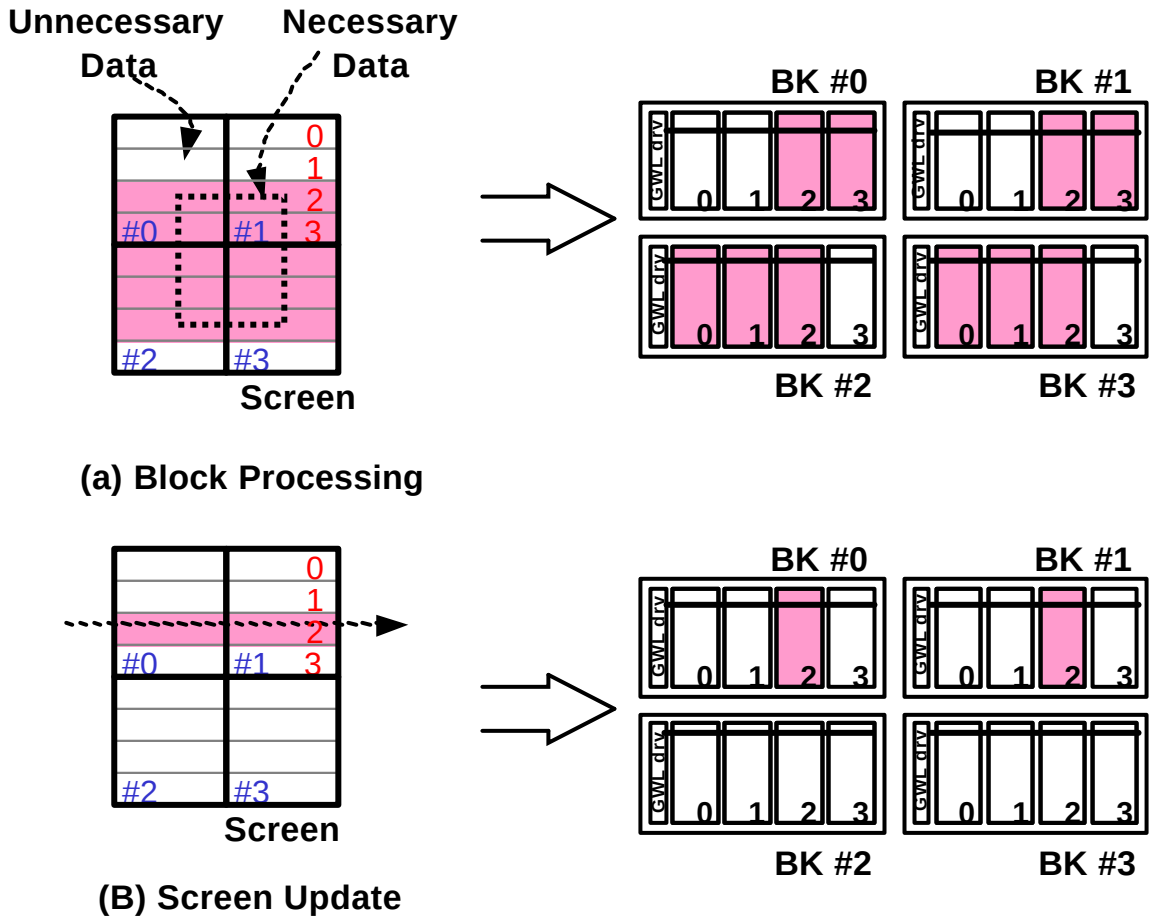


Increasing
Re-usability of DRAM Rows

Minimizing
Cell Core Activation in DRAM

Partial Activation Control Scheme

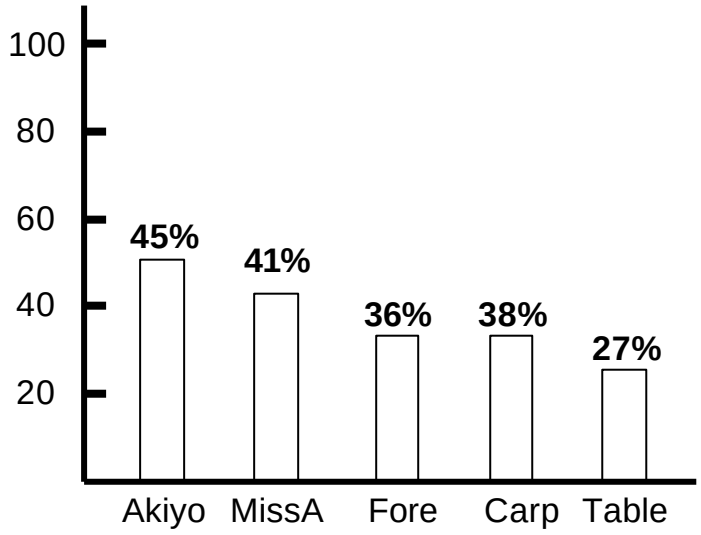
: Low Power Technique (2)



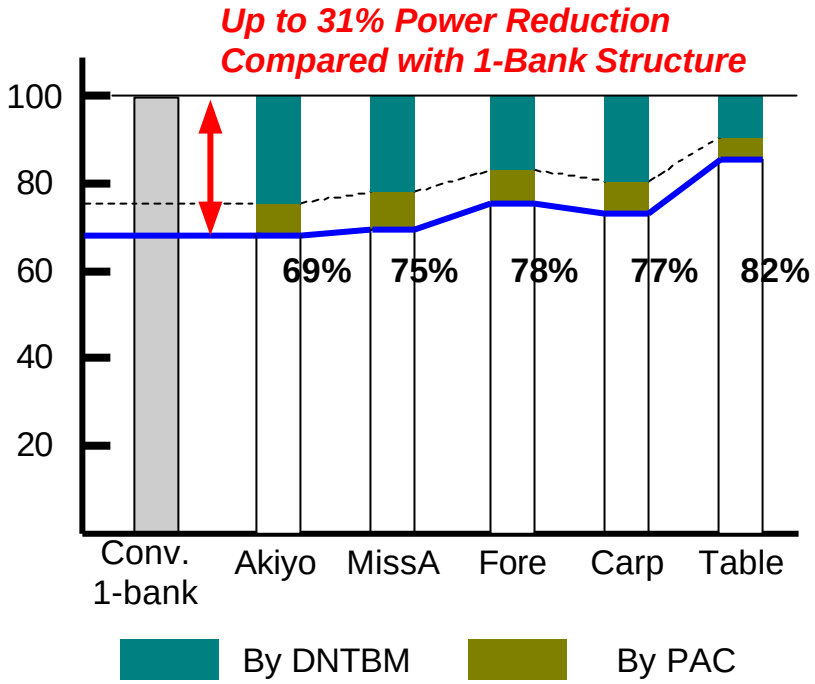
(a) Block Processing

(B) Screen Update

Power Savings

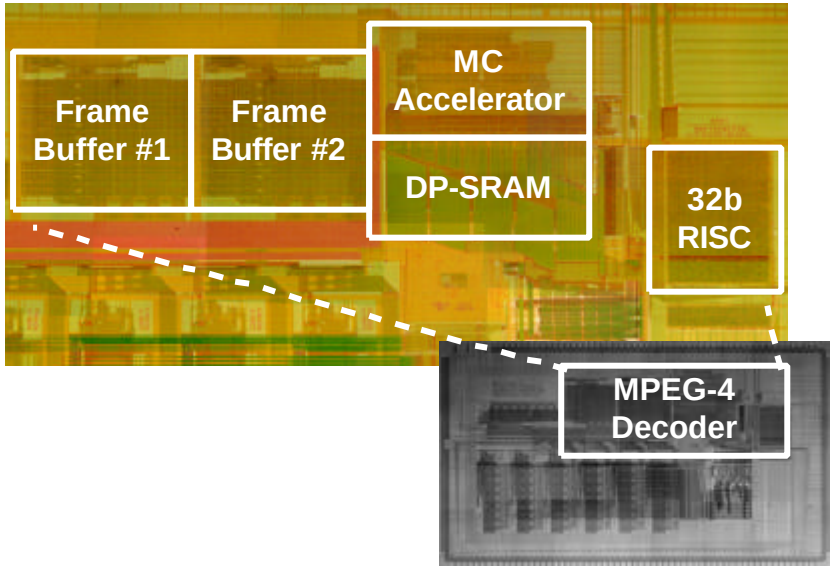


Row Reusability



Power Reduction

Implementation Results



Technology	0.18um EML technology with 3-poly, 6-metal	
	Logic	DRAM
Area (mm^2)	2.3 mm^2	5.25 mm^2
Power Supply	1.5 V	2.5 V
Clock Frequency	20 MHz	20 MHz
Power	4.6 mW	11.7 mW
DRAM Capacity	1.125 Mbit 2 x (512bit x 128row x 9bank)	
Target Functionality	MPEG-4 SP@L1, H.263, H.263+	

[Ref] C.W. Yoon et al, "A 80/20MHz ~", JSSC 2001

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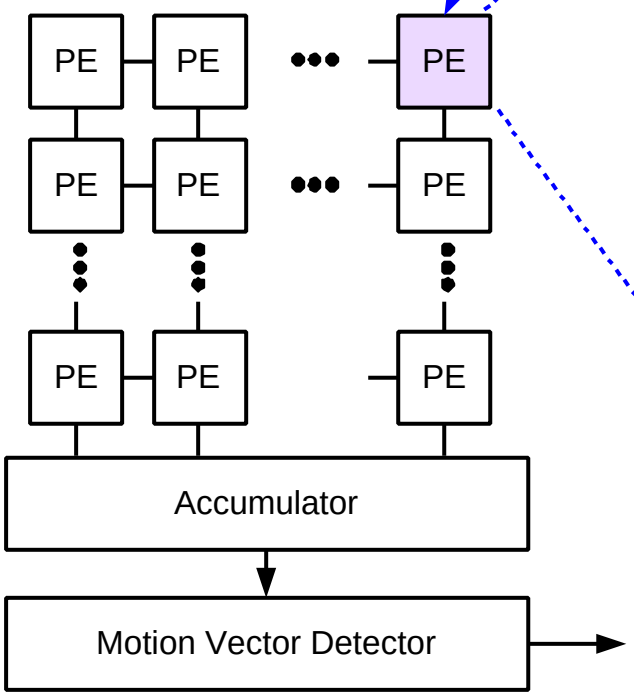
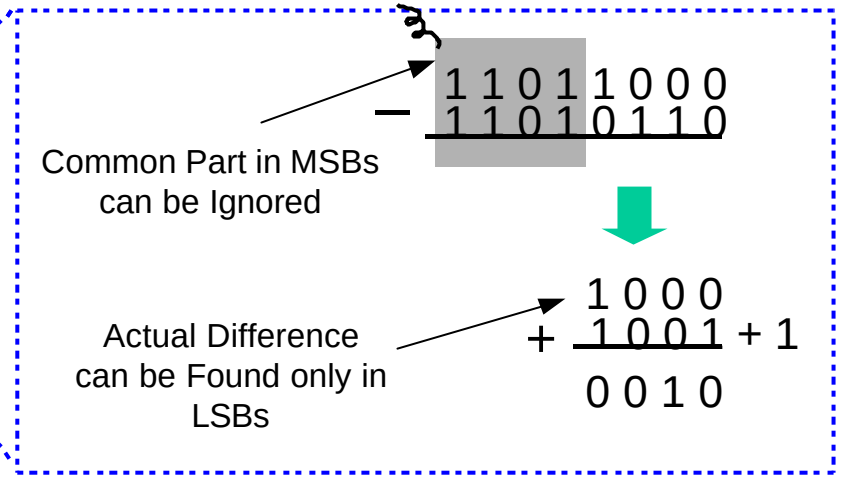
Concept of Adaptive Bit-Resolution Control Scheme

$$SAD(i,j) = \frac{1}{MN}\sum_{k=0}^{M-1}\sum_{l=0}^{N-1}\left|C_{i,j} - R_{i,j}\right|$$

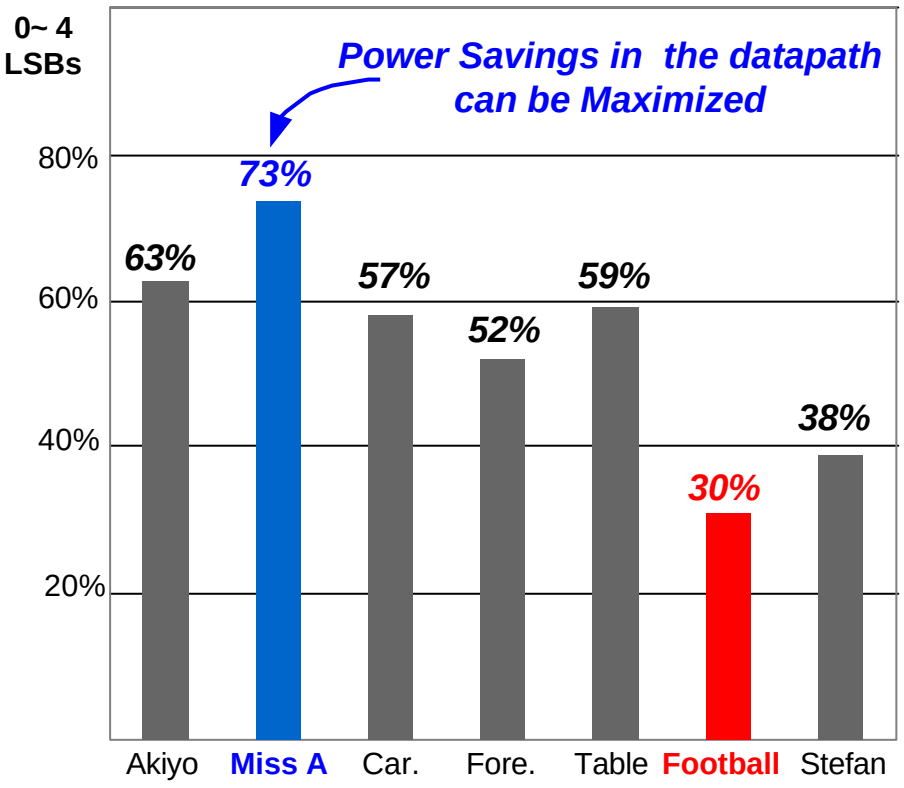




Reduced bit Operation in Hardware

Redundant Transitions in Datapath are Reduced

Bit Resolution Distribution



Full Search *[-16, 15.5]*

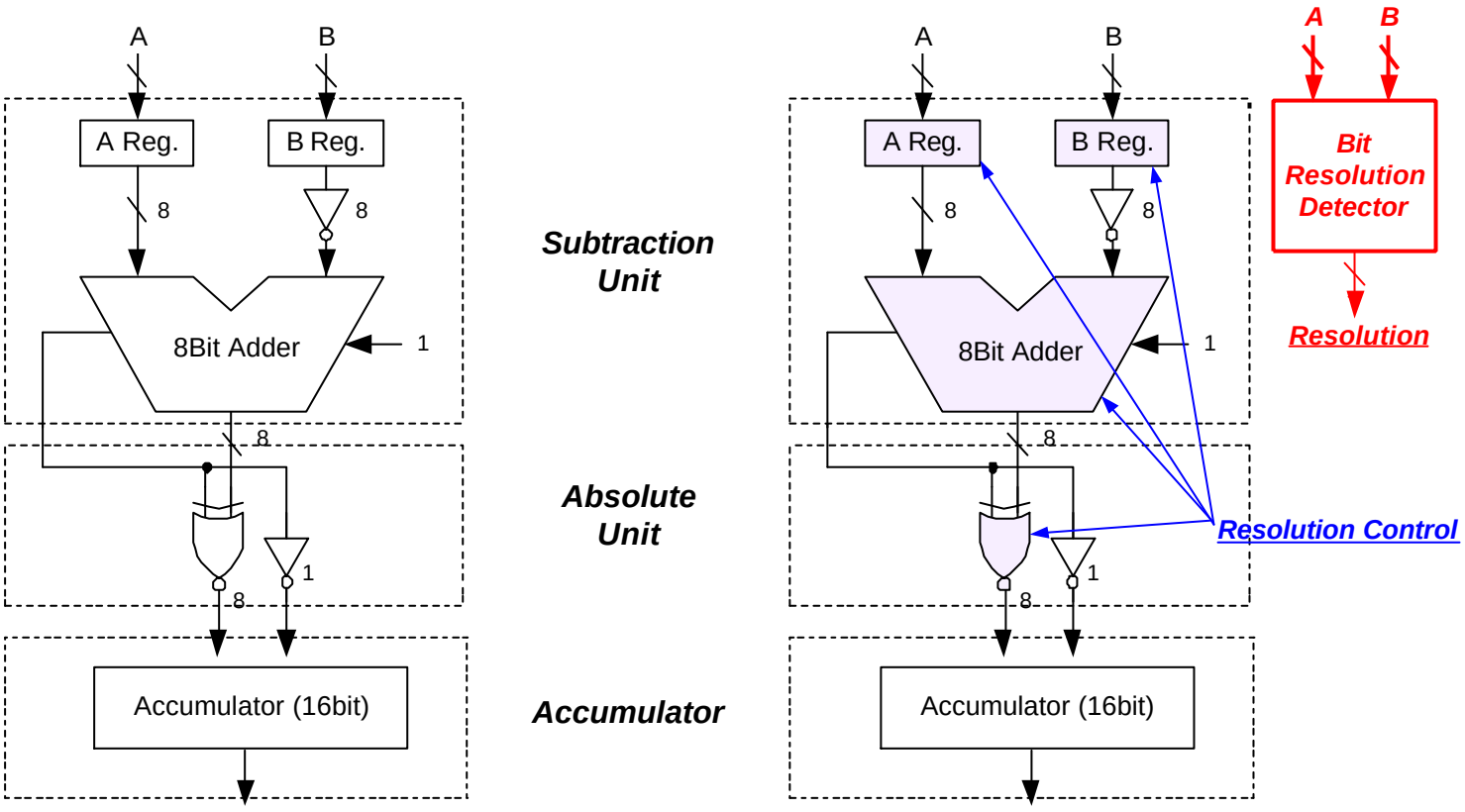
Constant Color & Small Movement

Miss America

Contains many of fast moving objects

Football

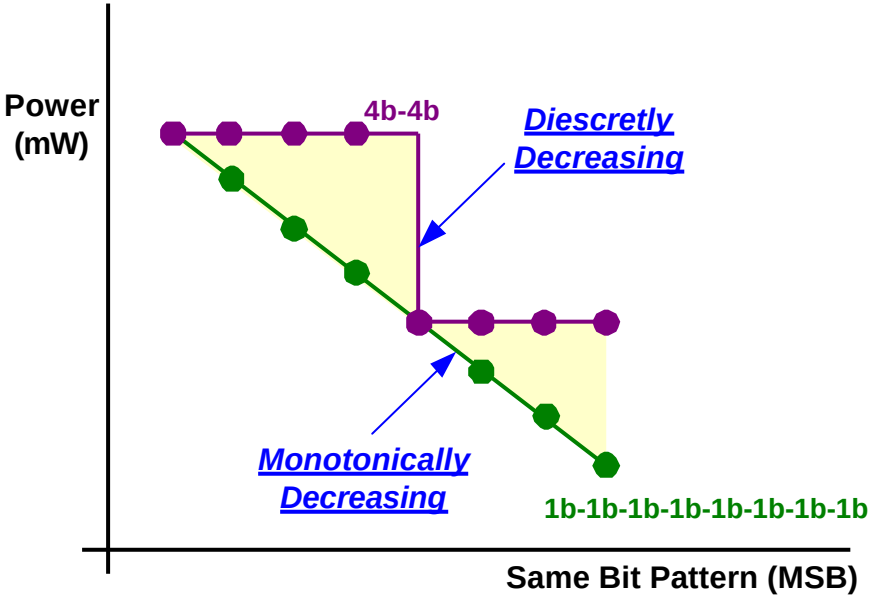
Circuit Implementation



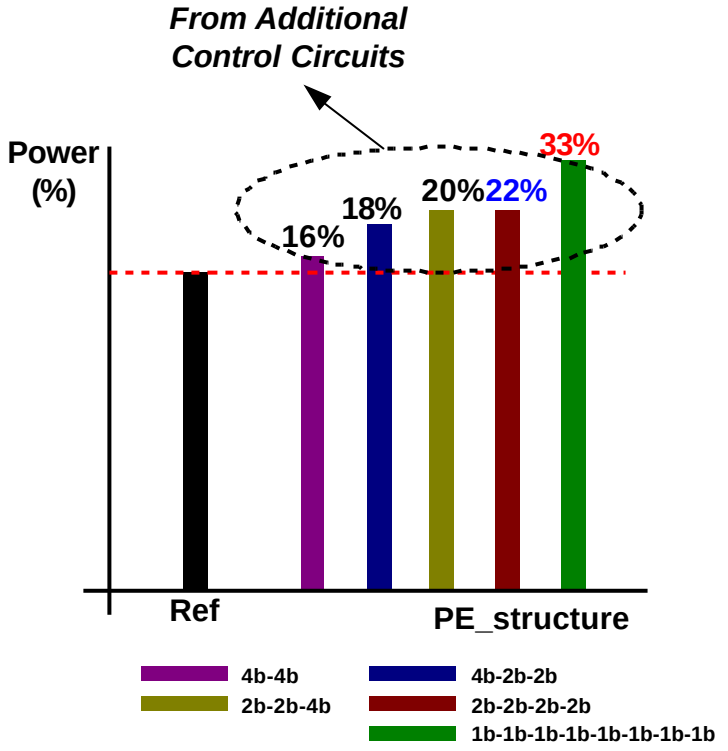
Conventional PE

PE with ABRC

Trade-off (1) : Power

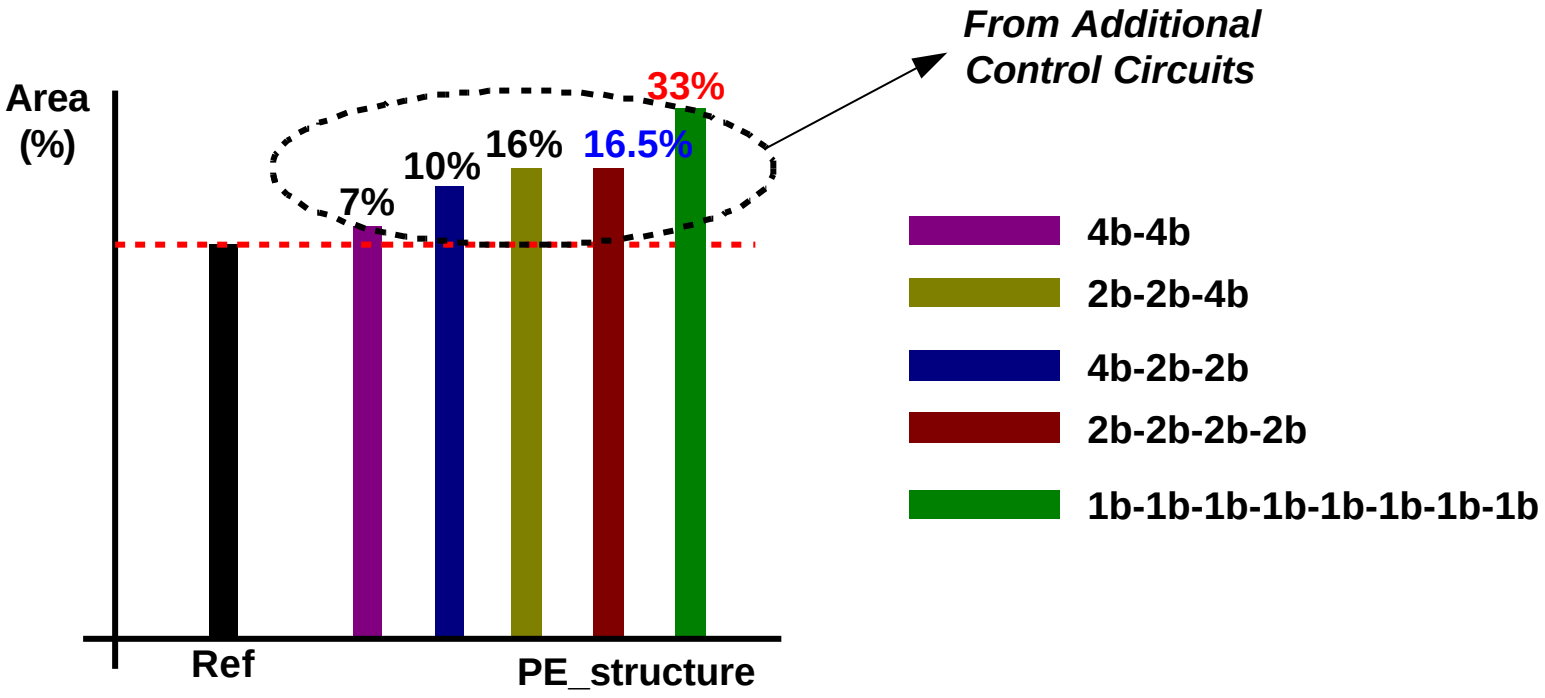


Power (Datapath)

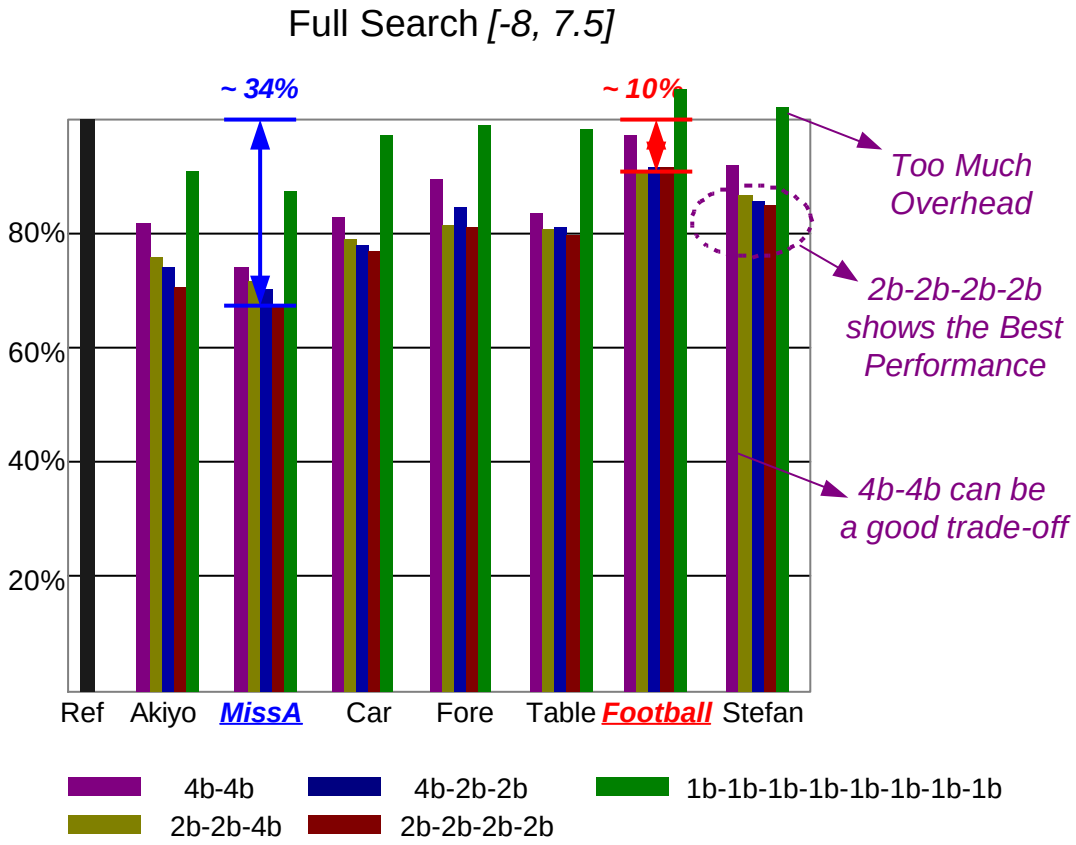


Power (Control Circuits)

Trade-off (2) : Area



Power Savings



P. Savings for Various Algorithms

Method	Max	Min.
FS [-16, 15]	39%	15%
BBGDS [-8,7]	***41%***	***13%***
BBGDS[-16,15.5]	39%	10%

Conclusions

- **Low Power MC Accelerator For Portable Applications**
  - ***Optimized Architecture in terms of Low Power Consumption***
    - **Various Low Power techniques**

- **Low Power PE for Systolic Array-based ME**
  - ***Adaptive Bit Resolution Control*** **according to Operands**
    - **10~40% Power Savings in Datapath**
    - **Without any sacrifice of Calculation accuracy**
  - **Comparison of Various PE structure**
    - **PE with 2b Granularity Control scheme shows the best performance**
    - **PE with 4b Granularity can be a good trade-off**