Low Power Motion Compensation Block IP with embedded DRAM Macro for Portable Multimedia Applications

Chi-Weon Yoon*, Jeonghoon Kook, Ramchan Woo, Se-Joong Lee, Kangmin Lee and Hoi-Jun Yoo

Semiconductor System Laboratory
Department of Electrical Engineering
Korea Advanced Institute of Science and Technology (KAIST)
Outline

• Introduction
• Motion Compensation Accelerator
  • Overall Architecture
  • Low Power Designs
• Example System
• Implementation
• Conclusions
Introduction

Various Portable Multimedia Applications
2D Image Processing
(Decoding)

Hardware Implementation

Most Computation-Intensive Part in Video Decoding

Coded Data

VLD

Inverse Scan

I- AC/DC Prediction

Inverse QT.

Inverse DCT

Motion Compensation

Decoded Pels

VOP Memory

Intensive Memory I/O

Prediction Error
Motion Compensation (MC) Accelerator

Frame Buffers (Embedded DRAM)
- Internal Data Transactions (128b)
- Distributed Nine-Tiled Block Mapping
- Partial Activation
- Partial I/O control

Datapath (Logic)
- Scanline Buffer
- Pixel Selection
- HPel ALU Array #0 ~ #7
- Pixel Alignment
- Pixel ALU Array #0 ~ #7
- Line Selection
- Pixel Buffer

Adaptive Fetch Control
Parallel Pixel Processing
Prediction Error

20MHz

I/O
Frame Buffer #1
Frame Buffer #2

I/O
Frame Buffer Structure

9 Banks

Shared I/O (128b)

Bank #0
(128b x 128row x 4seg)

PA_Ctrl

PIO_Ctrl

MWL

SWL

Seg3

Seg2

Seg1

Seg0

#1

#8

IO_En

PIO_Ctrl
Memory Access Patterns

- Screen Out (1 Line)
- Data Processing (1 Block)
- Required Pixels in a MB
- Required Blocks for Reconstruction
- Reusable Blocks

Large Spatial Locality
Distributed Nine-Tiled Block Mapping & Partial Activation Control Scheme

Mapping Adjacent Blocks to Different Banks

Minimizing # of Cell Core Activation

Bank #0

Bank #1

Bank #8

Bank #2

Bank #8

A block in a Row

Partial Activation

Activating only Necessary Parts

Ref : C.W. Yoon et al, "A 80/20MHz 160mW Multimedia ~", ISSCC2001
Row Reusability

Up to 31% Power Reduction Compared with 1-Bank Structure

Row Reusability

Car: 39%, Cla: 26%, Fmn: 45%, Miss: 27%

Power Reduction

Car: 73%, Cla: 82%, Fmn: 69%, Miss: 80%, 1-Bank Structure: 100%
Frame Buffer Operations

Burst Read

BL 2 Read
(Screen Out)

BL 4 Read
(Pixel Processing)

BL<1,2,4>

DFF

CLK

EXT_Yaddr

<1:0>

To
Y-Dec

ICAS#

EXT_CAS#

CAS#

Burst Controller

CLK

DFF

DFF

EXT_Yaddr

<1:0>

ICAS#

EXT_CAS#

CAS#

Dout

Clk

CAS#

BL4

BL2

1 0 1 0 1 0 1 0
Sequential Pixel Scan

Sequentially Scan 18 Pixels

Horizontal Data Buffering

Vertical Data Buffering

Required Pixels (9x9)

8x8 Block Reconstruction

\[
\begin{array}{c}
0 & 1 \\
0 & 1 \\
2 & 3 \\
\end{array}
\]
Pixel Alignment

Scanline Buffer
- Pixel Selection

8x8 Barrel Shifter
- sel<lb>
- in<lb>
- out<lb>

HPEL ALU Array
- #0 ~ #7

Pixel ALU Array
- #0 ~ #7

Line Selection
- Pixel Buffer

Time Flow

Offset

Shift L : offset

0 1 2 3 4 5 6 7

Shift R : (6 - offset)

0 1 2 3 4 5 6 7

Reconstructed Pixels

IDCT Data

Compensated Data
Adaptive Fetch Control Scheme

Up to 29% Power Reduction

No transitions
Half-Pel ALU

<table>
<thead>
<tr>
<th>Pel</th>
<th>halfx / halfy</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>d</td>
<td>00</td>
<td>D</td>
</tr>
<tr>
<td>b</td>
<td>01</td>
<td>(B+D +1 - Round) / 2</td>
</tr>
<tr>
<td>d</td>
<td>10</td>
<td>(C+D +1 - Round) / 2</td>
</tr>
<tr>
<td>a</td>
<td>11</td>
<td>(A+B+C+D+2 - Round) / 4</td>
</tr>
</tbody>
</table>

MPEG-4 : Round

MPEG-4 & H.263 Compatible

No Division
Example System

MPEG-4 Video SP@L1 Decoding System
Die Photograph

Ref: C.W. Yoon et al, "A 80/20MHz 160mW Multimedia ~", ISSCC2001
## MCA Features

<table>
<thead>
<tr>
<th>Technology</th>
<th>Logic</th>
<th>DRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>0.18um EML technology with 3-poly, 6-metal</td>
<td></td>
</tr>
<tr>
<td><strong>Area (mm²)</strong></td>
<td>2.3 mm²</td>
<td>5.25 mm²</td>
</tr>
<tr>
<td><strong>Power Supply</strong></td>
<td>1.5 V</td>
<td>2.5 V</td>
</tr>
<tr>
<td><strong>Clock Frequency</strong></td>
<td>20 MHz</td>
<td>20 MHz</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>4.6 mW</td>
<td>11.7 mW</td>
</tr>
<tr>
<td><strong>DRAM Capacity</strong></td>
<td>1.125 Mbit</td>
<td>2 x (512bit x 128row x 9bank)</td>
</tr>
<tr>
<td><strong>Target Functionality</strong></td>
<td>MPEG-4 SP@L1, H.263, H.263+</td>
<td></td>
</tr>
</tbody>
</table>
Measurement Results

![Waveform Diagram with Clk, Dout0, and Dout1 signals with 20MHz frequency]
Conclusions

• **Low Power MC Accelerator for Portable Multimedia Applications**
  – Logic + Embedded DRAM

  – Support Various Video Compression Standards
    • MPEG-4 SP@L1, H.263

  – Low Power Designs
    • Distributed Nine-Tiled Block Mapping
    • Partial Activation, Partial I/O scheme
    • Adaptive Fetch Control Scheme