A 80/20MHz 160mW Multimedia Processor integrated with Embedded DRAM, MPEG-4 Accelerator and 3D Rendering Engine for Mobile Applications

Chi-Weon Yoon, Ramchan Woo, Jeonghoon Kook, Se-Joong Lee, Kangmin Lee, Young-Don Bae, In-Cheol Park and Hoi-Jun Yoo

Dept. of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Korea
Outline

• Introduction
• System Architecture Overview
• Low Power Block Design
  • 32Bit RISC
  • MPEG-4 Accelerator
  • 3D Rendering Engine
  • Embedded DRAM Frame Buffer
• Features of Test Chip
• Conclusions
Requirements for Future Mobile Information Terminals

• Multimedia Signal Processing
  – mp3, 2D Image Processing, etc.
  – 3D Graphics

• Low Power Features
  – Battery-driven Products

• Low Cost Solutions
  – Major Factor for Consumer Electronics
Target Specifications

3D Image Rendering
- > 2 Mpolygons /sec
- 256 x 256 Resolution with 24b True Color
- 16b Z-Buffering
- Alpha Blending
- Double Buffering

System Power
- < 200mW

Low Power Multimedia Processor

MPEG-4 Video Decoding
- Simple Profile
- QCIF(176 x 144)
- 15 frames /sec

Others
- mp3, etc.
The Proposed Solution

**H/W & S/W Mixed Solution**
Optimized at Architecture / Circuit Level

- High Perform. CPU
- Optimized Perform. CPU
- Dedicated H/W
- Embedded DRAM

- Large Area
- High Power Consumption
- Distribution of Computational Load
- Small Area
- Programmability
- Circuit Level Low Power Techniques
Architecture Overview

Fast / Narrow Data Transaction (32b @ 80MHz)

Data Buffering

Slow / Wide Data Transaction (512b @ 20MHz)

On-Chip Wide Bus between Logic / eDRAM

Ext. I/O

ARM9

MAC

32b

B.W. Equalizer

Dual-Port SRAM (2KB)

512b

20MHz

3D Rendering Engine

MC Accelerator

128b

Frame Buffer + Z-Buffer

2048b

YCrCb to RGB

SAM

80MHz

Data Buffering

Color Out (24b)

Slow / Wide Data Transaction (512b @ 20MHz)

On-Chip Wide Bus between Logic / eDRAM

Ext. I/O

ARM9

MAC

32b

B.W. Equalizer

Dual-Port SRAM (2KB)

512b

20MHz

3D Rendering Engine

MC Accelerator

128b

Frame Buffer + Z-Buffer

2048b

YCrCb to RGB

SAM

80MHz

Data Buffering

Color Out (24b)
Multimedia Enhancement in RISC

- 5-Stage Pipeline
- Execution Units
- Tree Structure with 4:2 Adders

- 1-Cycle 32b x 32b Multiplication
- 2-Cycle 32b x 32b Multiplication and Accumulation
- 23% Cycle Reduction Compared with Conventional ARM Architecture
Bandwidth Equalizer

From RISC
32b @ 80MHz

Flow Cont.
32
DP-SRAM (2KB)
512b

To Dedicated H/W
512 (32)b @ 20MHz

Single Ended
for Tight Bit Pitch

Act as
A Row Cache

WBE : Wide Bus Enable
STR : Cache Store
DDO : Direct Data Out
Motion Compensation (MC) Accelerator

FB Cont | Frame Buffer #0 (512b x 128row x 9bank) | FB Cont | Frame Buffer #1 (512b x 128row x 9bank)

128b (16 Pixels)

Pixel Buffer

MUXing Logic

Pixel ALU #0

Data Alignment

Half-Pel ALU #0

MUXing Logic

FB Buffer

Adaptive Fetch Control

Parallel Operation @ 20MHz

20MHz

512b

128b (16 Pixels)

512b (16 Pixels)
Frame Buffer for MCA

9-Bank with 128b I/O

Sub-wordline with Partial Activation, Partial I/O Scheme
Spatial Locality

- Blocks to be Reconstructed
- Needed
- Previously Used
- Commonly Used
- Newly Needed

70~90% are Confined in 8x8 Boundary

Large Spatial Locality

Distribution of Motion Vectors for Class A/B (MVx, MVy)

Re-usable Block
Distributed Nine-Tiled Block Mapping: Low Power Technique (1)

- Minimizing Cell Core Activation in DRAM

Diagram:
- A Block in A Row
- Row Conflicts
- Bank #0
- Bank #1
- Bank #8
- BK#0
- BK#8
- Frame Image
- Increasing Re-usability
- 1-Bank
- 9-Banks (1- Macro)
Partial Activation Scheme

: Low Power Technique (2)

Unnecessary Data

Necessary Data

Normal Operation

Partial Activation

SAM Transfer

DNTBM + Partial ACT

Up to 31% Power Reduction Compared with 1-Bank Structure
Adaptive Fetch Control Scheme

: Low Power Technique (3)

Block-by-Block Reconstruction

No Switching in Datapath

Adaptive Fetch Control

Valid Data

Garbage Data

FP Buffer

Muxing Logic

PE #0

PE #1

PE #2

PE #3

PE #4

PE #5

PE #6

PE #7
3D Rendering Engine

Bandwidth Equalizer

Polygon Buffer

Left

Right

1-Edge Processor

Calculating 8 Pixels/Cycle

Parallel Datapath for RGB and Z

Frame-Buffer Interface

Old Pixel (RGBZ)

Shading

Blending

Z-Unit

Depth Comparison

New Pixel (RGBZ)

Update

1280b

20MHz
ViSTA Architecture

- Virtually Spanning 2D Array (ViSTA) Architecture

![Diagram of ViSTA Architecture]

Previous Work (ISSCC2000 TP14.7)

1/8 Scaling

Virtually Spans 2D Array

This Work (ViSTA)

- 8 EP's
- 64 PP's

Parallel EP

1 EP

8 PP's

8-Stage Pipelined EP

Dynamic Bus Reconfiguration
Frame Buffer for 3DRE

\[
1280b \times 20MHz = 3.2GB/sec
\]

From Pixel Processors

Concurrent Data Transfer

640b

768b

24b

True Color

SCLK

Write

Read

Depth Buffer

Frame Buffer #0

Frame Buffer #1

512kb DRAM

512kb DRAM

512kb DRAM

512kb DRAM

512kb DRAM

512kb DRAM

Interchangeable Double Color-Buffers
Single Bitline Writing Scheme

: Low Power Technique (4)

No Transitions in /BL

Single Bitline Writing

8Kb Cell Array with 2K Column

- Periphery & Control: 30.47 mW
- Data Sensing: 15.0 mW

$20\%$ Power Reduction in Data Sensing
System Power Consumption

Power Consumption Comparison:

- Conventional Design - I (Ext. FB)
  - 25mW
  - 50mW
  - 75mW
  - 100mW
  - 125mW
  - 150mW
  - 175mW

- Conventional Design - II (Embedded FB)
  - 175mW

- Proposed System
  - 160mW

By Embedding eDRAM Macro, this work reduces the power consumption significantly compared to conventional designs.

This Work

160mW
Die Photograph

- 0.18um EML Technology with 3-poly, 6-metal
- 240pin QFP
- 84mm² (14 x 7 Including I/O Cells)
Chip Features (Physical)

- MC Accelerator:
  - 80MHz
  - 1.5V
  - 12mW
  - 1.7mm²

- B.W. Equalizer:
  - 80/20MHz
  - 1.5V
  - 4.6mW
  - 2.3mm²

- ARM9:
  - 20MHz
  - 1.5V
  - 4.6mW
  - 2.3mm²

- I/O Cells: 3.3V

- 3D Rendering Engine:
  - 20MHz
  - 1.5V
  - 36mW
  - 5mm²

- Frame Buffer:
  - 20MHz
  - 2.5V
  - 11.7mW
  - 5.25mm²

- 3D Rendering Engine:
  - 20MHz
  - 2.5V
  - 84mW
  - 16.4mm²

- I/O Cells: 3.3V

- < 40mW

- < 140mW
Conclusions

• **Low Power Multimedia Processor** for Mobile Applications
  – Optimized H/W & S/W Mixed System
  – Multimedia Signal Processing
    • Not only 2D Image, But also *3D Graphics*
  – Low Power Techniques
    • Distributed Nine-Tiled Block Mapping
    • Partial Activation, Partial I/O scheme
    • Adaptive Fetch Control Scheme
    • Single Bitline Writing Scheme

• 160mW, 84mm²