A 120mW Embedded 3D Graphics Rendering Engine with 6Mb Logically Local Frame-Buffer and 3.2GByte/s Run-time Reconfigurable Bus for PDA-Chip

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Outline

- Introduction
- Frame Buffer and Bus Architecture
- Line Block Memory Mapping
- Power Reduction Techniques
- Implementation Results
- Conclusion
Mobile Multimedia Era

- Polygon Data over Wireless Network
  - 3D Fax
  - 3D Game
  - 3D Advertisement

- Realtime Audio
- Realtime Video
- 3D Graphics

Multimedia PDA
3D Graphics on PDA

- Low Power
- Small Area
- High Performance
8-pixel-parallel rendering at every clock cycle
Conventional Frame Buffers - 1

- Local Frame Buffer

- High Memory Bandwidth
  - Parallel access via local routes

- Low Power
  - Selective Activation

- Large Area
  - Poor DRAM Cell Efficiency
Conventional Frame Buffers - 2

- **Global Frame Buffer**

  - Smaller Area
    - High Cell Efficiency
  - Low Memory Bandwidth at Low Clock
    - Sequential Access with bank interleaving
  - Large Power Consumption
    - Rectangular memory mapping
Logically Local Frame Buffer

- Small Area
  - High DRAM Cell Efficiency
- High Memory Bandwidth
  - Parallel access through R2bus
- Low Power
  - Selective Activation
Line Block Memory Mapping - 1

Each adjacent Line Block is mapped onto different macro unit

Line Block = 8x1 screen pixels
Line Block Memory Mapping - 2

Selective Activation to Reduce Power

Macro A0, B0
READ V2
WRITE
READ V4
WRITE
Simultaneous Read-Modify-Write

Macro A1, B1
WRITE
READ
WRITE
READ

Continuous Pixel Processor Operation

Select the appropriate clock frequencies and memory mapping for efficient operation.
Power Reduction Techniques - 1

- Selective Macro Activation (SMA)

More than 90% lines in polygons require only one macro activation

Screen
Power Reduction Techniques - 2

- Partial Wordline Activation (PWA)

One Line Block activates only one Sub-Wordline

SWL driver

GWL driver

eDRAM Macro
Power Reduction Techniques - 3

• Partial I/O Activation (PIA)

![Diagram showing Partial I/O Activation (PIA)]

- Inactive I/O Bus
- active I/O Bus
- eDRAM Macro

Disable
Unnecessary
DBSA by I/O Mask

0 0 0 0 0 1 1 1

GWL drv
SWL drv
S/A

DBSA
REN
REN
REN

0
0
0
0
0
0
0
0

1
1
1
1
1
1
0
0

0
Run-time Reconfigurable Bus

Bidirectional Memory Bus
x1280

Cascaded 2-to-2 MUX
(inter-bus)

16-to-8 Bus-Shifter
(intra-bus)

Omnidirectional PP Bus
x640

A0
(x320)

A1
(x320)

B0
(x320)

B1
(x320)

1280bits Bus Reconfiguration
@ 20MHz = 3.2GByte/s
Operations of R2bus

(a) Normal Rendering  (b) Individual Activation  (c) Broadcasting
Area and Power Reduction

Area (mm²)

- Logic
- eDRAM Core
- eDRAM Peri

25% Area Reduction

Power (mW)

- Logic
- eDRAM Core
- eDRAM Peri and I/O Bus

70% Power Reduction
Rendering Engine in PDA-Chip

- External Polygon Database
  - External Memory
  - Wireless Network

- 32bit RISC
- BEQ (SRAM)

- Other Hardware Blocks
- Rendering Logic
- R2bus
- Frame Buffer

- Embedded 3D Graphics Rendering Engine
- LCD - 24bit RGB Data
# Rendering Engine Features

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ramP-II Multimedia PDA-Chip
- 3D Rendering
- Personal Information Management
- MP3 Audio
- MPEG-4 Video

PDA-Chip : ISSCC2001 TP 9.2
Measured Waveforms

- REclk
- Sclk
- Dout[0]: 100ns
- Dout[1]: 01110
Conclusion

- **3D Graphics for PDA-Chip**
  - 24bit True Color on 256 x 256 LCD screen
  - 2.2Mpolygons/s

- **Embedded 3D Graphics Rendering Engine**
  - 6Mb Logically Local Frame Buffer
  - 3.2GByte/s Run-time Reconfigurable Bus
  - 25% Area Reduction
  - 70% Power Reduction

- **24mm², 120mW**