A 670ps, 64bit Dynamic Low-Power Adder Design

Ramchan Woo*, Se-Joong Lee and Hoi-Jun Yoo

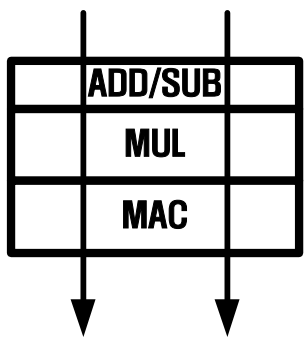
Semiconductor System Laboratory
Department of Electrical Engineering and Computer Science
Korea Advanced Institute of Science and Technology (KAIST)

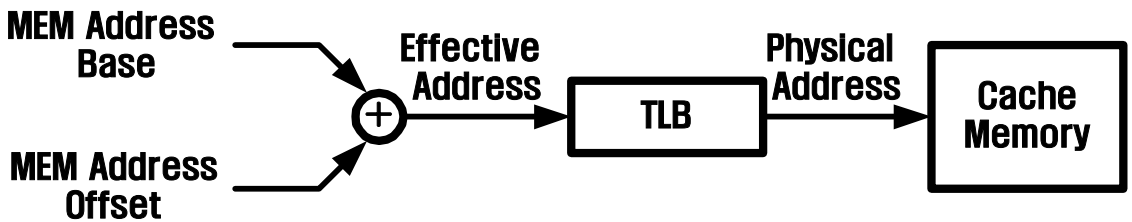
Outline

- Introduction
- Adder Design
  - Fast 'P' Generation
  - Carry Propagation Architecture and Circuit Implementation
- Adder Summary
  - Worst-case Waveforms
  - Features
- Conclusions

Introduction

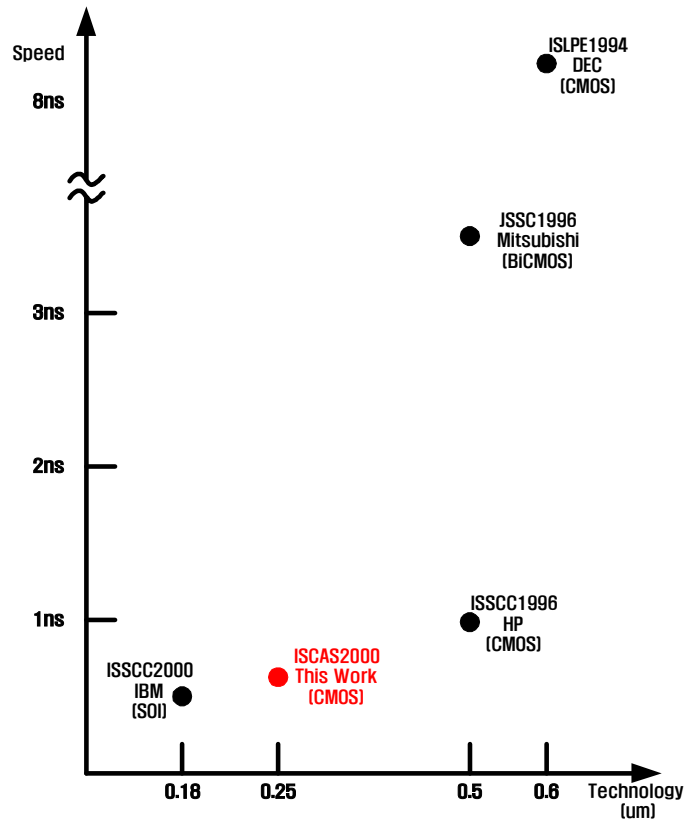
- Adders in High-Speed Microprocessor
  - High-Speed Data Path
  - Effective Address Calculation in Load/Store Unit





Introduction

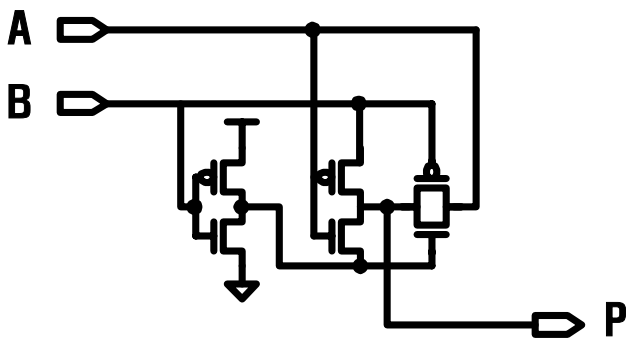
- Speeding-up the Adder in deep-submicron process technology
  - Fast 'P' Generation in Carry Look Ahead
  - Separated Carry Propagation Path
  - Efficient Carry Grouping to Extract More Parallelism
  - Simple Dynamic Circuits



Adder Speed Comparison

Fast P Generation

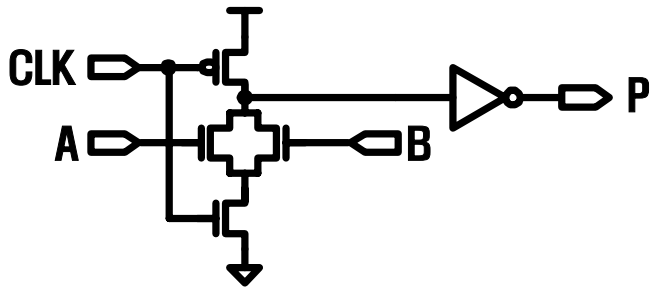
- Fast P Generation in Carry Look Ahead



Conventional XOR 'P' (XORP)

$$P = A \oplus B$$

$$G = A \bullet B$$



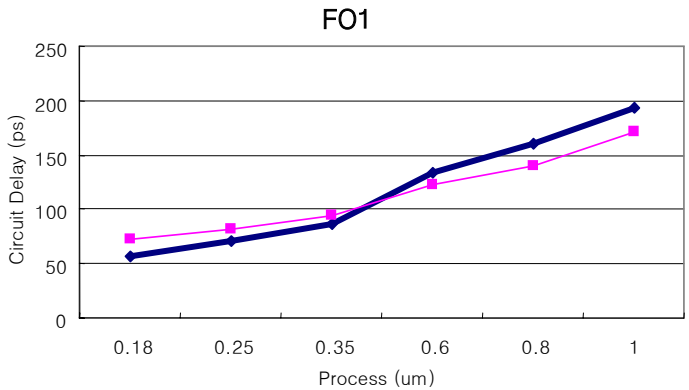
Proposed Dynamic-OR 'P' (DORP)

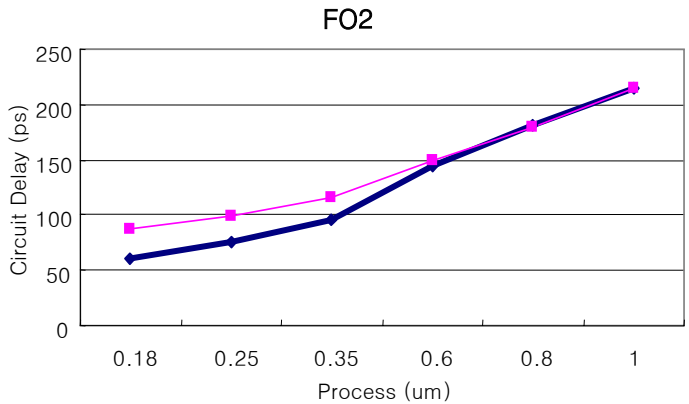
$$P = A + B$$

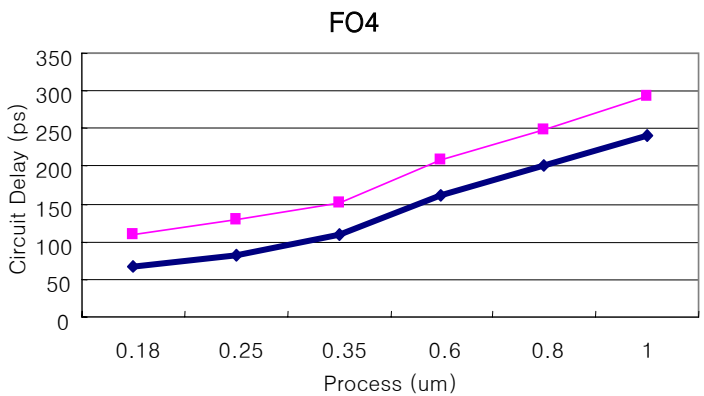
$$G = A \bullet B$$

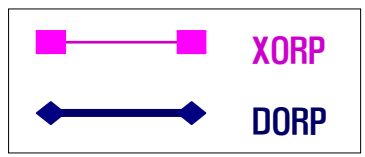
Fast P Generation

- DORP and XORP Simulation Results





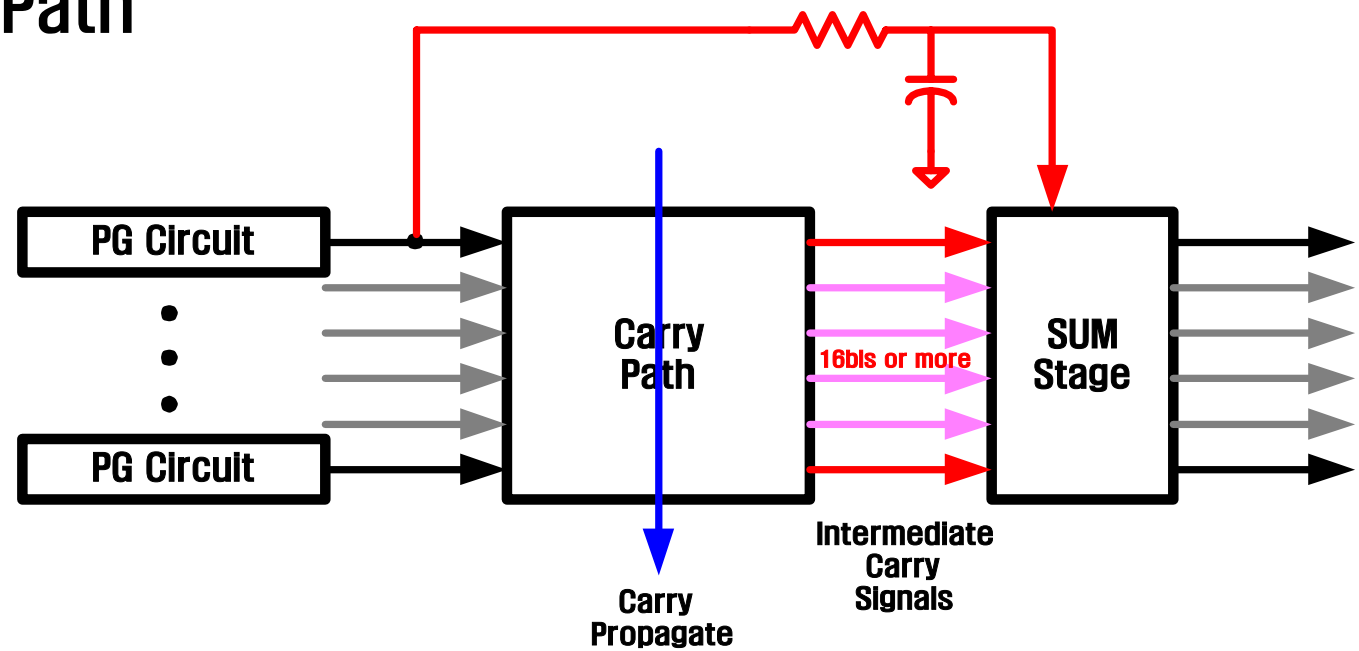




DORP is 30% Faster than XORP
@ 0.25μm

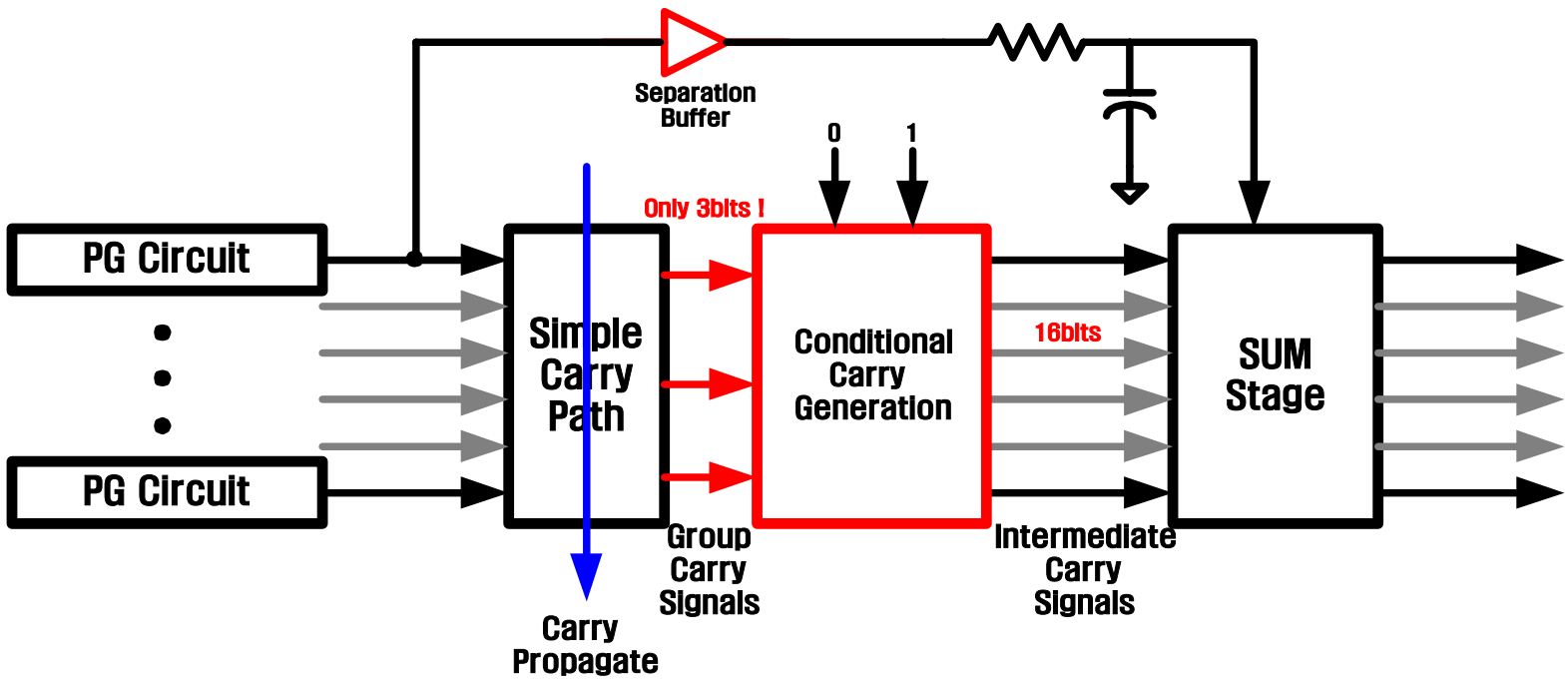
Separated Carry Propagation Path

- Conventional Carry Propagation Path
  - Large Capacitance Loading in PG and Carry Path
  - Increased Circuit Complexity in Carry Propagate Path



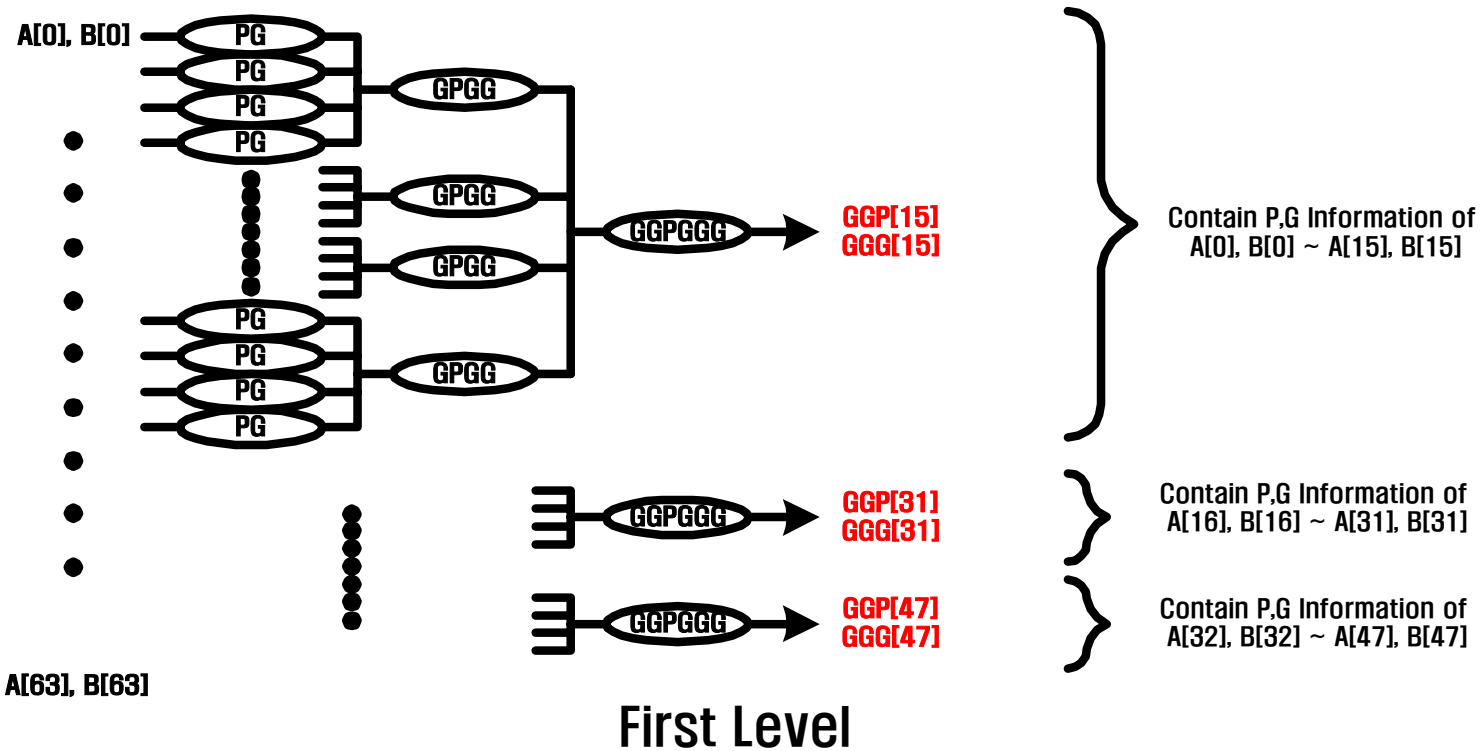
Separated Carry Propagation Path

- Proposed Carry Propagation Path
  - Reduced Capacitance Loading
  - Simple Circuits in Carry Path

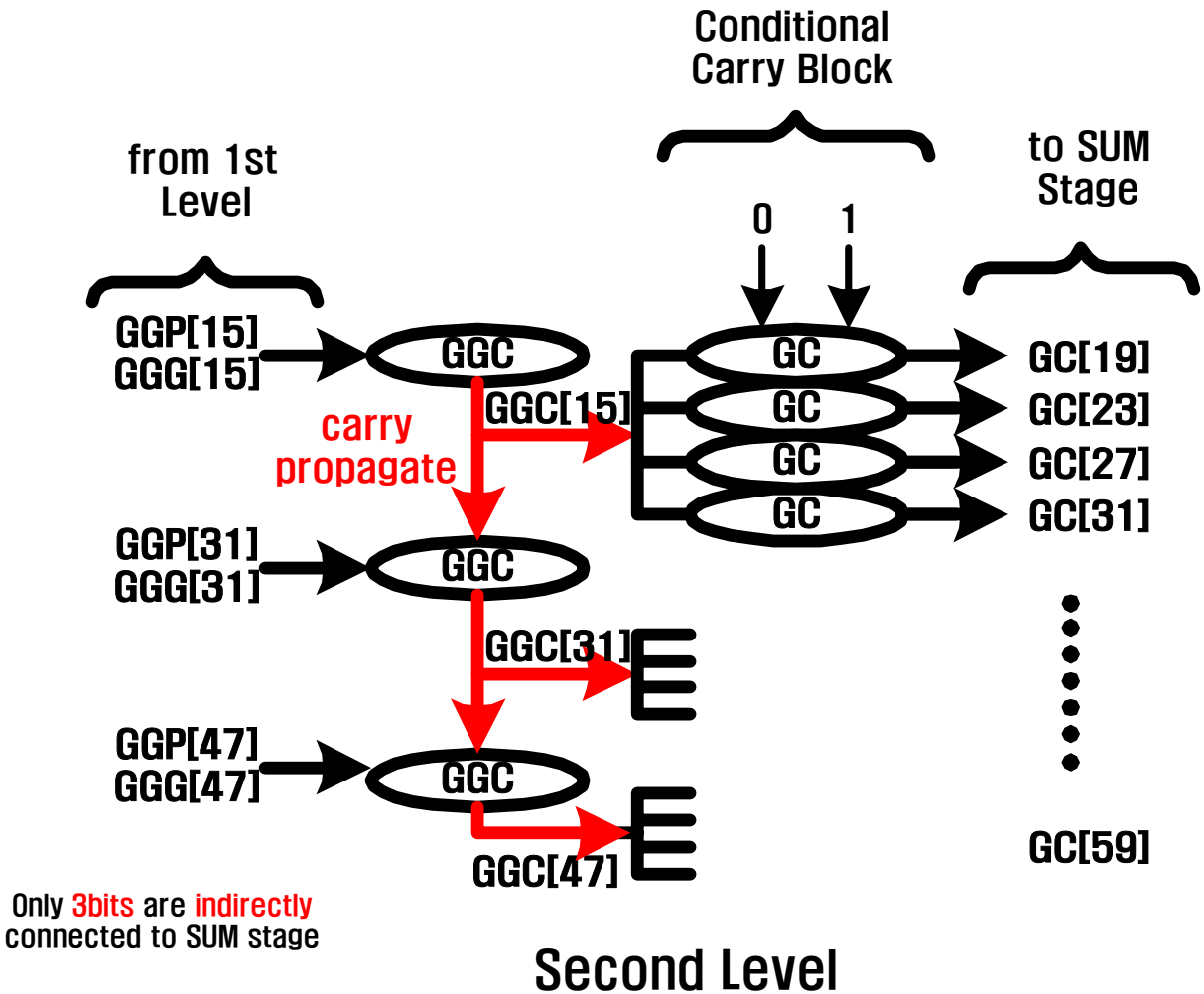


Efficient Carry Grouping

- Parallel Quaternary-tree form of Group Carry Selection

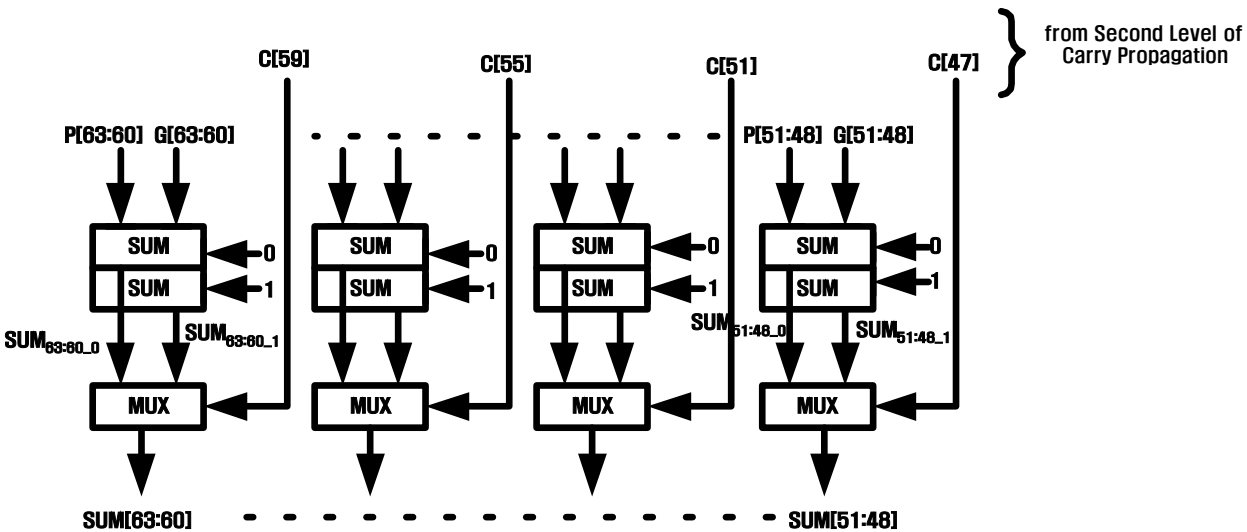


Efficient Carry Grouping



Conditional Sum Select

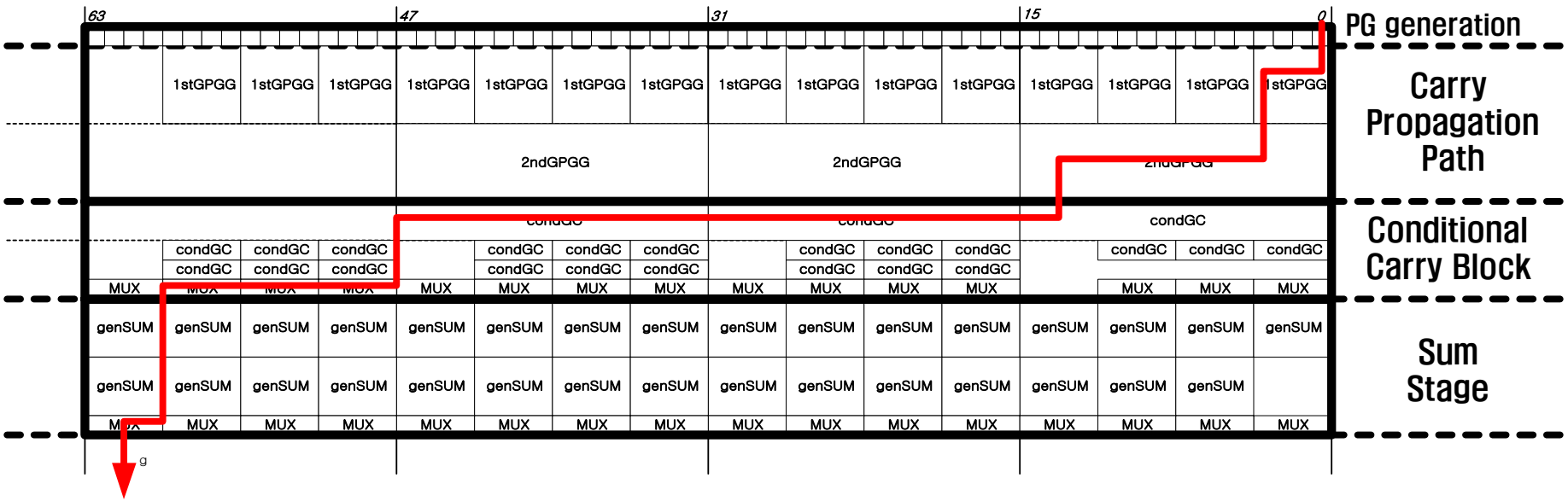
- 4bit Ripple-Carry SUM Blocks with Conditional Sum Select



Each SUM generation is changed because of Dynamic-OR 'P'

$$SUM[i] = G[i] \bullet C[i-1] + G'[i] \bullet (C[i-1] \oplus P[i])$$

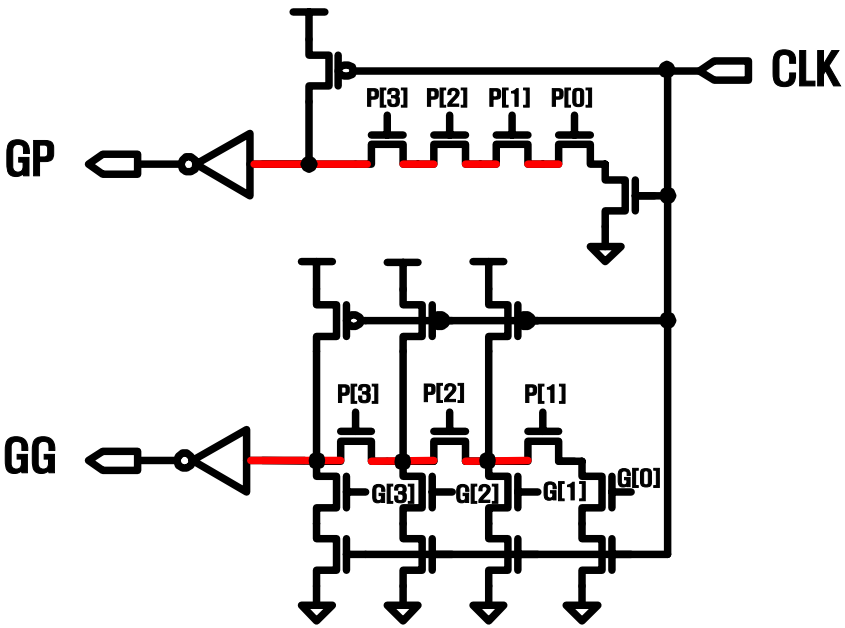
Floorplan and Carry-Path



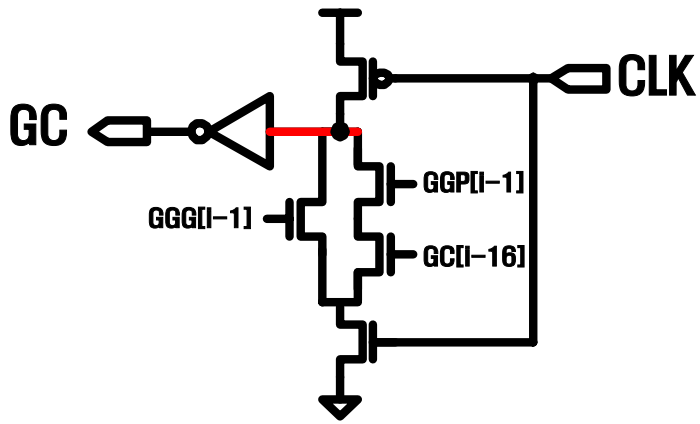
Carry passes only 8 Blocks

Circuit Implementation

- Simple Dynamic CMOS Circuits



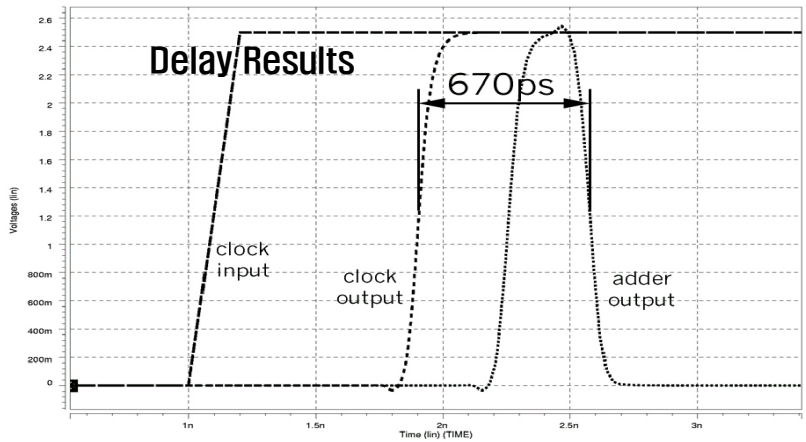
GP/GG Generation

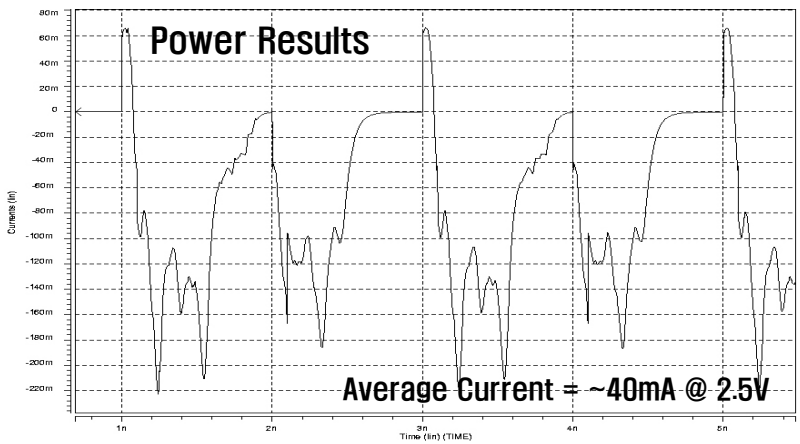


GC Generation

25% Speed-Up due to Small Junction Capacitance

Adder Summary

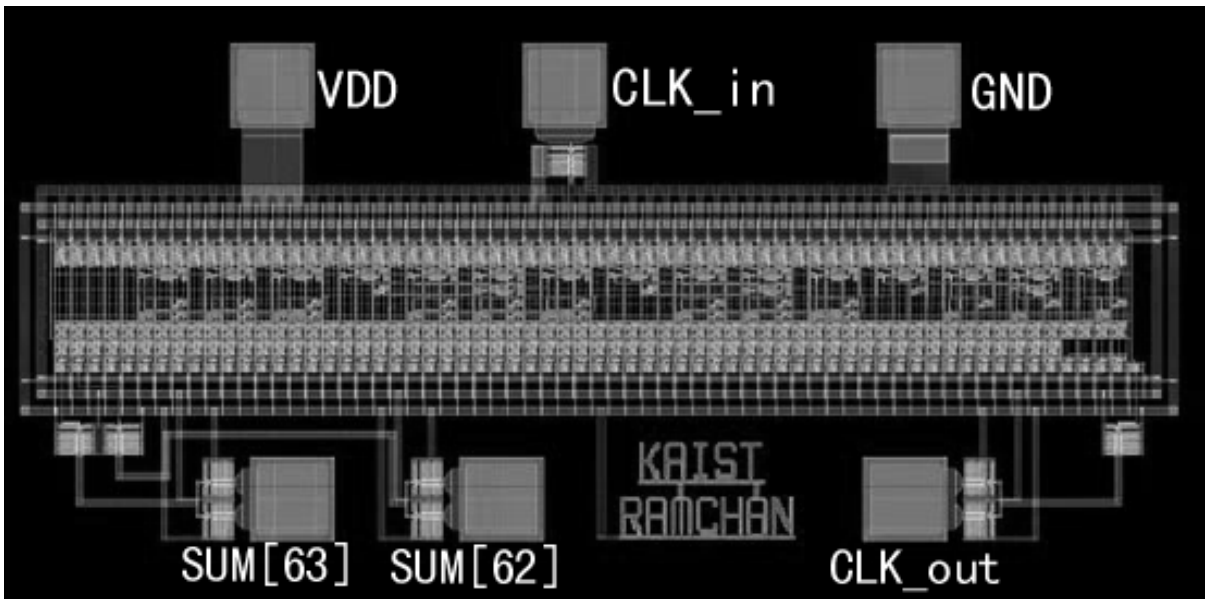




Process	0.25μm 1-poly 5-metal CMOS
Supply Volatge	2.5V
Adder Delay	670ps
Power Dissipation	100mW @ 500MHz CLK Cycle
Transistor Count	5460
Active Adder Area	0.16mm² (1284μm x 130μm)
Chip Size	0.84mm² (1400μm x 600μm)

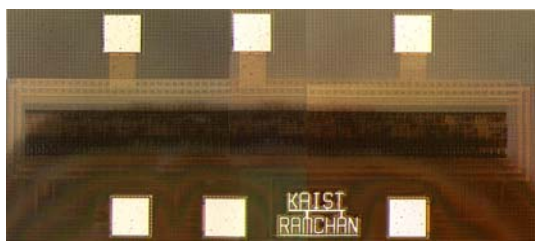
Adder Features

Layout and Die-Photo



Layout of Adder Test Chip

Die-Photo



Chip Size : 0.84mm^2 (1400μm x 600μm)

Conclusions

- A 64bit Dynamic Adder is designed and fabricated using 0.25μm CMOS technology.
- Dynamic-OR 'P' Scheme yields 30% Speed-up in PG-stage.
- Separated Carry Propagation Path yields 25% Performance Improvement by using Simple Dynamic Circuits.
- Adder shows 670ps Worst-case Delay and 100mW Power Consumption @ 500MHz Clock Cycle.