A 210mW Graphics LSI implementing Full 3D Pipeline with 264Mtexels/s Texturing for Mobile Multimedia Applications

Ramchan Woo, S. Choi, J.H. Sohn, S.J. Song, Y.D. Bae, C.W. Yoon, B.G. Nam, J.H. Woo, S.E. Kim, I.C. Park, S. Shin\textsuperscript{1)}, K.D. Yoo\textsuperscript{1)}, J. Chung\textsuperscript{1)}, and H.J. Yoo

Semiconductor System Laboratory
Korea Advanced Institute of Science and Technology
\textsuperscript{1)} Hynix Semiconductor Inc., Korea
Outline

- Introduction
- System Integration Overview
- Low Power IP Blocks
  - RISC, BEQ, 3DRE, DRAM, PPO
- Low Cost Process Technology
- Implementation Results
- Summary
Multimedia Processing on Hand

### System Requirements
- Long Battery Lifetime
- Small Footprint
- Low Cost

### Multimedia Applications
- Realtime Audio
- Realtime Video
- Realtime 3D Graphics

- 2D/3D Graphics LSI for Mobile Multimedia
  - Highest Level of Integration for Portable 3D
  - Low Power Techniques
  - Low Cost DRAM Process
Portable 3D Graphics

- Wireless Applications on Hands
  - 3D Avatar, 3D Games, Advertisements

- Functional Requirements
  - Texture Mapping + Special Rendering Effects
  - Gouraud Shading, Alpha Blending, Depth Comparison
## Standouts of 3D Rendering Engine

<table>
<thead>
<tr>
<th></th>
<th>ISSCC2000</th>
<th>ISSCC2001</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Generation</strong></td>
<td>1st</td>
<td>2nd</td>
<td></td>
</tr>
<tr>
<td><strong>Process Technology</strong></td>
<td>0.35(\mu)m EML</td>
<td>0.18(\mu)m EML</td>
<td>0.16(\mu)m DRAM</td>
</tr>
<tr>
<td><strong>Power Consumption of</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3D Rendering Engine</td>
<td>590mW</td>
<td>120mW</td>
<td>140mW (Texture)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>80mW (No Texture)</td>
</tr>
<tr>
<td><strong>Pixel Fill Rate</strong></td>
<td>40Mpixels/s</td>
<td>70Mpixels/s</td>
<td>66Mpixels/s</td>
</tr>
<tr>
<td><strong>Texturing Performance</strong></td>
<td>X</td>
<td>X</td>
<td>264Mtexels/s</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bilinear MIPMAP</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Perspective Correct</td>
</tr>
<tr>
<td><strong>Special Rendering</strong></td>
<td>X</td>
<td>X</td>
<td>Programmable</td>
</tr>
<tr>
<td><strong>Effects</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Size of Embedded</strong></td>
<td>0.5Mbits (FB / ZB)</td>
<td>6Mbits (FB / ZB)</td>
<td>29Mbits (FB / ZB / TM)</td>
</tr>
<tr>
<td><strong>DRAM</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Integration of Full 3D Pipeline

3D Pipeline
- Geometry Engine
  - T&L
- Vertex Buffer
  - Shading
- Rendering Engine
  - Texturing
- Rendering Memories
  - Frame/Depth
  - Textures

Operation
- Fast Calculation (>0.5M Vec/s)
- Programmability
- Efficient Data Xfer
- Parallel Calculation (>10M Pix/s)
- Huge Memory BW (>1GB/s)
- Large Capacity (>10Mb)
- Fast Cycle Time
- Many Access Ports
Architecture Overview

RISC
- 4kB I$
- 4kB D$
- ARM-9 Core

BEQ
- CTRL
- 1KB DP SRAM

3DRE
- SlimShader
  - TSE
    - PP #0
    - PP #1
    - TE #0
    - TE #1
  - AAL
- Memory Programmer
- Display Output
- 1.6GB/s @ 33MHz

External Interface

Clock Control Unit

PLL

PPO

DRAM
- 2Mb Depth Buffer
- 3Mb Frame Buffer
- 24Mb Texture Memory
Multimedia-Enhanced RISC

- **Enhancement with MAC**
  - 32x32 MAC in a single cycle
  - 3D Geometry Acceleration
    - 1.04Mvertices/s
    - 43% Improvement
  - Hand-Optimized S/W Library
  - MPEG-4 SP@L1 Decode

- **Memory Interface**
  - Direct path to BEQ
  - On-Chip SP-RAM Support
  - Non-Cacheable Addressing
Bandwidth Equalizer
: Low Power Technique (1)

- Partial Activation of DP-SRAM 20% Power Save
- Polygon Buffer / SP-RAM
3D Rendering Engine Architecture
: Low Power Technique (2)

TSE eliminates ~7000 RISC cycles

SlimShader

Address Alignment Logic (AAL)

Display Output

RISC

BEQ

3DRE

12 DRAMs reduce power consumption

MP

PP0

PP1

Texture Filter

Pixel Blending

Texture Addr.

Intpl. / Depth Comp.

Texture Filter

Pixel Blending

Texture Addr.

Intpl. / Depth Comp.

6Mb Texture Memory 0

6Mb TM1

6Mb TM2

6Mb TM3

512kb DB 0

DB1

DB2

DB3

768kb FB 0

FB1

FB2

FB3

Intpl. / Depth Comp.

Depth Comp.

Texture Addr.

6Mb
Depth First Clock Gating
: Low Power Technique (3)

□ DFCG prevents Unnecessary Transition
High Performance & Low Power Texturing

: Low Power Technique (4)

- **Address Calculation**
  - Perspective-Correct
  - Per-Pixel Dividers
  - Removes Artifacts

- **Texture Filtering**
  - Bilinear MIPMAP
  - Improves Pixel Quality

- **AAL**
  - Reduces the TM Requests
  - Simple Texture Cache

- **Embedded TMs**
  - Eliminates Off-chip loading
Address Alignment Logic
: Low Power Technique (5)

Number of Texture Requests
8 -> 2.5

☐ DFCG and AAL reduce 20% Power
Memory Programmer

: Low Power Technique (5) – Cont’d

- SIMD-parallel Datapath
- 16b Commands
- Commands Registers
3D-Optimized DRAM : FB / ZB
: Low Power Technique (6)

- Read-Modify-Write in a single Cycle < 20ns
- Partial Wordline Activation
Programmable Power Optimizer
: Low Power Technique (7)

- Fully software controllable
- Adjusting the frame rate during runtime
- Zero-latency frequency change
- PPO with PLL consumes less than 3mW
PPO Circuits and Measurement

: Low Power Technique (7) – Cont’d

Zero-Latency Frequency Scaling

GDFF eliminates glitch during frequency change

Measured Waveform
DRAM-based SoC Implementation

- Global Routing
- Resistive M0
- Std Cell Routing

- Low Cost
- Large On-Chip Memory with Little leakage current
- Logic, SRAM, Analog : Periphery Transistors
Die Photograph

- 0.16μm DRAM
  - 1-W 3-AL
- 11mm x 11mm
- 240pin I/O
- Power Supply
  - 2.0V : DRAM Core
  - 2.5V : Logic/Analog
  - 3.3V : I/O
- Power Consumption
  - Less than 210mW
- Transistors
  - 1M Logic
  - 29Mbits DRAM
  - 72kbits SRAM
System Power Consumption

Power (mW)

External Memory

No AAL, DFCG

3DCG with Texture

3DCG without Texture

MPEG4 Decoding

by Embedded DRAM

22% reduction with AAL, DFCG

210mW

145mW

85mW

3DRE and DRAM are Gated Off

FAST Mode

DB
FB
TM
3DRE
RISC
PPO
Rendering Performance Comparison

- **Pixel Rate**
  - MPxPS/mW = \( \frac{MPixels/Sec}{mW} \)
  - ISSCC 2000: 0.07
  - ISSCC 2001: 0.5
  - THIS WORK: 0.8
  - 1.4x increase

- **Texel Rate**
  - MTxPS/mW = \( \frac{MTexels/Sec}{mW} \)
  - ISSCC 2000: 0
  - ISSCC 2001: 0
  - THIS WORK: 1.88
  - No Texturing

- **Performance Index of Portable 3D**
  - JSSC Oct. 2002
  - Rendering Performance / Rendering Power
  - Analogous to MIPS/mW
System Evaluation Board
Summary

- Low Power 2D/3D Graphics LSI for Mobile Multimedia Applications
  
  (1) Highest Integration Level and Performance
  - Full 3D Pipeline: RISC + BEQ + 3DRE + DRAM + PPO
  - True-Color Pixels at 66Mpixels/s, 264Mtexels/s
  - Programmable Special Rendering Effects

  (2) Low Power Techniques
  - DFCG, AAL, PPO
  - Partial Activation: SRAM, DRAM

  (3) Low Cost Implementation
  - 0.16μm DRAM Process

- <210mW, 121mm²
  - Ready to be on your Hand