A Low Power 3D Rendering Engine with Two Texture Units and 29Mb Embedded DRAM for 3G Multimedia Terminals

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Outline

- Introduction
- System Architecture
  - Low-Power 3D Rendering Engine
  - Pipeline Structure
  - Texture Unit
- Embedded DRAM
- Implementation Results
- Conclusion

3G Multimedia Terminals

- **Mobile Multimedia Center**
  - Camera
  - 2D Graphics
  - MP3 Audio
  - MPEG-4 Video
  - Java Gaming



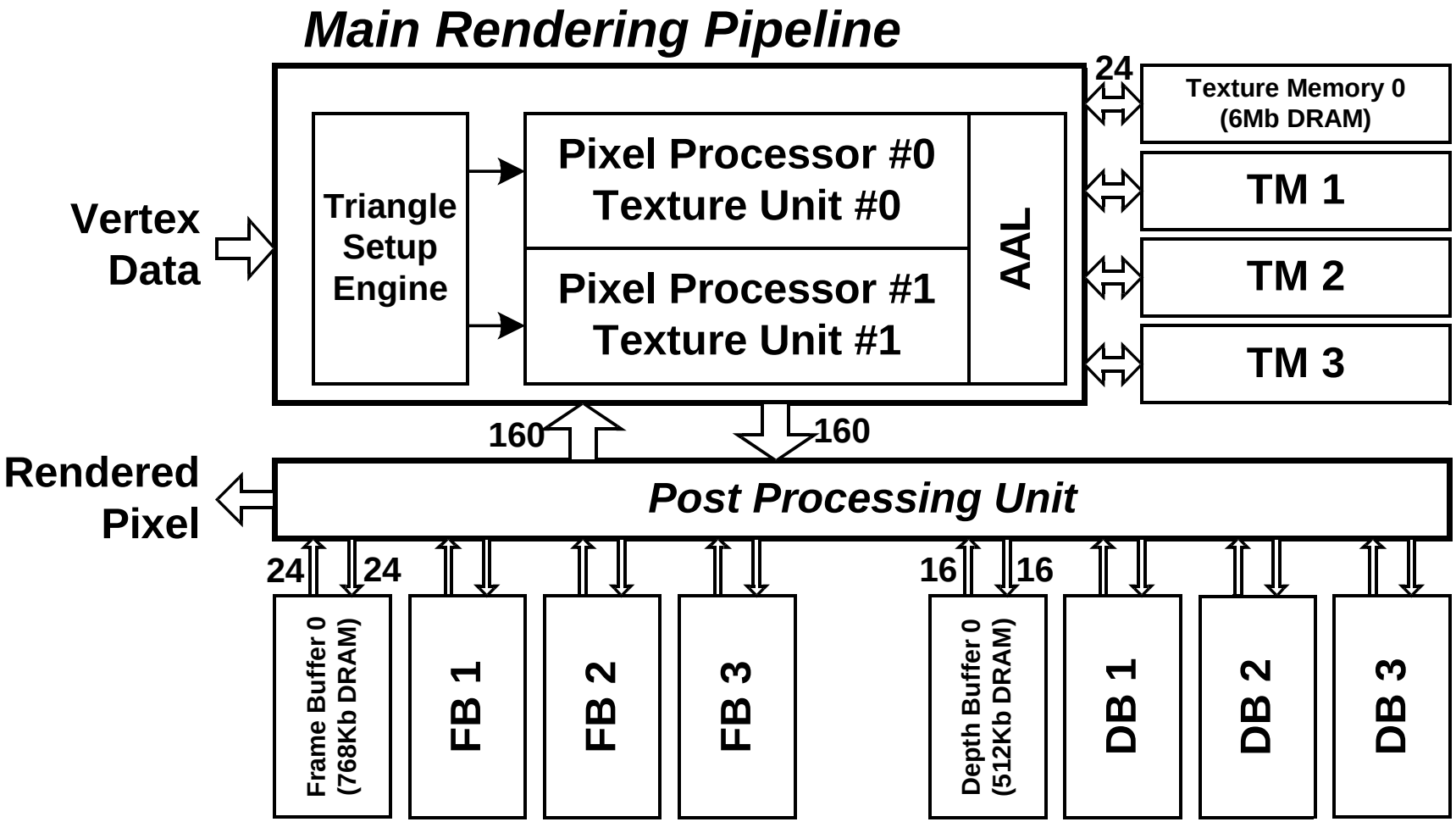
- **3DCG is the next step !**


Avatar

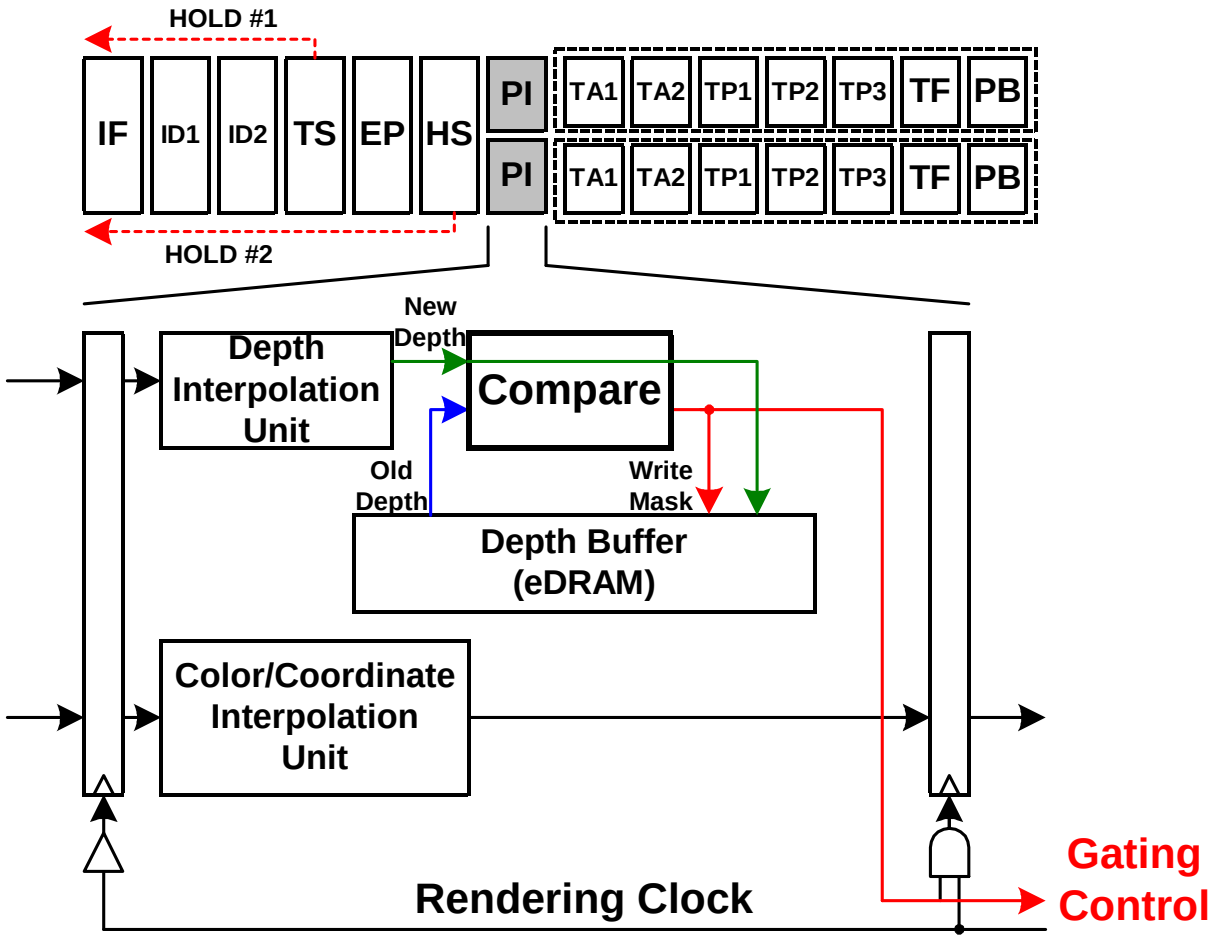

Game

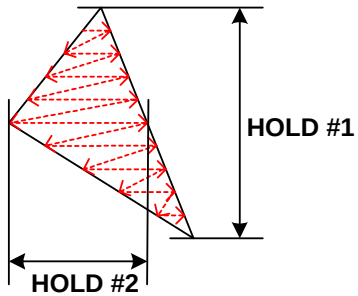

Advertisement

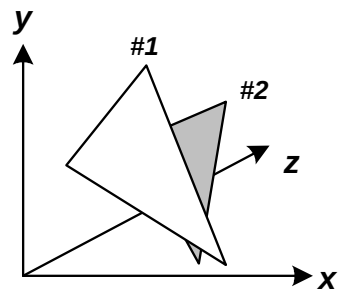
Rendering Engine Overview

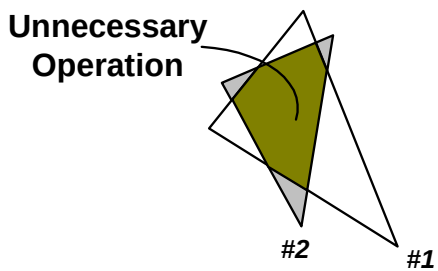


Pipeline Architecture with Clock Gating
: Low Power (1)

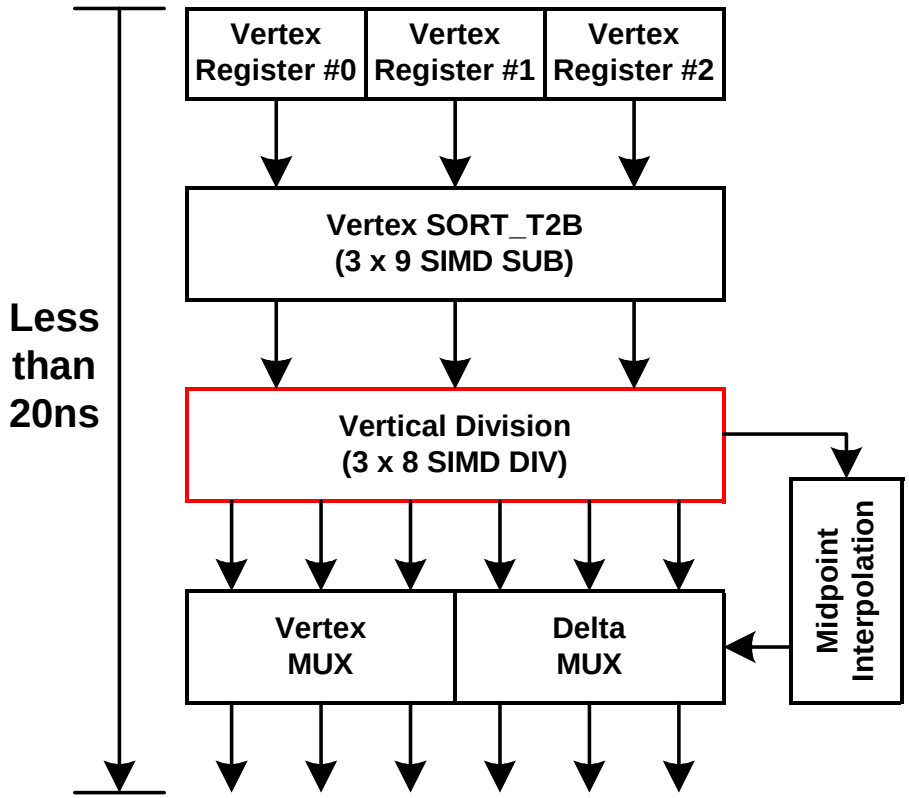








Triangle Setup Engine
: High Performance

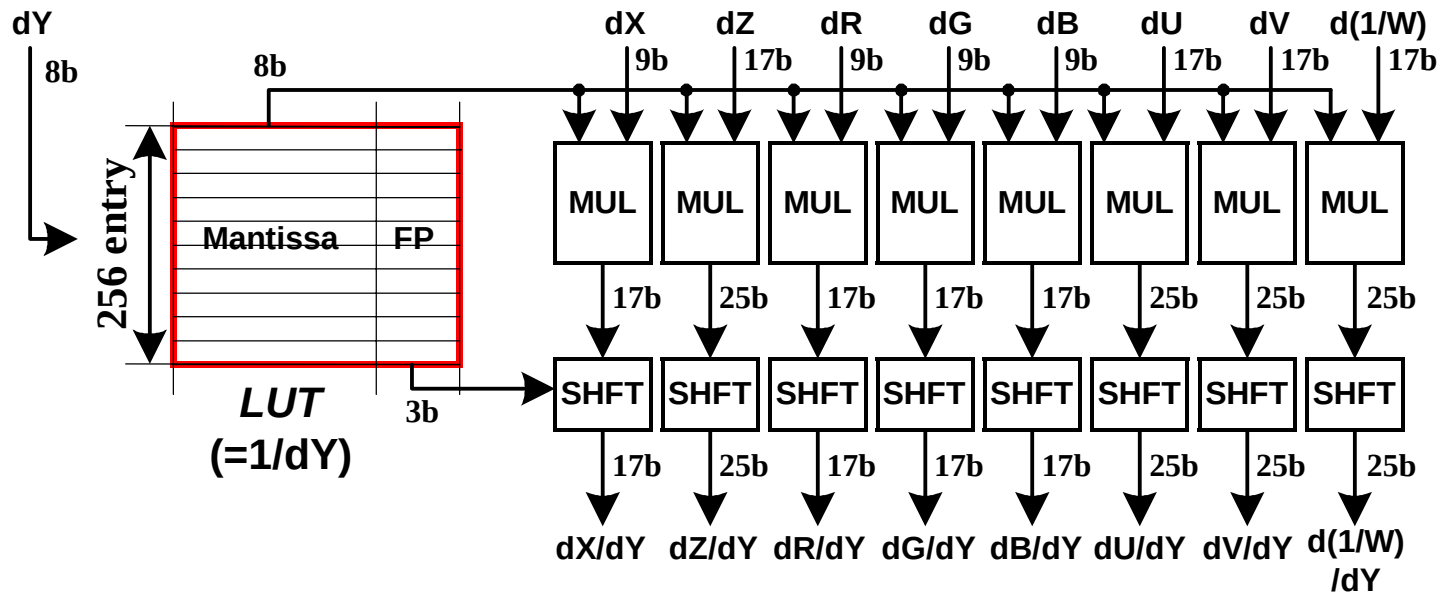


- **Operation**
  - Sorting Vertices
  - Setting-up Parameters

    $\Delta(X, Z, R, G, B, U, V, 1/W)/\Delta Y$
- **Hardware Resources**
  - 3 x 9-way SIMD SUBs
  - 3 x 8-way SIMD DIVs
  - MULs, MUXes
- **Performance**
  - 1 Rendering Cycle (50MHz)
  - ~7,000 RISC Cycles by Software

Precision-Controlled LUT Divider

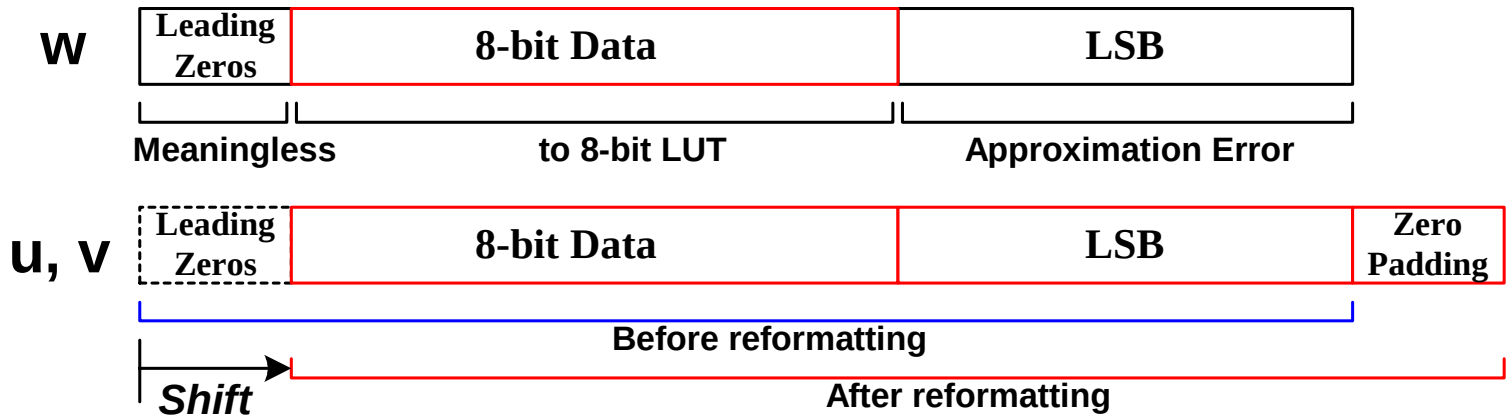
: Low Power (2) and Small Area



- **Optimized Floating-Point Division**
  - **Preserving Required Precision**
  - **Saving 95% Power and 85% Area Compared with IEEE754**

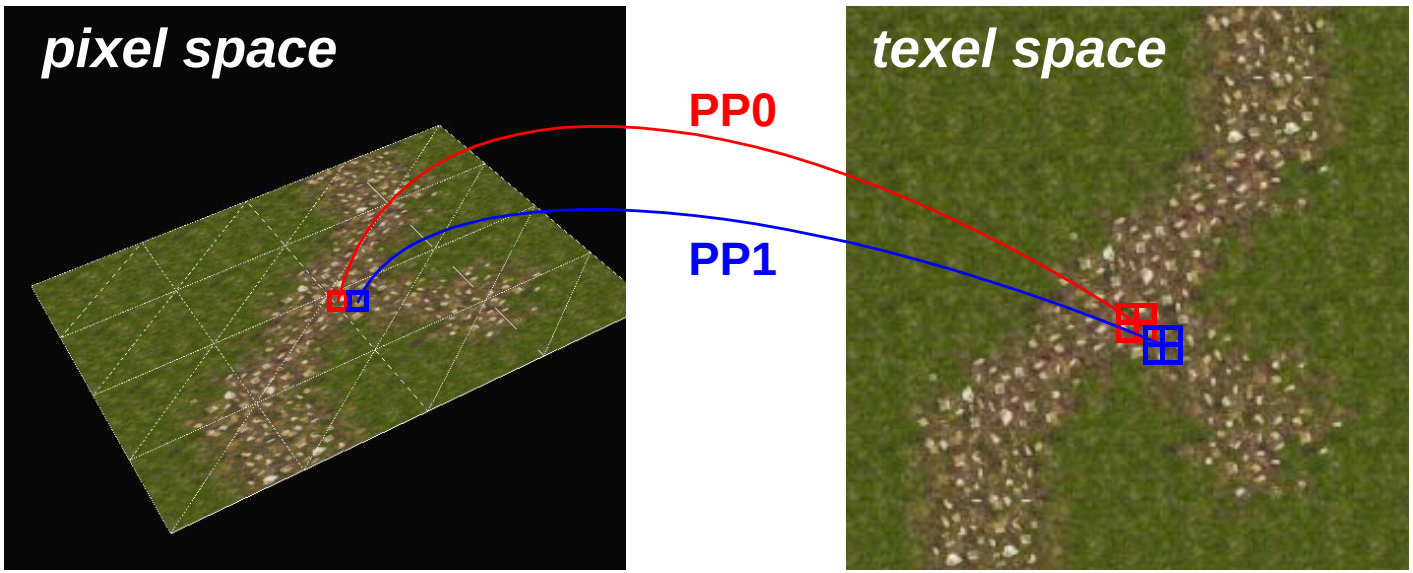
Texture Unit : Per-Pixel Division

: Low Power (3) and Small Area



- **Operation**
  - U = u/w, V = v/w, (where, u, v, w = 16bits each)
  - 16bits / 16bits Division is a Large Overhead
  - Use 16bits / 8bits Instead (w $\geq$ u, v)
- **Precision Reduction**
  - $0.78\%_{MAX}$ Calculation Error
  - 95% Area Reduction

Texture Unit : AAL Operation
: Low Power (4)



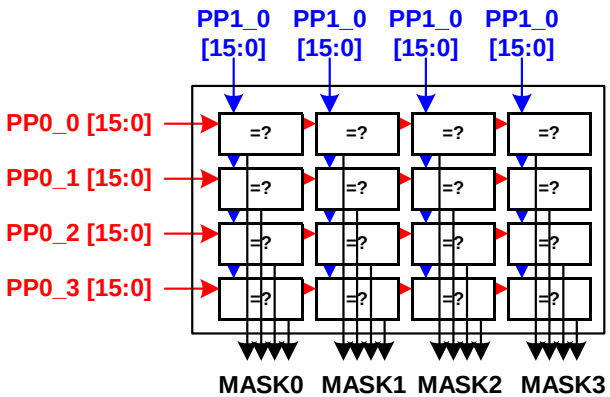
Screen Image

Texture Image

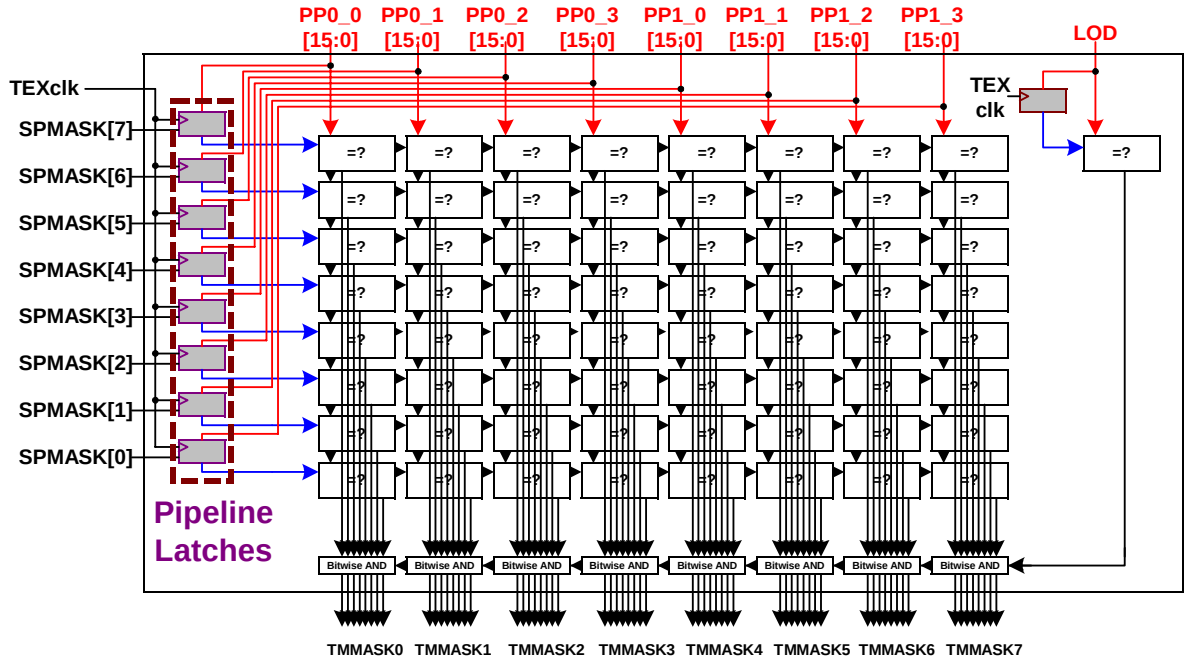
- **Bilinear MIPMAP Filtering**
  - Requires 4 texels / 1 pixel → 8 texels / cycle
- **AAL Gathers and Reduces Texel Requests**
  - 8 → 2.5

Address Alignment Logic

: Low Power (5)



Spatial Aligner



Temporal Aligner

- **Exploiting Locality**
  - Two PPs Render Adjacent Pixels
  - TM Requests : 8 → 5 → 2.5

Embedded DRAM

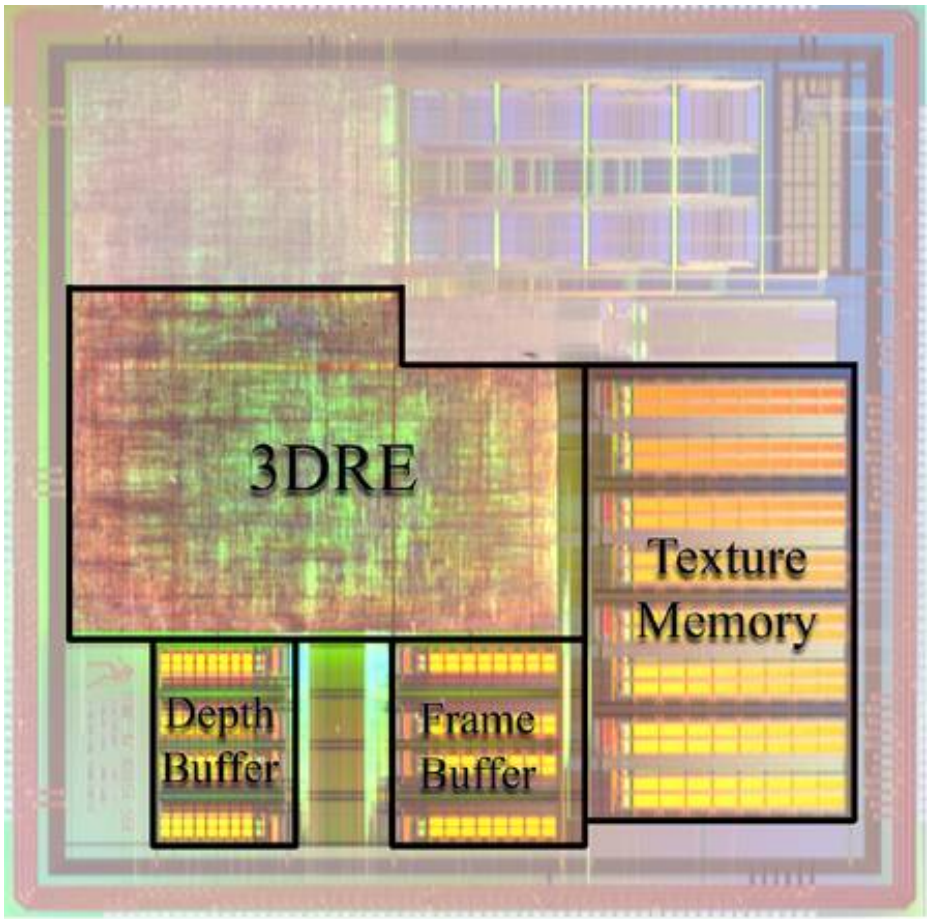
: Low-Power (6) and High Performance

- **12 3D-Optmized Memories**
  - **Selective Activation for Low-Power Consumption**

	Frame Buffer	Depth Buffer	Texture Memory
T_{RC}	20ns (50MHz)		
Macro Size	768Kbit	512Kbit	6Mbit
I/O Interface	24bit read 24bit write	16bit read 16bit write	24bit I/O
Commands	Read-Modify-Write Read, Write Auto Refresh		Read, Write Auto Refresh
Latency	0	0	1

- **Huge Memory Bandwidth**
  - **416bit-Wide On-Die Memory Bus**
  - **2.4GByte/s @ 50MHz, Random Row-Change**

Integration into a Mobile Graphics LSI



- **0.16um DRAM**
  - **1-W 3-AL**
- **3DRE + eDRAM**
  - **46mm²**
  - **5M ~ 50MHz Scalable**
  - **10M ~ 100Mpixels/s**
  - **40M ~ 400Mtexels/s**
- **Mobile Graphics LSI**
  - **121mm²**
  - **Chip : 33MHz**
  - **210mW (Full Die)**
  - **140mW (3DRE+eDRAM)**

REMY-I : First Prototype System

REMY-II : PDA Prototype

Summary

- **Low-Power 3D Rendering Engine for 3G Multimedia Terminals**
  - **(1) High Performance**
    - **x50 Faster than QVGA Phone Requirements**
  - **(2) Low Power Technique**
    - **<140mW**
  - **(3) Low Cost Implementation**
    - **0.16um 256Mb DRAM Process Technology**
- **<140mW, 46mm^2**
  - **Integrated into the Mobile Graphics LSI**
  - **Successfully Demonstrated on System Evaluation Boards**