A Sub 1V 96 μW Fully Operational Digital Hearing Aid Chip With Internal Status Controller

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***Abstract*—A Low power fully operational digital hearing aid chip is proposed and implemented. The Σ-Δ ADC adopts the status controller to realize adaptive SNR technique without any external control. To achieve both low power consumption and high programmability, dedicated low power DSP with 6 control parameters is designed. The heterogeneous Σ-Δ DAC reduces more power dissipation without performance degradation. The digital hearing aid system is fabricated in 0.18 μm CMOS technology, consumes less than 96 μW and has a die size of 2.8 mm x 1.1 mm.**

I. INTRODUCTION

In these days, the enormous attention of the bioelectronics system market requires new design methodologies to achieve both low power and high performance [1-3]. Especially more and more people suffer from their hearing problems, and the number of people with some degree of hearing loss continuously increased every year [4]. According to this requirement, the development of the digital hearing aid system with low power consumption, more flexibility, small form factor and low cost is getting to achieve much attention. The previous studies had accomplished low power hearing aid system by adopting special CMOS process such as low-threshold voltage [6] or by using a log-domain analog hearing aid with sub-threshold technique [7]. However, those approaches have some weaknesses to reduce power dissipation because of boosted supply voltage for analog blocks or signal processing with analog filters which dissipates high power. In this paper we present a fully operational one chip implementation of a digital hearing aid with less than 100 μW power consumption. This chip is based on our previous low-power analog front-end circuit for digital hearing aid [1] and a status controller, a low-power dedicated DSP and heterogeneous Σ-Δ DAC are integrated newly for the full function of digital hearing aid.

II. SYSTEM OVERVIEW

Fig. 1 shows the proposed one chip digital hearing aid architecture. In order to achieve high programmability and accurate preamplification with low-power consumption, the combined gain control (CGC) preamplifier is designed [1]. The Σ-Δ ADC chooses the adaptive-SNR (ASNR) technique to acquire low power dissipation and wide dynamic range according to the external environment [1]. The proposed hardwired DSP achieves low power consumption and high flexibility by using 6 control parameters. The Σ-Δ DAC with heterogeneous frequency reduces power consumption further by decreasing the input signal frequency compared with the clock frequency of the Σ-Δ modulator without performance degradation.

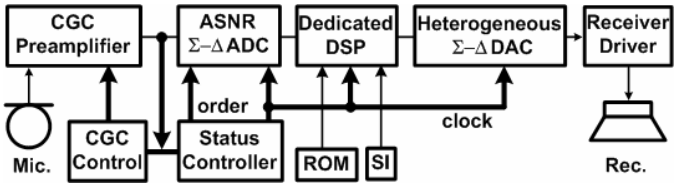

Figure 1. Overall architecture of the digital hearing aid

III. BUILDING BLOCKS

A. *Adaptive SNR Σ-Δ ADC with status controller*

The architecture of the proposed analog front end is shown in Fig.2. It is composed of the CGC preamplifier and the ASNR Σ-Δ ADC. To introduce the ASNR technique input signal range is divided into four parts. Each part has own combination of the clock frequency and order of the Σ-Δ modulator to achieve different SNR values.

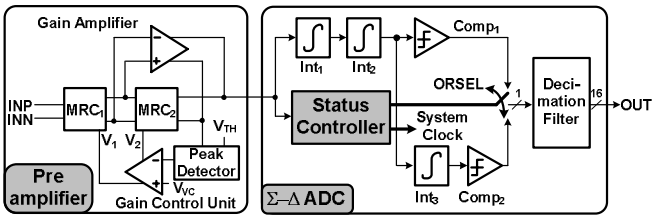

Figure 2. Proposed analog front-end

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In the previous work, control register and a DSP with external control signal is applied to determine the clock frequency and order of the Σ-Δ modulator [1]. In this work, status controller is implemented to achieve fully operational ASNR technique of the Σ-Δ ADC without any external control signal.

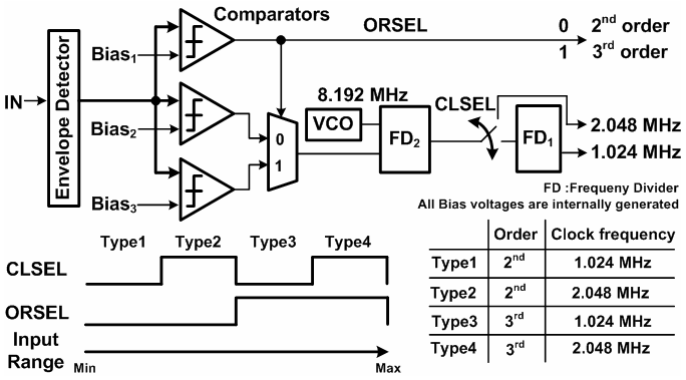


Figure 3. Status controller architecture and signaling

Fig. 3 shows the architecture of the status controller. The status controller determines the control signals, ORSEL and CLSEL, to decide the status of the Σ-Δ modulator. By comparing the output signal of the preamplifier with the reference voltages generated by internal regulator, the values of the ORSEL and CLSEL are decided. The VCO generators the internal system clock according to the CLSEL.

The ORSEL choose the order of the Σ-Δ modulator between two and three while the CLSEL generates the reference clock between 1.024 MHz and 2.048 MHz. By alternating this two control values, four different status of the Σ-Δ ADC for adaptive SNR technique is achieved using only internal signals.

B. Low power dedicated DSP

Fig 4 shows the block diagram of the proposed digital signal process (DSP) unit. It is composed of a DSP core, serial interface, coefficient ROM, and coefficient selector.

The output signal of the decimation filter is spited into two frequency bands, high-band and low-band, to give the different gain according to the input frequency. After the each sub-band is processed, it is combined to achieve the signal information of the overall frequency band.

For achieving the parameter coefficients of the DSP, this system allows to use whether serial interface or coefficient ROM. The coefficient selector chooses the parameter coefficients between the serial interface and coefficient ROM outputs. When the serial interface is enabled, DATA is propagated into the serial interface. After that, LE signal is activated and each parameter is transmitted to the digital signal processor. On the other hand, when the serial interface is disabled, the coefficient ROM outputs the stored parameter coefficient by decoding the parameter, CO.

Fig. 5 presents the advanced two-band DSP algorithm compared with the previous one [8]. The proposed DSP adopts the 6 parameters to enhance the system programmability with low power dissipation. By controlling the parameter P, the frequency response characteristics of the high-band signal and low-band signal are determined. Parameter G_0 enhances the low-band signal gain after the band split. In addition, high-band signal adopts the threshold knee parameter K to suppress the excessively high gain. When the amplitude of the high-band signal is smaller than the value of K, gain parameter G_1 is applied to achieve necessary signal gain. On the other hand, G_2 is selected to compress the high-band response. The volume control parameter VC controls the amplitude of the input signal to customize digital hearing aid for each individual user.

By implementing the band split filter as an FIR filter, the finite word-length. To reduce the power dissipation, the multiplying function is implemented using only hardwired shifting and adding by selecting the all filter coefficients as 0.5. The transfer function $H_{DSP}(z)$ of the proposed DSP is given by

$$H_{DSP}(z) = [0.5(1+G_0)(1+z^{-4}) - 0.5^P(G_2|_{HP\geq K} + G_1|_{HP\leq K})(1-z^{-4})^P]$$

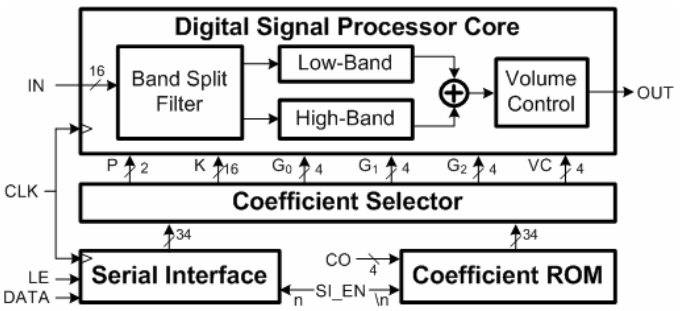


Figure 4. Dedicated DSP architecture

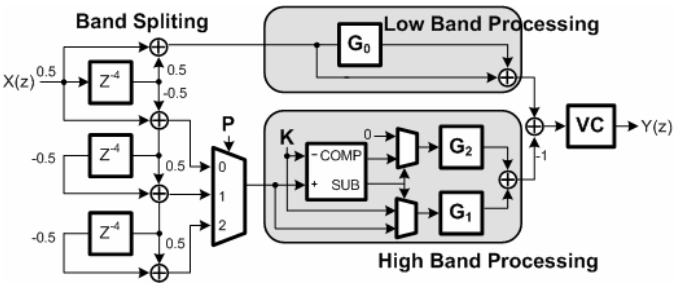


Figure 5. Advanced two-band DSP algorithm

C. Heterogeneous Σ-Δ DAC

The proposed heterogeneous Σ-Δ DAC consists of three interpolation filter and a 3rd order Σ-Δ modulator is shown in Fig.6. The 16-bit, 32 KHz DSP output signal is used as the input signal of the proposed Σ-Δ DAC. In order to increase the signal frequency of the interpolation filter up to 512 KHz without

hardware design difficulties, the interpolation filter consist of 3 stages which upsampling ratio is two, two and four, respectively. The upsampling ratio of 3rd stage is selected as four because the frequency selectivity is lower than those of 1st and 2nd stage.

In the conventional Σ-Δ modulator, the frequencies of the input signal should be equal to that of sampling clock. It means the interpolation filter should upsample input signal up to sampling clock frequency of the Σ-Δ modulator. However the ratio of the input signal frequency and the sampling clock frequency is very high, for example 32 KHz and 2.048 MHz respectively, upsampling of the input signal dissipates high power.

In the heterogeneous Σ-Δ DAC, frequency of the input signal is different from that of the sampling clock of the Σ-Δ modulator, for example 512 KHz and 2.048 MHz, respectively. Fig.7 shows the principle of the proposed heterogeneous Σ-Δ DAC. If the 512 KHz signal is input to the Σ-Δ modulator operating at 2.048 MHz sampling clock frequency, it is equivalent to transfer the input signal through the 4th order low-pass filter, $H(z)=1+z^{-1}+z^{-2}+z^{-3}$. The filtered input suppresses the signal component outside of the pass-band region. However the input audio signal is less than 8 KHz, most of the signal energy is inside of the fundamental pass-band and only tolerable amplitude degradation is occurred. The error due to the filtering is about 0.16 %. Compared with the scheme using the interpolation filter with 2.048 MHz output signal frequency which can give accurate results, the heterogeneous Σ-Δ DAC dissipates less power and occupies smaller area in consideration of its reasonable accuracy. The heterogeneous Σ-Δ DAC reduces power dissipation and area penalty by 26% and 27%, respectively.

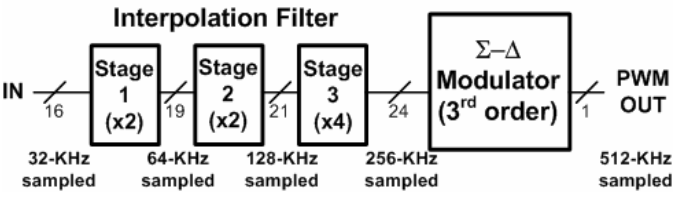


Figure 6. Heterogeneous DAC architecture

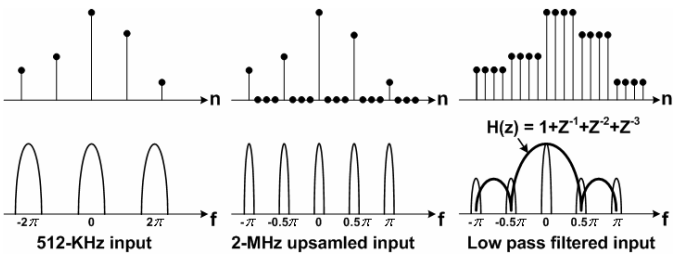


Figure 7. Principles of the heterogeneous DAC

IV. Implementation Results

The digital hearing aid chip has been fabricated in a 0.18 μm standard CMOS technology. Fig.8 shows a microphotograph of the proposed digital hearing aid chip. The active area is 2.8 mm x 1.1 mm. It dissipates less than 100 μW from a 0.9 V supply. Fig.9 plots the measured frequency response of the Σ-Δ modulator. The measured peak SNR is 73 dB at type 1 with 1 KHz sinusoidal input signal. Fig. 10 shows the measurement results of the status controller. According to the input amplitude of the proposed Σ-Δ modulator, the ORSEL change the order between two and three while the CLSEL alternates the clock frequency between 1.024 MHz and 2.048 MHz respectively.

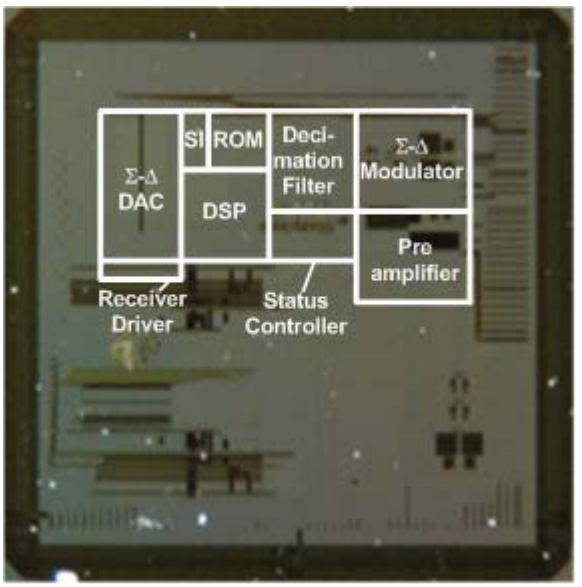


Figure 8. Chip microphotograph

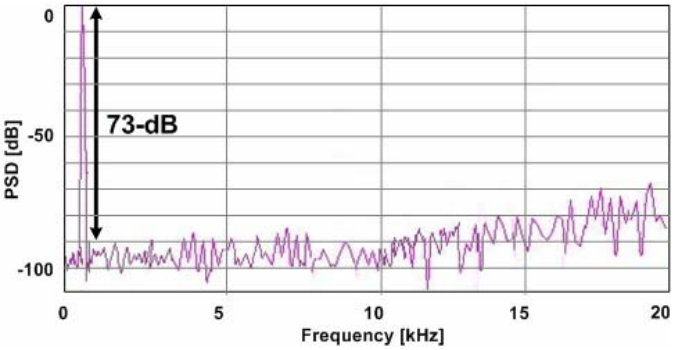


Figure 9. Output spectrum of the proposed Σ-Δ modulator

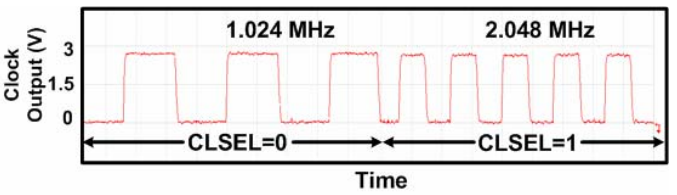


Figure 10. Output clock frequency due to the status controller

Fig.11 shows the frequency compensated gain characteristics of the proposed DSP. By adopting parameter values to control the gain, ski-slope is well compensated. Fig. 12 shows the PWM output signal driving the receiver driver (RD) from the digital pad and the RD output voltage. Fig. 13 represents the performance comparison between other hearing aid circuits and the proposed system. The average power consumption from type 1 to type 4 is reported. It reveals that the proposed digital hearing aid chip consumes the lowest power.

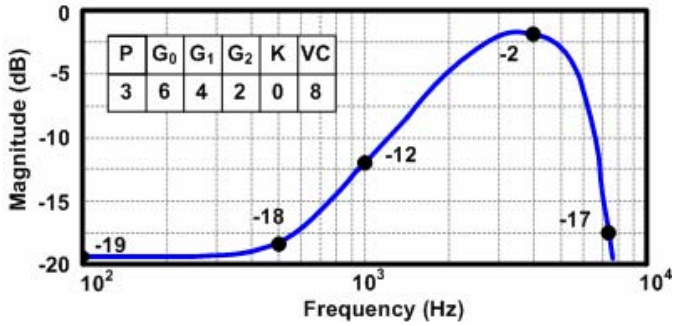


Figure 11. Gain characteristics of the proposed DSP

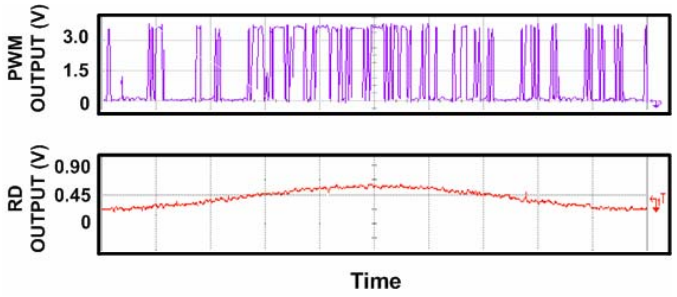
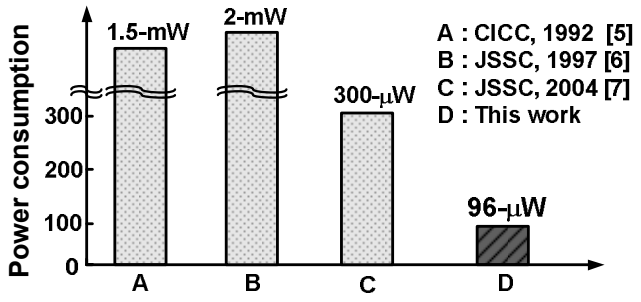


Figure 12. PWM output and RD output of the heterogeneous Σ-Δ DAC



Supply Voltage	1.3 V	1.3 V	1.1V	0.9 V
Peak SNR	NA	77 dBA	70 dB	79 dB
Process (CMOS)	3-μm BiCMOS	0.8-μm	1.2-μm	0.18-μm

Figure 13. Comparision of the power consumption with previous works

The performance of the proposed low power digital hearing aid chip is summarized in TABLE I. The clock frequency of the proposed DSP is 32 KHz and gate count is 10k. The average power dissipation of the overall system is less than 100 μW.

TABLE I. PERFORMANCE SUMMARY

System	Power supply		0.9 V
	Power dissipation		96 μW
	Input referred noise		4.1 μVrms
	-3 dB bandwidth		8 KHz
	Core area		2.8 mm x 1.1 mm
	Technology		0.18 μm CMOS
Build blocks	Preamplifier	Max gain	34 dB
	Σ-Δ ADC	SNR	87(Max) ~ 73(Min)
	DSP	Gate count	10 K
		Clock frequency	32 KHz
	Σ-Δ DAC	Gate count	16 K
		Clock frequency	2 MHz

V. CONCLUSIONS

A low power high flexibility digital hearing aid chip is implemented using low power techniques. To implement the fully operational adaptive SNR technique of the Σ-Δ ADC without any external control, the status controller is newly designed. By adopting the dedicated low power DSP with 6 control parameters, both the power reduction and programmability enhancement is achieved. Moreover, the heterogeneous Σ-Δ DAC reduces extra power dissipation further. The digital hearing aid chip is fabricated in a 0.18 μm CMOS process. It consumes less than 96 μW with a 0.9 V single supply.

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