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# A TCAM-based Periodic Event Generator for Multi-Node Management in the Body Sensor Network

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*Abstract*— **Low-power periodic event generation is essential for a node controller in the network system with centralized control and the timer interrupt generation for various devices in a CPU. The proposed TCAM-based periodic event generator manages the issuing events with the programmed value and the number of the events is equal to the number of the word line of the TCAM block. The NAND-type TCAM cell operates with as low as 0.6V supply voltage and the low-energy match line precharge reduces the search line transition which causes most of the search energy dissipation. The implemented event generator consumes 184-nJ energy to schedule events of 255 nodes for 24-hours, which is less than 10% of energy consumption of conventional hardware timer blocks.**

## I. INTRODUCTION

A system with lots of slave nodes has to check the status of each node and send the data-request command as well as operation command to the nodes. In case of body sensor network (BSN) system [1] for mobile medical service applications [2], data of each node should be periodically gathered in accordance with the characteristics of the sensors. For example, a body temperature should be gathered every 2-minutes while a blood pressure should be checked three times a day. And the number of the sensor nodes is increased for accurate monitoring. Conventional BSN systems [3, 4] were implemented with wireless sensor network (WSN) with Ad-hoc network topology. In the network, however, every node requires extra processing workload to process the network routing and forwarding protocol, which brings big form-factor to support the requirements. The centralized network with star-topology, meanwhile, can relieve such redundant operations because a network controller requests data with pre-defined period of each node. In this case, the controller has to manage the period information of all the sensor nodes. However, conventional general-purpose processors [5] cannot meet the requirement because they have just limited number of timers which is essential for counting the period.

This paper presents a new application of a content addressable memory (CAM) [6, 7], a periodic events generator using TCAM-based associative memory block. With the proposed generator structure, the number of the period information which is as many as the number of the match lines minus one can be managed and corresponding issue signals are generated with ultra low-energy consumption. The test chip with 256 word lines or 16-bit TCAM block manages 255 individual periods and consumes 184-nJ energy for one day operation.

## II. PERIODIC EVENT GENERATION

Figure 1 shows conventional two approaches to generate n-periodic request signals. Figure 1 (a) uses n hardware timers, and each of which compares the pre-defined period information (P) and the real-time counter value (C). If P and C are equal, it generates the request signal so that a CPU or a controller can take actions. It is used to generate hardware timer interrupt in the general-purpose CPUs. Conventional CPU provides just 3~4 timers because the block consumes considerable power and silicon area. The approach with figure 1 (b) stores all the period values to the memory block and shares a hardware timer. Within every counting time unit, every 1-second for example, the block loads a period information (Pi) and compare it with the timer value (C) whether Pi should be issued or not. If C of present time is multiple of Pi, it generates the interrupt signal for node i and it scans next Pi. Although such operation can reduce the number of hardware timer, it requires additional hardware blocks and operations for memory access as well as match operation. Moreover, its faster operation clock increases its internal signal transitions which results in energy dissipation.

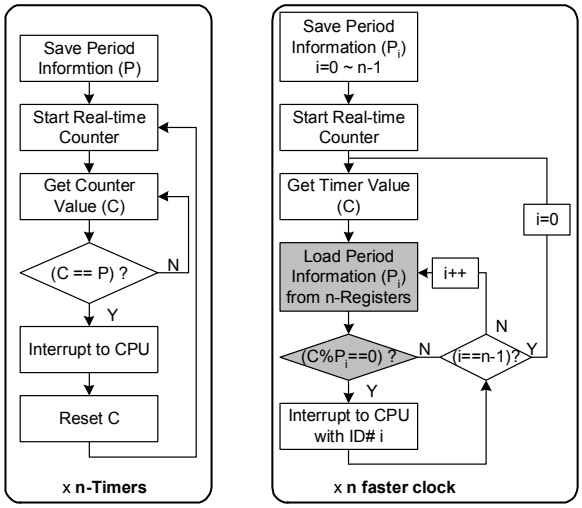


Figure 1. Operation Flow of Conventional Event Schedule

## III. CAM-BASED EVENT GENERATOR

The characteristics of CAM's simultaneous search operation can dramatically reduce the signal transition count and corresponding energy dissipation. Although its capacitive loading is heavy for high speed operation, the proposed cell relieves the loading by the cell structure optimized for the search operation. In the proposed CAM-based generator, energy-consuming search operation occurs once a counting time unit, 1-second in this case, and the events are generated with low clock frequency, 16-kHz in this case. Figure 2 shows the operations and corresponding clock frequency values of the proposed scheduler.

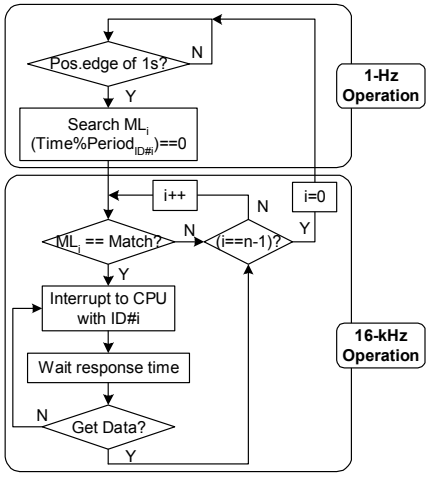


Figure 2. Operation Flow of CAM-based Event Scheduler

In this paper, a NAND-type TCAM which consumes lower power [7] than NOR-type in search operation is used as an associative memory for the proposed event generator. And various schemes for low-energy consumption and low-voltage operation are proposed to reduce the energy consumption of the search operation.

### A. CAM-based Event Generator

The proposed periodic event generator (PEG) consists of three components, the timer block, (15+1)-bit TCAM block and the ID generator, as shown in figure 3. The ID generator issues and generates the data-request signals by using the match line results ($ML_i$). $ML_i$s are generated with the comparison results between the value of the timer block and the TCAM block which are performed every 1-second.

In the CAM operation, most of energy is consumed for search operation. In this application, however, search operation occurs just once a second and it finds out the ID of the nodes to be issued by enabling corresponding match lines ($ML_i$). The search results are issued in order, from $ML_1$ to $ML_n$, by the ID generator with 16-kHz clock frequency. If a ML is enabled, the generation block issues the request signal by using the row number as the node number. And if the ML is disabled, it skips the packet generation and checks next ML.

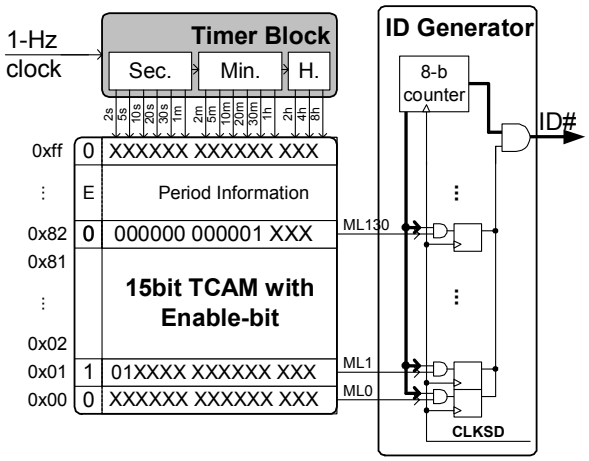


Figure 3. TCAM-based Periodic Event Generator

### B. Schemes for Low-Energy Consumption

Figure 4 shows a word structure used in the CAM block. It consists of a SRAM-based enable bit (E) and 15 TCAM-based period information bits (C0~C14). And the precharge signal is stitched every four cells to prevent the voltage degradation by the pass transistors. The enable bit E suppresses unnecessary evaluation of the match line which stores garbage data or out-of-date data. And the NAND-type TCAM cell is modified for low voltage search operation by adding two pMOS transistors. Although it has two more transistors compared with previous NAND-type TCAM cell [7], the transmission gate passes the match signal without Vth-drop, which enables 0.6V supply voltage search operation.

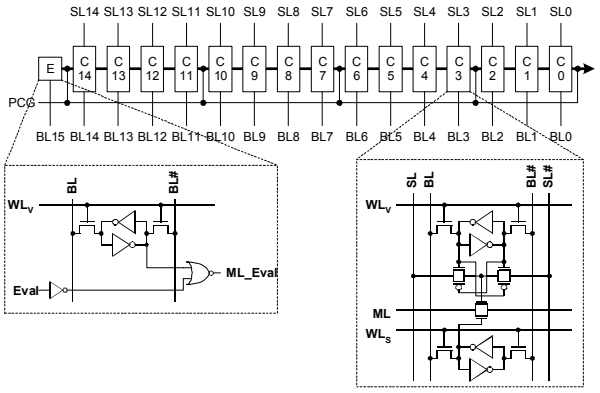


Figure 4. CAM Word Structure

A newly proposed match line precharge scheme (MLPCG) reduces the search line (SL) transition which consumes most of the energy in the CAM search operation. With the conventional search operation shown in figure 5 (a) and (b), the evaluation phase follows the MLPCG phase every cycle, and all the SLs and SL#s should be set to high for MLPCG. In the proposed scheme shown in figure 5 (a) and (c), however, the match lines are precharged at the end of evaluation phase without the transition

of SL pairs. Figure 6 shows the transition pattern of each SLs provided by the timer block. And the proposed MLPCG scheme reduces 74.5% SL transition compared with conventional MLPCG operation when the search value increases linearly like the pattern in figure 6.

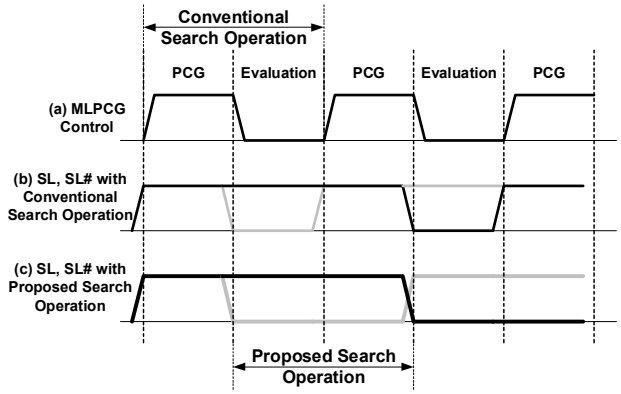


Figure 5. Timing of MLPCG and SL transitions for Search Operation

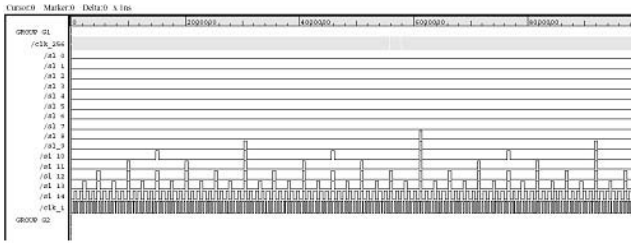

Figure 6. SL Transition Pattern provided by the Timer Block

Bit ordering of the search data affects the search energy consumption of the NAND-type CAM, while it does not in general memory access. Figure 7 shows the power distribution in accordance with the position of the mismatched bit in the NAND-type CAM word. It shows that the SL transition power is constant regardless of the mismatched bit position, the MLPCG power decreases as the mismatched bit position is close to MSB, the starting point of the match evaluation.

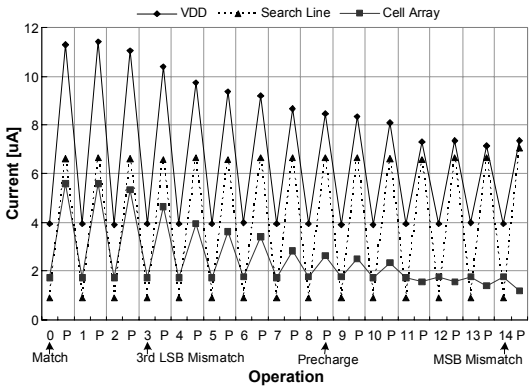


Figure 7. Power Consumption with Mismatch Bit Position

The timer block in PEG generates the search data with real-time and the value increases linearly as shown in figure 6. The NAND-type TCAM compares each bit sequentially, from MSB to LSB. If MSB mismatches, the CAM consumes less energy than the mismatch with LSB because the loading capacitance of the match line (ML) decreases. We can reduce the ML energy consumption by allocating the frequently changing bit to MSB of the CAM. Figure 8 shows the search power consumption of the CAM blocks with and without the bit order consideration. In the figure 8, the block with bit-order consideration consumes 61% power of the block without it.

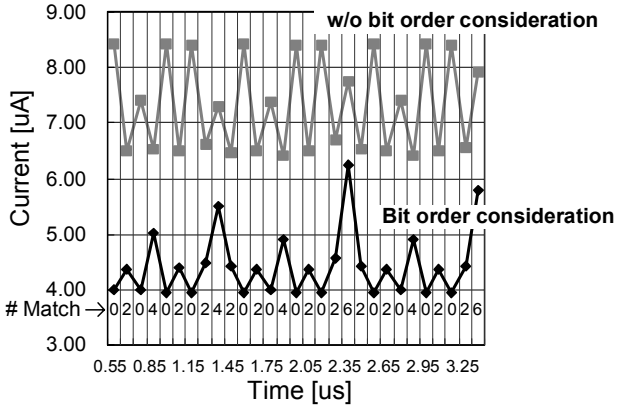


Figure 8. Power Consumption with the Bit Order Consideration

Figure 9 compares the energy consumption for managing 255 periods for 1-day of time second-by-second. The TCAM based PEG structure dramatically reduces the energy consumption and the proposed schemes reduces the energy to 30% of conventional TCAM blocks.

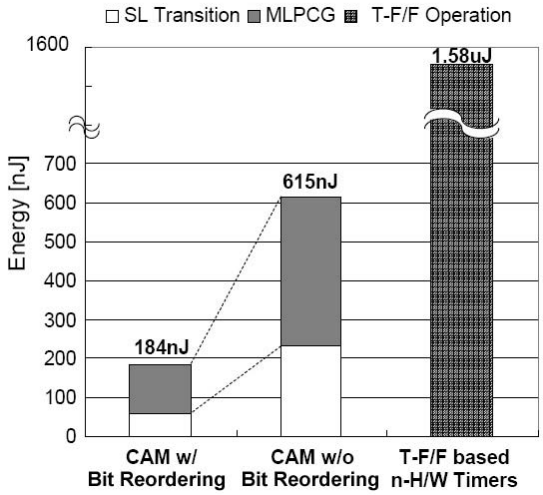


Figure 9. Energy Consumption for Managing 255 Periods

## IV. IMPLEMENTATION RESULTS

The proposed structure is implemented as a part of an ultra low-power BSN control processor [1] as shown in figure 10. The PEG with 256×16-bit NAND-type TCAM block occupies 1900μm×600μm chip area and the request signals generated by PEG are transferred to the communication transceiver block. The test chip is implemented with 0.18-μm CMOS logic process and it works with 0.6V core voltage.

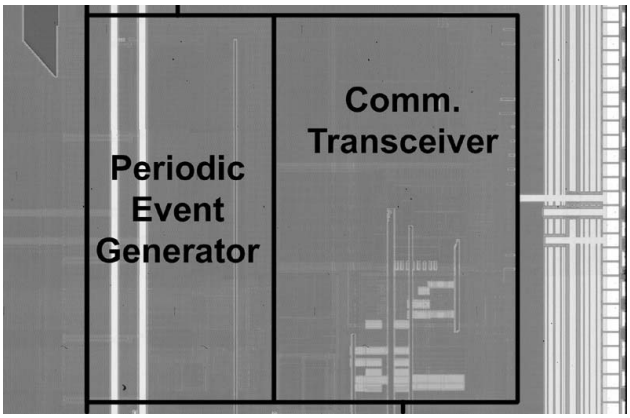


Figure 10. Implemented PEG with Communication Transceiver

Figure 11 shows the measured waveforms of the match result for the period comparison operation with 0.6V supply voltage. The waveform shows that the fabricated PEG can work up to 16-MHz operation in 0.6V VDD, which means that the number of managing node can be increased without changing the supply voltage and the SD architecture. And the block can expect lower energy consumption by operating it in the subthreshold operation region [8].

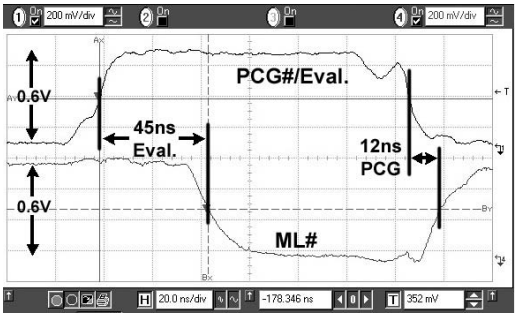


Figure 11. Measured Waveform of the TCAM Search Operation

Figure 12 compares the energy consumption of the conventional hardware timer and the proposed PEG with three values of TCAM match ratio. If the CAM searches 10 match lines out of 255 words every search cycle, the ratio becomes 4%. It shows that the proposed PEG consumes 10x less energy for management of 200 nodes.

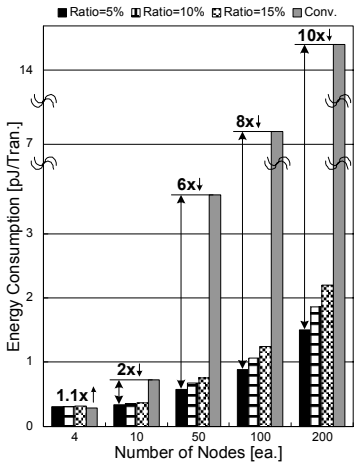


Figure 12. Energy Comparison between the Proposed PEG and Conventional H/W Timers

## V. CONCLUSIONS

The paper presents the structure of the periodic events generator for multiple slave node management. The proposed NAND-type TCAM-based PEG exploits the characteristics of parallel comparison for low energy timer count so that it can manage hundreds of periodic events with lowest energy consumption. The proposed CAM cell structure operates with 0.6V supply voltage with 45ns evaluation time and the energy-aware match line precharge schemes reduces the energy consumption to 30% compared with conventional MLPCG operation. The PEG block with 256×16-bit NAND-type TCAM cells is implemented with 0.18-μm CMOS logic process and consumes less than 10% of energy compared with conventional T-F/F based counter blocks.

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