A 200Mbps 0.02nJ/b dual-mode inductive coupling transceiver for *cm*-range interconnection

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***Abstract*— A 200Mbps 0.02nJ/b dual-mode inductive coupling transceiver is proposed for cm-range inductive coupling interconnection. The parallel capacitor combined with the TX inductor enhances the transmitted signal slew rate so that it increases the transmission distance by twofold. The proposed inter-symbol interference (ISI) reduction scheme of the transmitter improves data rate up to 200Mbps. And the proposed pulse generation scheme allows the transceiver to consume only 0.02nJ/b energy. The transceiver consumes 0.012 mm^2 in a TSMC 0.25um CMOS process.**

I. INTRODUCTION

Recently, short range (< 5cm) wireless communications with high data rate (> 100Mbps) are widely used for battery powered devices such as Wireless Personal Area Networks (WPANs) or implantable systems [1], [2]. Since these applications are powered by battery, low energy is one of the most important design issues. The long distance wireless communication schemes such as Zigbee, Bluetooth, and RFID are not appropriate for WPANs, because their maximum data rate is only few hundreds of kbps. Moreover, since the previous *cm*-range inductive coupling approach [3] shows only few hundreds of kbps data rate, it is not proper for WPANs. In contrast, although the micro-range inductive coupling interconnection [4] provides few Gbps data rate, it cannot provide such high data rate in a *cm*-range interconnection. Ultra-wideband (UWB) wireless technique is another candidate for high data rate applications [1], [2]. However, UWB consumes still as much as 236mW energy [5]. Because both high data rate and low energy are important issues and they have not been achieved at once as yet, a low energy and high data rate above 100Mbps transceiver with the communication distance of *cm*-range is needed.

In this paper, we propose a dual-mode inductive coupling transceiver for low energy and high data rate. Effective inter-symbol interference (ISI) reduction scheme improves the data rate as high as 200Mbps. And the low energy consumption of only 0.02nJ/b is achieved by the proposed pulse generation scheme. By employing an adaptively enabled parallel capacitor, we can implement the dual-mode transceiver for low energy and extended range. The rest of the paper is organized as follows. In section II, the proposed system will be covered. Section III describes the design of the transceiver circuits, and section IV presents the implementation results. Finally, conclusions will be made in section V.

II. SYSTEM OVERVIEW

A. Inductive link modeling

Since larger inductance makes the communication distance longer, more than 2uH inductance is needed in this design. Considering [6], an on-board 10mm-diameter 10-turn rectangular inductor is determined. And an inductance of 2.5uH and a self-resonance frequency around 430 MHz are measured. To consider the process variation, up to 5uH inductance can be compensated by the capacitor which is in parallel with the inductor. Although the capacitance is fixed as one value, it is verified that the effect of the inductor variance is reduced.

The amplitude of the received voltage depends on the coupling coefficient, k. The received voltage $V_{out}(t)$ is derived by the transmitted voltage $V_{in}(t)$ as in (1) :

$$V_{out}(t) = k \cdot V_{in}(t)\,. \qquad (1)$$

Based on (1), coupling coefficient versus the distance between the transmitter and the receiver is measured. From the measurement result, the relationship between the distance d, and the coupling coefficient k, can be derived as in (2) :

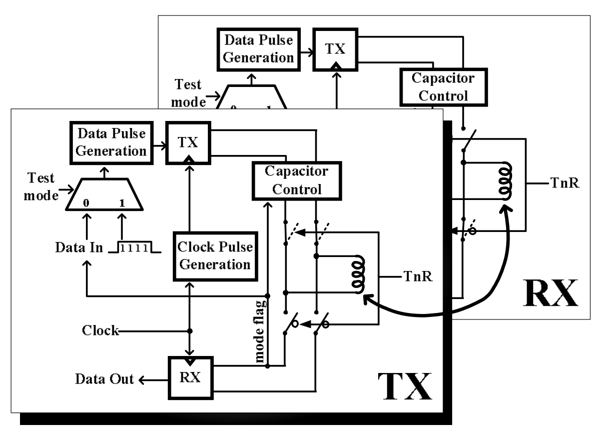

Figure 1. Transceiver block diagram

$$d \propto \frac{1}{k}. \tag{2}$$

The measured coupling coefficient k is 0.0212 at 30mm and 0.017 at 59mm. Therefore the received signals that are as small as a few tens of milli-volt levels must be recovered at the receiver.

B. *Tranceiver Operation*

Fig. 1 shows the block diagram of the proposed inductive coupling interconnection transceiver. The transceiver consists of a pulse generation block, a capacitor control block, and circuits for transmission and reception of data. The TX transmits the data as a pulse, and the RX receives the data through the inductor channel by coupling and recovers the data using Schmitt triggers. The transceiver automatically changes TnR signal to operate as a transmitter or a receiver. There are two modes for transmission. One is a power saving mode to achieve low energy consumption, and the other is an extended range mode to extend the communication distance. In the power saving mode (mode flag = “0”), an inductor is used alone for wireless interconnection antenna. To check the successful transmission, a test sequence of ‘11111111’ is periodically transmitted and TnR signal is toggled for 3 cycles. After 2 cycles, the feedback signal (mode flag) is sent from the receiver to change the transmission mode if necessary. If the test sequence is not detected properly at the receiver, the transmission mode changes into the extended range mode (mode flag = “1”) and the capacitor is used in parallel with an inductor as an antenna. By using the capacitor and the inductor together, data transmission is extended by 97%, up to 59mm.

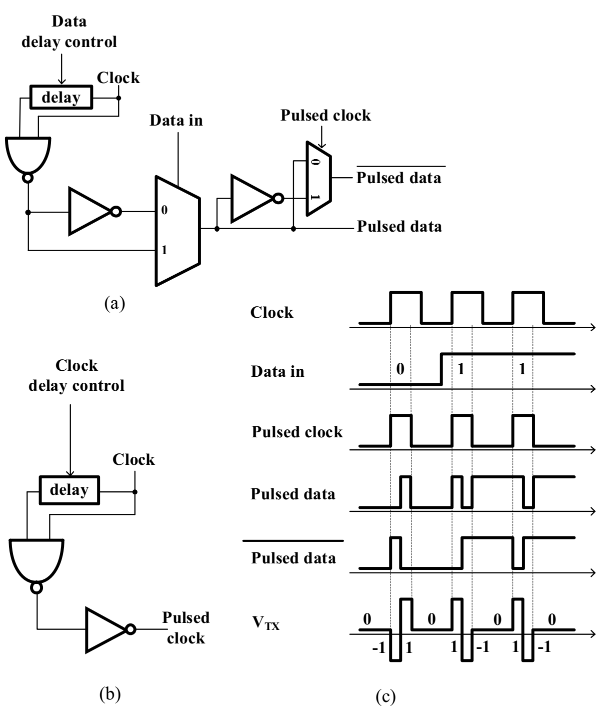

Figure 2. Pulse generation block (a) data (b) clock (c) waveforms

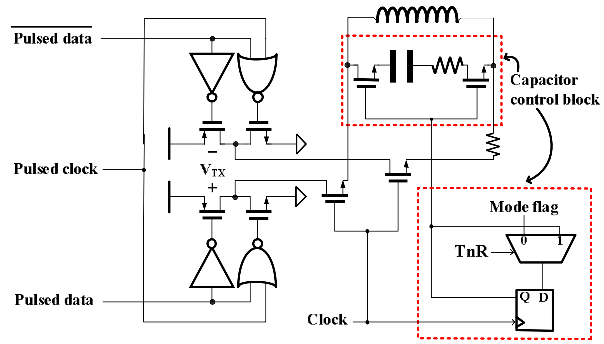

Figure 3. Transmitter and capacitor control block architecture

III. TRANSCEIVER CIRCUIT

A. *Low energy pulse generation block*

To reduce the unwanted direction current across the TX inductor, the voltage across the TX inductor (V_{TX}) should be shaped into the 2-level pulse. Fig. 2 shows pulse generation blocks of data and clock and their waveforms. A V_{TX} pulse width is controlled by the clock delay control block to reduce the energy consumption with the same slew rate [4]. The transmitter sends (-1, 1) and (1, -1) for 0 and 1, respectively. This pulse generation method is similar to the 2-level pulse generation method [3]. However the method in [3] needs two delay blocks which consume much energy to make pulses.

To reduce the energy consumption, the proposed pulse generation block of Fig. 2 employs both the data pulse and the clock pulse to make 2-level pulses. When the *pulsed clock* is low, $\overline{pulsed\_data}$ and *pulsed data* are the same. Therefore as shown in Fig. 2 (c), a V_{TX} is nominally zero at the low duration of *pulsed clock*, and the pulse generation block can operate exactly same as [3] with less energy consumption.

B. *High data rate transmitter*

Fig. 3 shows the architecture of the transmitter. It consists of H-Bridge controlled by *pulsed data* and *pulsed clock*, and 2 NMOSs which are switched by the clock.

H-Bridge transmitter is often used in inductive coupling transceiver systems [3], [4]. Most of them focus on the pulse duration control to reduce power consumption and harmonics. However, since effective ISI reduction and increasing the communication range are not considered seriously, they are additionally investigated in the proposed transmitter.

The ISI reduction technique is implemented by employing 2 NMOSs. They act similarly as a NMOS through the H-Bridge used in [3]. Since the *pulsed clock* always goes high at the rising edge of the clock, any signal in the low clock period can make ISI. Therefore it is needed to suppress the signals when the clock is low. There are two choices to solve above problem – one is to connect two bridges [3], and the other method which is proposed in this paper is to disconnect the inductor. While the approach in [3] is good for passing GND signal using a NMOS and VDD signal using a PMOS, it has a limitation to apply to the proposed transmitter architecture due to the pulse generation method. In the proposed architecture, both passing VDD signal case and passing GND signal case are occurred depending on the input data as shown in Fig. 2

(c). Therefore not a NMOS or a PMOS but a pass gate must be used to connect two bridges. However, due to the characteristic limitation of the pass gate, it doesn't operate as well. Since a NMOS can block both VDD signal and GND signal well, the method of using a NMOS only to disconnect the inductor during the low clock period is proposed. By using proposed method, the data rate increases by 14%.

C. Capacitor control block

For the complex impedance $\widetilde{Z} = R + jX$, the Q factor is the ratio of the reactance to the resistance as in (3) :

$$Q = \left| \frac{X}{R} \right|. \quad (3)$$

Because the total impedance of parallel elements is always smaller than the impedance of each element, the Q factor of a parallel LC circuit is smaller than the Q factor of L. The smaller the Q factor is, the more frequency components there are in frequency domain. And it also means that there is a steeper slope in time domain waveform. Therefore, if the parallel capacitor with the inductor is used together, the transmitted signal slew rate becomes larger.

The slew rates of two modes are shown in Fig. 4. The slew rate is increased by 8.2% in the extended range mode. Based on Fig. 4, the small signals are transmitted correctly only in the extended range mode, not in the power saving mode.

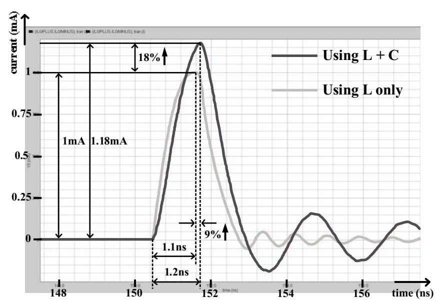

Figure 4. Slew rate of transmitted signal

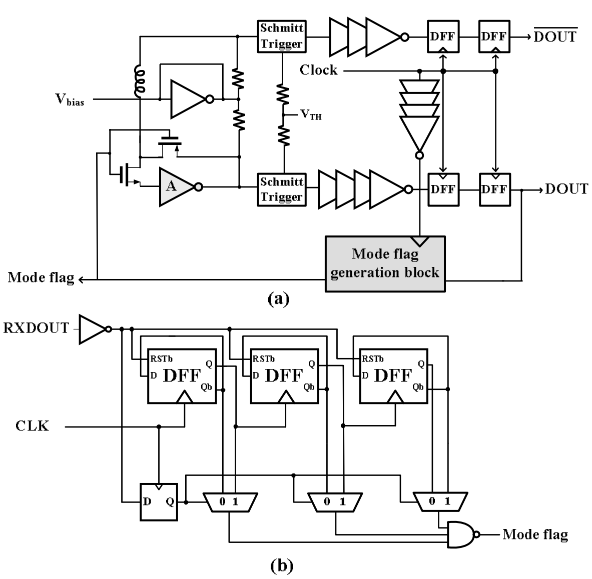

Figure 5. (a) Receiver overall architecture (b) mode flag generation block

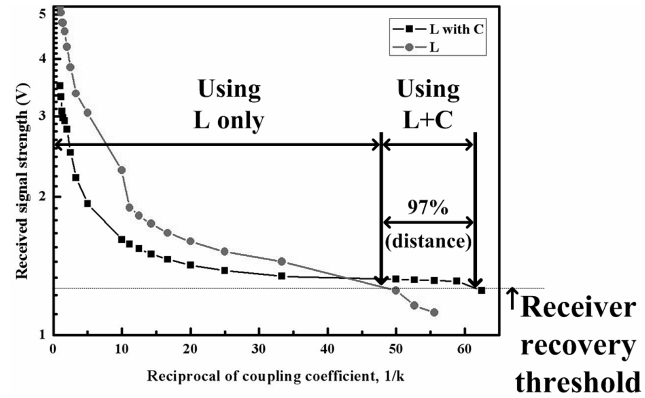

Figure 6. Received signal strength vs. reciprocal of coupling coefficient, 1/k

D. Receiver

Fig. 5 (a) shows the architecture of the receiver. It consists of two Schmitt triggers, four D flip-flops, the Mode flag generation block, and some inverters. For the successful data transmission, the mode flag is sent to the transmitter to control the capacitor control block. To achieve the low power consumption, the inverter A is not used in the power saving mode. However, the inverter A is used for detecting much smaller signals in the extended range mode. By separating the transmission mode, the power saving mode reduces power consumption by 64% and the extended range mode extends the communication distance by 97%.

Fig. 6 shows the relationship between the received signal strength and the reciprocal of the coupling coefficient at 200Mbps. As in (2), the reciprocal of the coupling coefficient is proportional to the communication distance. Therefore, Fig. 6 also means the relationship between the received signal strength and the communication distance. The distance between a transmitter and a receiver can be modeled as a value of k. And all values of k according to the distance are based on the measurement. As shown in Fig. 6, the upper bound of the transmission using the inductor alone is 30mm, and the coupling coefficient k is 0.0212. In contrast, the upper bound of the transmission using the inductor and the capacitor together is 59mm, and the coupling coefficient k is 0.017. Therefore, the inductor is used alone under 30mm and the parallel capacitor with the inductor is used together over 30mm. By adaptively changing the antenna, the transceiver can save the power and extend the communication range in each transmission mode.

The Mode flag generation block diagram is shown in Fig. 5 (b). The Mode flag generation block consists of a 3-bit counter, a 3-input NAND gate, 3 multiplexers, and a D flip-flop. The only case that mode flag becomes 0 is that the input sequence '11111111' is detected correctly; otherwise, counter is reset to '0'. This value is sent to transmitter only when the Test flag in the transmitter is 1, because TnR signal is only toggled when Test flag is '1' in the transmitter. If the mode flag received in the transmitter is '0', the transmitter operates in the power saving mode; otherwise the transmitter operates in the extended range mode.

IV. Implementation Result

Fig. 7 shows the simulation results of successful data transmissions at 200Mbps data rate. The coupling coefficient k in Fig. 7 (a) is 0.02, and k in Fig. 7 (b) is 0.7. In case of Fig. 7 (a), the transceiver operates in the power saving mode initially, and the transmission fails. After a few clock cycles, the Test flag is set and transmitter sends the test sequence ‘11111111’ to the receiver. It isn’t received correctly; therefore the transmission mode is changed into the extended range mode. The TnR signal in transmitter is toggled for 3 cycles to receive the Mode flag. After the mode change, the transmission becomes successful. In Fig. 7 (b), the transceiver operates in the power saving mode successfully. Therefore, after the test sequence is transmitted, the transmission mode does not change and the transmission is still successful.

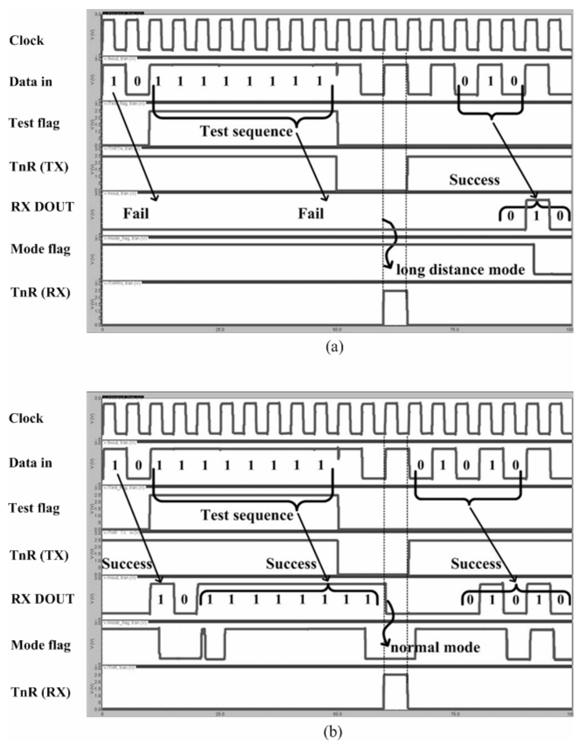

Figure 7. Data transfer waveform at 200Mbps (a) k = 0.02 (b) k = 0.7

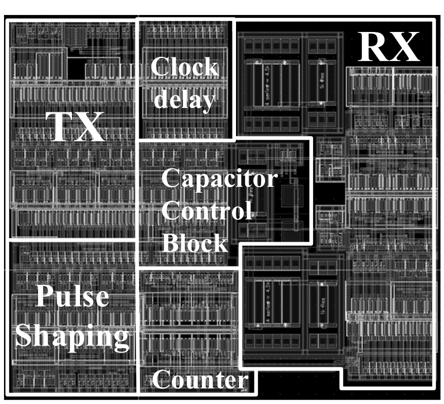

Figure 8. Layout photo (0.12mm x 0.1mm except pads)

TABLE I. Performance Comparison

REF. No.	ESSCIRC2007 [3]	ISSCC2007 [5]	ISWC2004 [7]	This work	
Mode	-	-	-	**Power Saving**	**Extended range**
Process	90nm	0.18um	-	**0.25um**	
Data rate	250kbps	400Mbps	100kbps	**200Mbps**	
Energy/bit	0.72nJ/b	0.59nJ/b	0.8nJ/b	**0.02nJ/b**	**0.032nJ/b**
Wireless Interface	Inductive (76nH)	UWB	Inductive (3.1uH)	**Inductive (2.5uH – TRX)**	
Communication distance	50mm	-	20mm	**30mm**	**59mm**

Fig. 8 shows the layout using 0.25um standard CMOS technology. The layout area except pad is $0.012mm^2$.

The performance comparison with other works is shown in Table I with respect to data rate, energy per bit and the communication distance. The proposed transceiver shows the lowest energy consumption and comparable or longer communication range with high data rate among other researches.

V. Conclusion

A 200Mbps 0.02nJ/b dual-mode transceiver for *cm*-range inductive coupling is designed and implemented at 0.25um CMOS process. The proposed pulse generation scheme makes the transceiver consume only 0.02nJ/b energy under 2.5V supply voltage. And an effective ISI reduction scheme improves the data rate up to 200Mbps. The parallel capacitor with the inductor increases communication distance by enhancing the transmitter signal slew rate. By employing an adaptively enabled parallel capacitor, the dual-mode transceiver for low energy consumption and extended range can be implemented. The transceiver consumes $0.012mm^2$ area at 0.25um CMOS process.

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