480ps 64-bit Race Logic Adder

Se-Joong Lee*, Ramchan Woo, and Hoi-Jun Yoo

Semiconductor System Laboratory
Department of Electrical Engineering
Korea Advanced Institute of Science and Technology (KAIST)
Outline

- Introduction
- Overall Architecture
- Fast Carry Generation for 64-bit Adder
- Simulation Results
- Conclusion
Introduction

Why Race Logic?

- Boolean Function
- Sum of Product, Product of Sum
  - Sum
  - Product
  - Race Logic
  - Wired-OR
  - Wave Pipelining
Introduction

Race Logic Architecture

Se-Joong Lee et al., IEEE ESSCIRC, 2000
Introduction

Test Chip Fabrication

- 64-bit CLA using Race Logic
- 0.25μm CMOS technology
- 6-metal (1W, 5Al)
- Clk – S31 : 0.9ns

Die Photo

Measured Waveform
Introduction

How Race Logic Works?
Introduction

A \cdot B operation
Introduction

A + B operation
64-bit Adder with Race Logic


8-bit CLA  g/k  8-bit CLA  g/k  8-bit CLA  g/k  8-bit CLA
8-bit CLA  G^g/G^k  8-bit CLA  G^g/G^k  8-bit CLA  G^g/G^k  8-bit CLA
8-bit CLA  G^g/G^k  8-bit CLA  G^g/G^k  8-bit CLA  G^g/G^k  8-bit CLA

G^g/G^k

MUX  c_55  MUX  c_47  MUX  c_7
S<56:63>  S<48:55>  S<8:15>  S<0:7>

Race Logic
Carry Generation Circuit

2-Level Gg/Gk Architecture

- Pre-process
- Level-1
- Level-2
Level-1 Group ‘g’ and ‘k’

Boolean Function

\[ G^1g = g_7 + \overline{k_7} \{ g_6 + \overline{k_6} \{ \ldots \{ g_1 + \overline{k_1} g_0 \} \} \} \]

\[ G^1k = k_7 + g_7 \{ k_6 + g_6 \{ \ldots \{ k_1 + g_1 k_0 \} \} \} \]

\[ g = A \cdot B \]

\[ k = \overline{A+B} \]
Level-1 Group ‘g’ and ‘k’

Schematic
Level-1 Group ‘g’ and ‘k’

Winner-Take-All Circuit

"Winner Passes"

"Loser Blocked"

Stay High

Turned off
Level-1 Group ‘g’ and ‘k’

Simulation Results

- 0.18μm CMOS param.
- Vdd = 1.62 V
- OUT follows G-line
- OUT stays High
- Delay time of WTAC = 15psec
Level-2 Group ‘g’ and ‘k’

Generates Every Carry Simultaneously
Level-2 Group ‘g’ and ‘k’
Level-2 Group ‘g’ and ‘k’

Simulation Results

(a) The worst Case
(Only $g_0$ is ‘1’)

(b) The best Case
(All of $g_i$ are ‘1’)

clk
C7~C55

clk
C7~C55
Simulation Results

- 0.18\(\mu\)m CMOS model parameter
- \(V_{dd} = 1.62\) V
- \(T = 85\) \(^0\)C
- \(Clk-S63 = 480\) ps
Simulation Results

Delay Time Analysis

203ps

57+185+218=460ps

480ps
Layout View

- g/k
- $G^1g/G^1k$
- $G^2g/G^2k$
- 8-bit CLAs
- MUX
- Clock Generator

Dimensions:
- 20% of total area
- 180μm
- 490μm
Conclusion

- 480ps 64-bit Race Logic Adder is designed by 0.18\(\mu\)m CMOS technology

- For Race Logic Adder, 2-Level Group generate and kill scheme is suggested

- Race Logic is successfully employed to design high-speed carry generation circuit