One chip - low power Digital-TCXO with Sub-ppm Accuracy

Se-Joong Lee, Jin-Ho Han, Seung-Ho Han*, Joo-Ho Lee, Jung-Su Kim, Min-Kyu Je and Hoi-Jun Yoo
Department of Electrical Engineering
Korea Advanced Institute of Science and Technology
Kusong-dong, Yuseong-gu, Taegon, Korea
(email : shocktop@einfo.kaist.ac.kr)
* ShinSung Elec. co., LTD
714-8 Mora-dong, Sasang-gu, Pusan, Korea

ABSTRACT

The digital TCXO(DTCXO) has been studied extensively because of its high frequency accuracy and rapid start-up time. The value of compensation capacitance used in the DTCXO is stored in ROM or calculated by computing circuit. In this work, ROM and computing circuit are integrated together to obtain the merit of both schemes: accurate value and high resolution of compensation capacitance, respectively.

The DTCXO contains temperature sensor, A/D converter, controller, EEPROM, capacitor bank, and oscillator. The oscillation frequency can be pulled from ±25ppm to the required frequency with sub-ppm accuracy. The maximum power consumption of the total chip is 6.6mW at 3.3V. The chip, die size of 9mm², is fabricated by a 0.5μm CMOS technology.

I. Introduction

Crystal oscillators play an important role in modern electronic circuits and systems. The resonant frequency of a crystal is accurately defined and its quality factor is very high, usually more than 10,000[1]. Whenever an application requires precise definition of oscillation frequency, low phase noise and low power, a crystal oscillator is the best candidate.

However, in communication systems, stability of oscillator is so critical that deviation of frequency due to temperature variation causes a serious problem. To improve accuracy of frequency, compensation circuits should be added to the oscillator. The only way to tune the frequency is by varying the equivalent capacitance parallel to the oscillator. These kinds of circuits are called TCXO(Temperature Compensation X-tal Oscillator)[2]. Recently, Digital-TCXOs are popular because of their accurate compensation ability and possibility of implementation in VLSI.

There are two approaches in implementation of a DTCXO.

One uses an integrated memory to store the information of compensation capacitor, and the other uses an computing circuit to generate the value of compensation capacitor. The calculation results obtained by computing circuit may differ from the real characteristics of the crystal oscillator. Memory scheme can achieve more accurate temperature compensation based on the real measured characteristics of crystal oscillator. But the frequency resolution is limited by the memory size.

In this work, we overcome these limitations by combining the merits of computing circuit method and memory approach; high accuracy of memory scheme and high resolution of computing circuit method.

Another feature of this work is the hierarchical capacitor bank scheme. Crystal oscillator shows different Δf for the same ΔC as C increases. We use two separate capacitor banks for equal accuracy irrespective of the value of C.

The proposed DTCXO consists of oscillator, temperature sensor, A/D converter, controller, memory, and capacitor bank. The DTCXO can program the EEPROM based on the measured characteristics of crystal oscillator, and the EEPROM whether the program is written correctly or not, and performs the temperature compensation. Temperature compensation range is from -40°C to 85°C.

II. Basics of a DTCXO

One of the widely known oscillator structures is the so called three-point oscillator shown in Fig.1[2]. For the best trade-off between frequency stability and required transconductance of M1, C1 and C2 should be equal. The oscillation frequency of the circuit is given by[1],

\[ f_{osc} = \frac{1}{2\pi \sqrt{\frac{CSC_L}{CSC_L + C_L}}} \approx \frac{1}{2\pi \sqrt{LSC_S}} \left(1 + \frac{C_S}{2C_L}\right) \]
The only way to tune the oscillation frequency is by varying $C_L$. To vary the value of $C_L$, additional capacitors should be attached parallel with $C_1$ and $C_2$.

![Diagram](image)

Fig. 1. The basic structure of a oscillator

Conventional DTCXO uses a varactor diode as a compensation capacitor. But they are not suitable for on chip VLSI, because a varactor diode cannot be formed on a VLSI chip[3]. Recent DTCXO has replaced varactor diode with capacitor array. Because these DTCXOs do not require a varactor diode, they can be integrated on a single chip. The block diagram of the recent DTCXO is shown in figure 2.

![Diagram](image)

Fig. 2. Operations of a DTCXO

On-chip temperature sensor detects the temperature variation and generates the DC voltage according to the temperature. The A/D converter changes the DC voltage into 9bit digital signal. The controller, which received 9bit data, finds the proper compensation capacitor value from EEPROM, and issues command signals to the capacitor-switch network to change the value of capacitance. By varying the value of capacitance, the frequency of the crystal oscillator is compensated to generate an accurate resonance frequency.

![Diagram](image)

Fig. 3. Block diagram of the designed DTCXO

III. Structure of the designed DTCXO

Figure 3 shows the block diagram of the overall system. The system consists of mainly five parts; oscillator, capacitor bank, temperature sensor, controller, and memory. The capacitor bank is divided into four sub-banks. FSB determines the center of resonant frequency. With this sub-bank, user can adjust the center frequency of the crystal oscillator. TCB1 and TCB2 are used to compensate the frequency against temperature variation. TCB1 and TCB2 contain capacitor-switch array of which unit cell is shown in figure 4.

The capacitance value of the unit cell of TCB2 is 48F which is larger than that of TCB1, 36F. This dual size bank configuration is more effective than single size bank because the DTCXO can choose the bank selectively according to the temperature range, which will be detailed in section IV. The size of the unit capacitor is determined by the trade-off between accuracy of frequency and silicon area. Larger unit capacitor size means fewer number of unit cells and smaller means more cells on the same area. We decided to use 224 units per bank as shown in figure 4. Frequency deviation by temperature is mainly occurs in the range from $-40^\circ C$ to $85^\circ C$, and maximum variation is $\pm 30$ppm in this range. Considering the margin, the capacitor bank should be able to compensate the frequency by $\pm 40$ppm with 224 unit capacitors. This implies that frequency compensation per one unit capacitor should be 0.2ppm/bit. To obtain 0.2ppm/bit, the value of the unit poly-oxide-poly capacitor is chosen to be 36F.

![Diagram](image)

Fig. 4. Structure of the capacitor bank and an unit cell

VCB is for voltage controlled oscillator application. The oscillation frequency can be varied by the applied voltage on VCB_CTRL pin.

A Switch-Current, Switch-Capacitor Temperature Sensor scheme is used to implement temperature sensor[4]. In this
scheme, the resulting PTAT $\delta V_{BE}$ signal is amplified in an auto-zeroed switched-capacitor circuit, and converted to a digital output by SAR ADC. The temperature sensor provides a resolution of 0.5°C from -55°C to 120°C.

EEPROM is used to store programed data at off-power condition. The EEPROM has two banks; one is for storing the temperature compensation data, and the other is for storing the program codes for the controller. Memory size for compensation data and program code is 1Kbit and 64bit, respectively.

The controller, which is located in the center of block diagram, checks the temperature value from the temperature sensor, reads or writes data in the EEPROM, and issues command signals for the capacitor bank to vary the value of capacitance. Detailed operations of the controller will be described in the next section.

IV. Operations of the Controller

The controller consists of mode-controller, register file, ALU, I/O controller, and peripheral block as shown in figure 5. Mode controller is implemented with finite state machine. Peripheral block determines the mode of the controller. Register file has 10 registers; 3 memory registers, 6 internal registers and 1 temperature sensor register. Memory registers are concerned with address, input data, and output data. Internal registers are special purposed registers. The ALU block can perform two-operands addition, subtraction, and interpolation.

![Fig. 5. Block diagram of the Controller](image)

The controller has four operational modes: calibration, program, memory test, and operation mode. In the calibration mode, the controller senses oscillator temperature and outputs the value to outside of the chip. The value of compensation capacitance is selected for the specific temperature. This is repeated with varying temperature from -40°C to 85°C.

Finally, a table containing the necessary capacitor values at each measured temperature is completed.

To store the table and other informations in EEPROM, programming mode is used. The controller programs EEPROM which is monolithically integrated on the chip. After programming, the controller reads the data of EEPROM over the all addresses, or the chip is in the memory-test mode.

The normal mode of the DTCXO is the operation mode. When the chip works in operation mode, resonant frequency of the crystal oscillator is fixed by sub-ppm accuracy. The controller, first, gets temperature information from temperature sensor. According to the temperature value, controller brings a compensation capacitance data from the EEPROM to tune the oscillator. To reduce the size of temperature compensation data, the controller uses an interpolation scheme. Although a temperature sensor provides 0.5°C resolution, the value of compensation capacitor is recorded with 1°C resolution in the EEPROM. Therefore, to find out the proper value of compensation capacitor for the disaligned temperature, ALU of the controller interpolates the two neighbor values. The controller sets the proper capacitance values to two different banks, and repeats the sequence from sensing temperature task again.

When the controller sets capacitance values to the capacitor bank, it can use two banks - TCB1 and TCB2. The unit cell of TCB2 is larger than that of TCB1. If the controller wants a large variation of frequency by an unit capacitor, it uses TCB2. On the other hand, if the controller wants a small variation, it uses TCB1.

Figure 6 shows the relationships between $C_L$ and $\Delta f$. First, the controller figures out the position at which the frequency of oscillator is located. If the position is in the region I, the controller uses TCB1, and if the region II, TCB2 is used. Because the slope of curve in region II is flatter than that of region I, larger unit capacitor is necessary to obtain the same accuracy as that of region I.

![Fig. 6. Frequency variation vs. compensation capacitance curve](image)
The overall operations of controller is shown in figure 7.

![Diagram of controller operations](image)

Fig. 7. Operational modes of the Controller

V. Experimental Results

The designed DTCXO was fabricated using 0.5 \( \mu \)m CMOS process. Except the controller block which was synthesized by CAD tool, all blocks are designed in full custom. The total power consumption is 66mW at 3.3V, and die size is 9mm\(^2\). The frequency variation was measured while changing the controller outputs to capacitor bank as shown in figure 8. The larger the code is, the more capacitors are activated to compensate large variation. As shown in figure 8, the measured data show good consistency with simulated results.

![Graph of frequency calibration](image)

Fig. 8. Measured characteristics of frequency calibration with variation of the number of activated capacitors

VI. Summary

To develop a one chip - low power Digital TCXO with sub-ppm accuracy, functional blocks such as oscillator, capacitor bank, temperature sensor, controller and EEPROM are integrated monolithically by 0.5 \( \mu \)m CMOS process. The controller of the DTCXO have 4 operational modes; calibration, programming, memory test and operation mode. The accuracy of the oscillation frequency is sub-ppm because the unit cell capacitor of the capacitor bank is 36fF. The measured results show the frequency can be compensated by \( \pm 40 \)ppm when the total capacitors are activated in the capacitor bank. The chip area is 9mm\(^2\) and power consumption is 66mW at 3.3V.

References


