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The Reference Ear Modeling Method for Internally Feedback Controlled Digital Hearing Aid Chip

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***Abstract*—A reference ear modeling method for the real-time feedback controlled digital hearing aid chip is proposed and implemented. In order to reduce the modeling complexity and enhance the programmability, new ear modeling method using the acoustic filter theory is adopted to the digital hearing aid. To achieve the fully internal gain fitting and verification system, the responses from the damaged ear and the reference ear model are compared and the new gain parameters are processed for the multi-channel DSP. The digital hearing aid chip with reference ear model is fabricated in 0.18 µm CMOS technology, has a core area of 3.1 mm x 1.2 mm and dissipates less than 120 µA.**

I. Introduction

IN THESE DAYS the design paradigms of the biomedical devices are shifted to the 2nd generation. The main differences of the 2nd generation biomedical devices from the 1st generation are the consumer flexibility, reliability and user-optimized performance rather than high capacity or straight forward design which requires the user adaptation to the biomedical devices [1]. The 1st generation of the digital hearing aid demands the innovation of design approach to satisfy the various user requirements [2, 3]. Fig.1 (a) presents the architecture of the conventional digital hearing aid system. It is hard to customize the performance of the digital hearing aid according to the each individual user because of the open loop gain fitting and verification features. Moreover, this open loop architecture enables the only off-chip gain fitting and verification. It requires the additional control signals and several hearing loss tests. To achieve the high performance optimization and the comfort level for the patient the hearing aid chip incorporates the human factors before the chip fabrication by adopting the pre fitting verification algorithm and the ear modeling filter circuit in Fig.1 (b) [4]. In spite of its fast gain fitting, it still demands several external hearing loss test results because of open loop system. To enhance the user optimized design with single hearing loss test result and minimize the internal gain error for high accuracy the digital hearing aid chip should incorporate with the closed loop system to generate the DSP gain parameters.

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The advantages of the closed loop control system are already well known in many control system applications through various articles and designs.

Fig.1 (c) shows the newly implemented digital hearing aid chip with reference ear model and the comparison processor. To achieve the fully internal gain fitting and verification with only single external hearing loss test, the fabricated chip adopts the closed loop control technique for internal gain verification. From the comparison results between the reference ear model response and the damaged ear response, the DSP gain parameters are generated and used to compensate the hearing loss of the patient to the ideal reference ear.

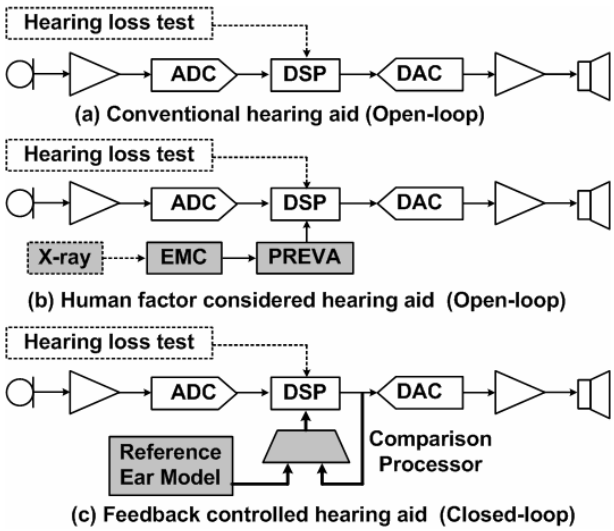

Fig. 1. Digital hearing aid architectures.

II. Modeling Overview

A. Various Human Ear Modeling Methods

Modeling of the human ear function has been described by adopting various approaches. The finite element method (FEM), a general numerical procedure, is usually used in modeling complex electro-mechanical biological system [5]. Although the FEM is accurate and intuitive method to model the human ear, it is hard to integrate the FEM algorithm into the digital hearing aid chip because of the seriously complex data processing algorithm of the FEM. The conventional analog human ear model is constructed by converting the ear

transfer function into the transformer circuit with passive or active analog circuit elements [6]. However, the inflexibility of the analog circuit and the excessively large values of the passive elements made it impossible to apply the conventional analog ear model to the digital hearing aid on a chip. To achieve the accurate and flexible ear modeling method to consider the human factors, the reference ear modeling filter circuit is newly implemented and embedded to the digital hearing aid on a chip.

B. Acoustic Analogies for the Reference Ear Model

In the acoustic filter theory, the side branch or winding of the pipe can attenuate sound energy transmitted in a pipe. Moreover, the input impedance of the side branch determines whether the system can have as a low-pass, high-pass or band-pass filters [7]. A low pass filter in Fig. 2 (a) is consisting of an enlarged segment of a pipe of cross-sectional area S_1 and length L in a pipe of cross-section S. At sufficiently low frequencies, the low pass filter is viewed as a side branch with acoustic compliance C in the form of (1) as

$$C = \frac{S_1 L}{\rho_0 c^2} \tag{1}$$

In this case, the acoustic impedance of this branch is pure reactance and it is presented in the form of (2) as

$$R_g = 0, X_g = -\frac{1}{C\omega} = -\frac{\rho_0 c^2}{S_1 L \omega} \tag{2}$$

A high pass filter is created by attaching a short length of pipe as a branch to a main pipe. Both the radius A and length L of this structure are small compared to a wavelength. In this case, the branch impedance of this high pass filter is given by

$$Z_g = -\frac{k\rho_0 c^2}{4\pi} + i\frac{\rho_0 \omega (L + 1.5A)}{\pi A^2} \tag{3}$$

To design the acoustic networks using the cross-sectional area of the closed-end pipe, a ladder-type network is used as an acoustic filter. One value of inductor (L) and one value of capacitor (C) are constructed as a one unit of the proposed filter.

The human external ear can be modeled into the closed-ended pipe which has various windings or side branches. In addition the sliced disk of the human external ear which has unit length L is characterized into the low pass filter or the high pass filter according to the announced acoustic theory. By using these analogies between the closed-ended pipe of the acoustic filter and the human external ear canal, reference ear modeling filter circuit is extracted. Fig. 2 (b) shows the response of the reference ear model unit compared with the natural response of the normal ear. The parameters from the external hearing loss test can input to the digital hearing aid through the serial interface.

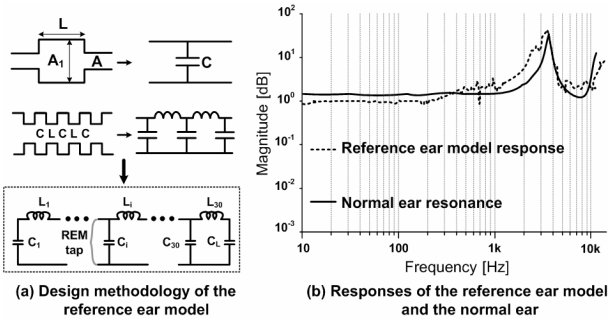

Fig. 2. Acoustic analogies for the reference ear model.

III. Design Considerations

A. Reference Ear Modeling Filter Circuit

Fig. 3 presents the fabricated reference ear model unit which models the reference ear to obtain the natural resonance values of the human external ear. The exact 2-D shape of the handicapped external ear can be formed based on the X-ray photo of the human. By using the X-ray photo results the cross-sectional area of the external ear is extracted. Then, a distributed LC filter is derived to model the acoustic filter characteristics of the external ear by using the achieved data from the X-ray photo. The achieved LC filter is embedded into the hearing aid chip to enable the feedback controlled gain fitting and verification for human-chip co-design.

The characteristics of the reference ear model can be changed according to the user requirements by adopting the external control signal CS_{REM}. It enables the high flexibility of the digital hearing aid by changing the value of the L or C. In this design, the reference ear model unit is designed to provide 30 taps and each tap has single L and C components. Since the typical length of the human external ear is about 30 mm, each cross-section of the external ear has 1 mm unit and it realizes the each tap of the reference ear model.

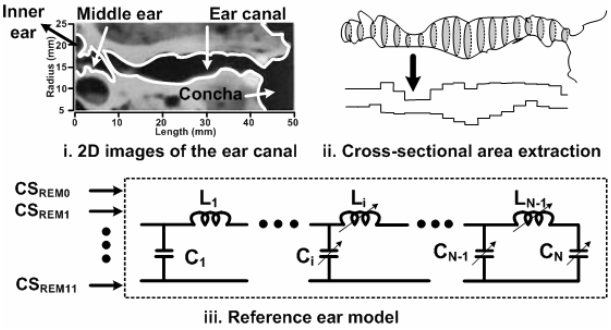

Fig. 3. Design of the reference ear model.

B. Overall Digital Hearing Aid System Design

Fig.4. presents the block diagram of the fabricated hearing aid chip with the reference ear model and the comparison processor. Through the envelope detector, the peak gain

values of the normal external ear from the REM responses are achieved as a function of frequency from 1 kHz to 8 kHz in steps of 1 kHz and digitized to 5 bit gain parameters. The introduced gain parameter, P_{REM}, from the reference ear model unit are stored in the internal register and processed to choose proper resonance value. To reduce the design difficulty and the power consumption of the overall chip, the three frequency channels are selected among the eight channels from the 1 kHz to 8 kHz. Because of its enormous influence to the gain fitting and verification of the digital hearing aid, the response of the reference ear model unit at the 2 kHz is usually taken into account. The parameter value which has the largest amplitude among the outputs of the SAADC and the parameter value at the 2 kHz are decided to the compensation parameters for the reference ear model unit (P_{REM}). From the hearing loss test the parameter values both at the 2 KHz and the one which has the largest amplitude are also decided to the compensation parameter (P_{HLT}) for the DSP. For the initial DSP gain fitting, the 1st parameter computation is accomplished by using the parameters both from the single hearing loss test, P_{HLT}, and the reference ear model response, P_{REM}. The values of the P_{HLT} are compared with the P_{REM} as a function of frequency. The differences between the two parameters are recognized by the parameter comparator and used to generate the new parameter, P_{TOT1}, to compensate these differences through the parameter synchronizer. During the 2nd gain verification, the newly generated DSP parameter from the 1st parameter computation, P_{PAT1}, is compared with the parameter from the reference ear model unit, P_{REM}, again to achieve the parameter differences for determining the verified gain. The acquired parameter, P_{TOT2}, from the 2nd parameter computation achieves the fine gain compensation to reduce the gain difference between the normal ear and the damaged ear by the multi-internal iterations. The parameter computation is continued until the parameter difference between the P_{REM} and the P_{TOTi} is minimized enough to satisfy the specific reference value.

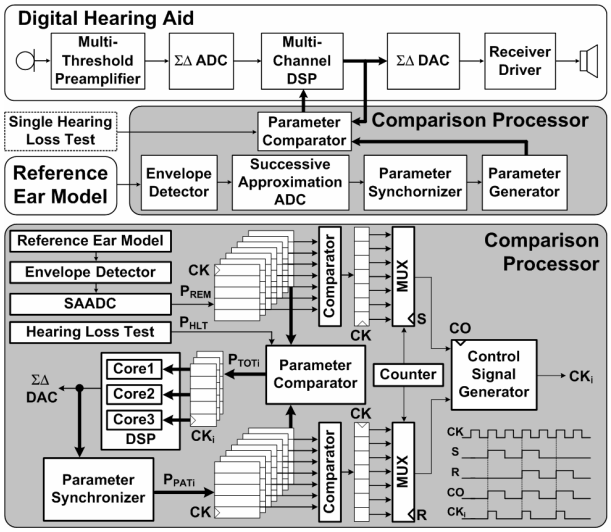

Fig. 4. Digital hearing aid architecture.

IV. Implementation Results

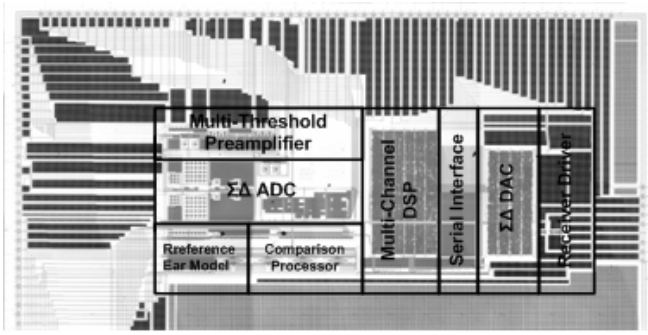

Fig. 5. Die micrograph.

Fig. 5 shows the die microphotograph of the digital hearing aid chip with the reference ear modeling circuit. It is fabricated in a 0.18 μm standard CMOS technology and the core area is 3.1 mm x 1.2 mm. The current dissipation of the digital hearing aid is less than 120 μA from a single 0.9 V supply.

The overall operation of the fabricated digital hearing aid chip is shown in Fig. 6. A hearing loss audiogram of a patient in Fig. 6(a) shows losses at 2 kHz and 4 kHz. In order to compensate such hearing losses, the compensation parameter is selected from the difference between the responses of the impaired ear and of the reference ear model. By adopting this parameter overall gain of the hearing aid is compensation in Fig. 6(b). The Fig. 6(c) shows the final compensation results by the comparison processor with multi internal iterations. In this case, the preamplifier gain is selected as 1 to verify the performance of the comparison processor with the reference ear model. Compared with the conventional open loop hearing aid this system enables the fast and accurate on-chip gain fitting and verification by incorporating the fully internal feedback with single hearing loss test.

Fig. 7 shows the measured results of the fabricated comparison processor with the result of the reference ear modeling circuit. After the peak values of the resonance signals of the patient are detected and inputted to the comparison processor in Fig. 7(a) to compare with the response of the reference ear model, the gain values are measured and digitized in Fig. 7(b). Finally, two gain values, the largest gain value and the gain value at the 2 kHz, are selected to achieve the internal verification gain in Fig. 7(c).

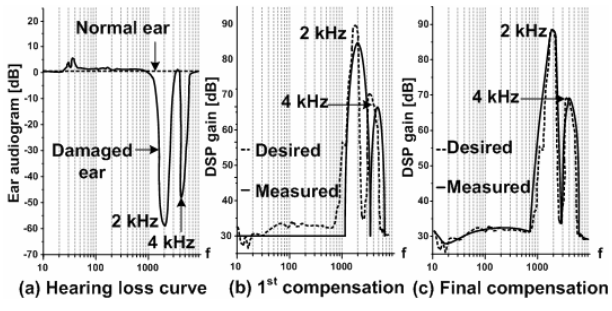

Fig. 6. Measurement results of the digital hearing aid chip.

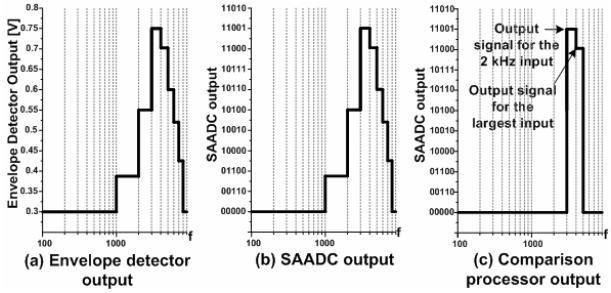

Fig. 7. Measurement results of the comparison processor.

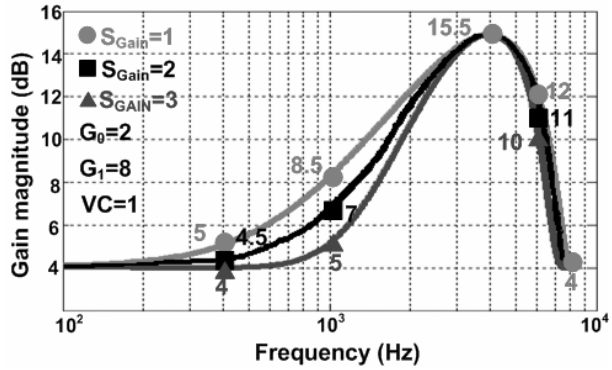

Fig.8. Measurement results of the multi-channel DSP.

Fig. 8 plots the frequency compensated gain characteristics of the DSP for ski-slope loss. By using parameter values to control the gain of the hearing aid, ski-slope is well compensated. TABLE I and TABLE II represents the performance of the fabricated chip. The current consumption of the complete digital hearing aid chip is less than 120 μA from a 0.9 V supply. The performance comparison with the other works related to the hearing aid chip is summarized in TABLE III. The main points are the design techniques based on the internal verification and power consumption. As a result, this work newly introduces the reference ear model with the comparison processor with the lowest power consumption.

TABLE I
PERFORMANCE SUMMARY (OVERALL SYSTEM)

Current consumption	< 120 μA
Supply voltage	0.9 V
-3 dB bandwidth	8 kHz
Input referred noise	4.2 μV_{RMS}
SNR_{PEAK}	81 dB
Core area	3.1 mm x 1.2 mm
Process	0.18 µm standard CMOS technology

TABLE II
PERFORMANCE SUMMARY (BUILDING BLOCKS)

Multi-threshold preamplifier	$Gain_{MAX}$	36 dB
	Current consumption	35.6 µA
	Output DR	0.45 V – 0.8 V
Adaptive-SNR ΣΔ ADC	SNRmax	87 dB
	SNRmin	73 dB
Multi-Channel DSP	Gate count	10 K
	Clock frequency	32 kHz
Heterogeneous ΣΔ DAC	Gate count	16 K
	Input frequency	512 kHz
	Clock frequency	2048 kHz

TABLE III
PERFORMANCE COMPARISON

	Neuteboom [8]	S. Graells [9]	This work
SNR_{PEAK}	77 dBA	70 dB	81 dB
Supply Voltage	1.3 V	1.0 V	0.9 V
Design Type	Digital	Programming	Digital
Feedback Controlled Design	No	No	Yes
CMOS Process	0.8 µm	1.2 µm	0.18 µm
Current cons.	1.5 mA	300 µA	< 120 µA
Area	35 mm^2	7.5 mm^2	3.72 mm^2

V. CONCLUSION

A reference ear modeling method and the comparison processor are newly implemented and embedded to the real-time feedback controlled digital hearing aid chip. It enables the fully internal DSP gain fitting and verification with single hearing loss test and internal error reduction using feedback technique. To compensate the hearing loss of the damaged ear, the response differences between the reference ear model and the damaged ear of the patient are achieved and processed to generate the gain parameters. To reduce the power compensation and achieve high flexibility, the multi-threshold preamplifier and multi-channel DSP are implemented. The hearing aid chip is fabricated in a 0.18 µm standard CMOS process and consumes less than 120 μA with a 0.9 V single supply.

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