An Energy-Efficient Analog Front-End Circuit for a Sub-1V Digital Hearing Aid Chip

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Abstract

A low-power, energy-efficient analog front-end circuit is proposed and implemented for a digital hearing aid chip. It adopts the combined-gain-control (CGC) technique for an accurate preamplification and the adaptive-SNR (ASNR) technique for an improvement of dynamic range with low power consumption. The proposed analog front-end achieves 87-dB peak SNR and dissipates 60-μW from a single 0.9-V supply. The core area is 0.5-mm² in a 0.25-μm standard CMOS technology.

Keywords: analog front-end, adaptive SNR technique, combined-gain-control technique, digital hearing aid

System Design Consideration

The proposed analog front-end consists of a preamplifier and a Σ-∆ modulator. The preamplifier uses CGC technique for accurate preamplification and Σ-∆ modulator adopts ASNR for wide dynamic range with low power consumption. The architecture of the proposed analog front end is shown in Fig. 1. The proposed analog front-end architecture achieves not only the high performance but also the power optimization to the external environment. This analog front-end includes an off-chip DSP for analyzing and modifying parameters. In the conventional preamplifier, an automatic gain control (AGC) and an exponential gain control (EGC) are designed separately because of its design difficulties. In this study, however, CGC integrates AGC and EGC into a single block to reduce power consumption and to expand its dynamic range.

The Fig. 2 shows the relationship between the input of a microphone and the input of the preamplifier. A preceding study reveals that a normal sound level, which is common in human daily life, is from 30 to 90-dB SPL, the Range 1 in Fig. 2 [4]. In this range, the sound amplitude is so small that high performance analog front-end must be used. On the other hand over 90-dB SPL, Region 2–4, high performance analog front-end is not necessary since the sound amplitude is sufficiently large. If we use the high performance analog front-end both in the entire sound regions, the analog front-end produces excessive performance and dissipates power needlessly. In the design of the new Σ-∆ modulator, input sound level is divided into four parts as described in Fig. 2 to control SNR separately at each range to optimize its power and performance.

Fig. 1 Proposed analog front-end

![Fig. 1 Proposed analog front-end](image-url)
The Fig. 3 shows the proposed preamplifier with CGC technique. The $V_{TH}$ is an external control parameter which determines the threshold knee voltage. The gain is given as follows.

$$\text{Gain} = \frac{V_{OUT}}{V_{IN}} = \frac{W_{1}L_{2}}{W_{2}L_{1}}\left[1+\frac{V_{X}}{V_{ad}}\right]$$

where $V_{1}$ and $V_{2}$ are negative and positive resistance-control-voltage-outputs, respectively, generated by the gain control unit (GCU). The $V_{VC}$ is a volume control voltage which determines the common mode level of $V_{1}$ and $V_{2}$. The $V_{X}$, a control voltage decided by the preamplifier output, decides the differential mode level of $V_{1}$ and $V_{2}$. The $W_{1}$, $W_{2}$ and $L_{1}$, $L_{2}$ are the width and the length of the transistor $M_{1}$ and $M_{2}$, respectively. The $V_{ad}$ is a supply voltage of the analog front-end circuit.

The MOS resistive circuit (MRC), which is composed of four N-type transistors $M_{1}$ and $M_{2}$, enables to obtain the exponential gain characteristics in accordance with gain amplifier (GA). In addition, the GCU with the peak detector (PD) helps CGC to get the automatic gain characteristics. The PD senses the envelope of the output voltage and controls the GCU.

The gain and the threshold knee point of the preamplifier can be changed by varying $V_{VC}$ and $V_{TH}$, respectively. When the value of $V_{VC}$ is low, the threshold gain, a gain which the threshold knee point is applied, decreases according to (1) and the power dissipation of the preamplifier is reduced. On the other hand when the value of $V_{VC}$ is high, the threshold gain grows up and the required resolution of the next-stage $\Sigma$-$\Delta$ modulator is decreased.

B. The $\Sigma$-$\Delta$ modulator with adaptive SNR technique

To provide wide dynamic range, the $\Sigma$-$\Delta$ modulator should provide different kinds of SNR values according to the input amplitudes. There have been studies on achieving different SNRs and one method is changing the clock frequency. By changing clock frequency, the $\Sigma$-$\Delta$ modulator achieves different SNR characteristics. But adopting high clock frequency makes the design of an analog circuit difficult such as operational transconductance amplifier (OTA), since the unity-gain frequency of the OTA should be at least four times higher than the clock frequency of the $\Sigma$-$\Delta$ modulator [5]. High order $\Sigma$-$\Delta$ modulator is an alternative approach to modify the SNR. In case of more than 3rd order $\Sigma$-$\Delta$ modulator, however, its performance seriously suffers from nonidealities due to finite gain and bandwidth of the OTA, and instabilities caused by saturation of the integrator [6]. In this paper, we introduce the ASNR technique to the $\Sigma$-$\Delta$ modulator to provide stable varying SNRs.

The proposed $\Sigma$-$\Delta$ modulator is described in Fig. 4. The $SW_{1}$ determines the order of the $\Sigma$-$\Delta$ modulator between 2nd and 3rd while the $SW_{2}$ chooses its clock frequency. The combination of these switches allows the $\Sigma$-$\Delta$ modulator to obtain four different kinds of SNRs. Its control parameters are stored in the control register and a DSP analyzes and modifies them for easy and convenient control. By selecting proper parameters according to the input amplitude, the $\Sigma$-$\Delta$ modulator obtains optimal SNR from power and performance point of view [7].

Fig. 5 shows the detailed architecture of the $\Sigma$-$\Delta$ modulator. When the $/SW_{1}$ is closed, it operates in 2nd order by bypassing the output from the 2nd integrator to the OUTN or OUTP. Because the resistance value of the conventional N-type switch varies according to drain voltage, the 2nd integrator output degrades seriously when it passes through $/SW_{1}$. A high performance switch, whose resistance value is constant under all range of drain voltage, is necessary to prevent this distortion. However, the high performance switch is difficult to design and consumes additional power. Therefore we adopts the COMP1 which converts the 2nd integrator output into a PWM signal and passes it through the $/SW_{1}$ without signal distortion. When the COMP1 is activated, the 3rd integrator and COMP2 are totally turned off to eliminate extra power consumption. On the other hand, if the $/SW_{1}$ is opened, the 3rd integrator accepts the output of the 2nd integrator as an input and performs a 3rd-order modulation. In this case, the COMP1 is turned off to avoid extra power dissipation. By turning the $SW_{2}$ on and off, clock frequency is changed between 2.048-MHz and 1.024-MHz, respectively.

![Fig. 2 Characteristics of a microphone for a digital hearing aid](image1)

**Proposed analog front-end**

A. The preamplifier with combined-gain-control technique

![Fig. 3 Proposed preamplifier with CGC technique](image2)

![Fig. 4 Proposed Σ-Δ modulator exploiting adaptive SNR technique](image3)
By changing \(SW_1\) and \(SW_2\) separately, four configurations of \(\Sigma\Delta\) modulator, which have different kinds of SNRs, are obtained as summarized in a box of Fig. 5. With \(SW_1\) opens, type 1 and type 2 of the 2nd order \(\Sigma\Delta\) modulator are achieved by turning the \(SW_2\) off and on, respectively. With the closed \(SW_1\), type 3 and type 4 of the 3rd order \(\Sigma\Delta\) modulators are given by turning the \(SW_2\) off and on, respectively.

The low power OTA is designed to have a compensated two-stage, which has an input stage with cross-coupled active load and a class AB output stage [8]. It shows 77.6-dB DC gain, 7.07-MHz unity gain bandwidth, and 55° phase margin for a 3-pF load. The 1-bit quantizers such as COMP\(_1\) and COMP\(_2\) with a clocked circuit minimize the hysteresis to offer good reset [9].

The Fig.6 shows MATLAB simulation results of the proposed \(\Sigma\Delta\) modulator. Different kinds of SNR values can be generated according to the input amplitude.

**Experimental Results**

The chip microphotograph of the proposed analog front-end circuit is shown in Fig. 7. It was fabricated in a 0.25-\(\mu\)m CMOS technology and its core size is 0.5-mm\(^2\).

In Fig. 8, variations of the measured threshold gains and the threshold knee points of the preamplifier are presented as a function of the \(V_{VC}\) with the \(V_{TH}\) as a parameter. The threshold knee point is determined by different values of the \(V_{TH}\). By reducing \(V_{TH}\), knee point is decreased simultaneously. Moreover, the threshold gain of the preamplifier is determined according to the values of the \(V_{VC}\) and \(V_{TH}\). By using these parameters, an excessively high gain is prevented and the power dissipation is reduced. Measured attack and release response is shown in Fig. 9. The output signal is shown when the input voltage level suddenly drops by 25-dB. After a 0.1 sec delay, its output gain increases gradually according to the input level.

The Fig. 10 shows the plots of the measured SNR and SNDR versus the input amplitude. A measured output voltage spectrum is presented in Fig. 11. The proposed \(\Sigma\Delta\) modulator is type 1 with 2-KHz sinusoidal input signal and 1.024-MHz clock frequency. The measured peak SNR is 72-dB.
The measured performance of the proposed analog front-end is summarized in TABLE I. When the input amplitude is higher than 105-dB SPL, the Σ-Δ modulator acts as the type 1 and reduces power dissipation effectively. But if the input amplitude is lower than 90-dB SPL, it operates as the type 4 and offers high SNR. It allows an efficient usage of the limited energy of a zinc-air battery usually adopted in digital hearing aid [10]. The typical input referred noise of the complete analog front-end circuit is 3.8-μVrms.

The 2nd and 3rd order Σ-Δ modulator enhances the SNR by 9-dB and an 8-dB, respectively with the shift of clock frequency from 1.024-MHz to 2.048-MHz. The extra power dissipation due to frequency change is less than 1-μW in each type of the modulator.

Table 1: Performance Summary

<table>
<thead>
<tr>
<th>Supply Voltage</th>
<th>0.9-V</th>
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<tbody>
<tr>
<td>Order</td>
<td>2nd</td>
</tr>
<tr>
<td>Type1</td>
<td>1.024</td>
</tr>
<tr>
<td>Type2</td>
<td>2.048</td>
</tr>
<tr>
<td>Type3</td>
<td>2.048</td>
</tr>
<tr>
<td>Type4</td>
<td></td>
</tr>
<tr>
<td>Peak SNR</td>
<td>72-dB</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>26.4-μW</td>
</tr>
<tr>
<td>(Σ-Δ modulator)</td>
<td></td>
</tr>
<tr>
<td>-3dB bandwidth</td>
<td>8-kHz</td>
</tr>
<tr>
<td>Input referred noise</td>
<td>3.8-μVrms</td>
</tr>
<tr>
<td>Power dissipation</td>
<td></td>
</tr>
<tr>
<td>(Preamplifier)</td>
<td>Vcm=0.75, Vcm=0.8, Vcm=0.85</td>
</tr>
<tr>
<td>Total power dissipation</td>
<td>59.4-μW ~ 74.7-μW</td>
</tr>
<tr>
<td>(Analog front-end)</td>
<td></td>
</tr>
<tr>
<td>Technology</td>
<td>0.25-μm CMOS technology</td>
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</tbody>
</table>

The TABLE II compares the performance of the proposed analog front-end circuit with those of the previous works. The proposed analog front-end circuit dissipates the lowest power at the 0.9-V power supply voltage.

Table 2: Performance Comparison

<table>
<thead>
<tr>
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<tr>
<td>Supply Voltage</td>
<td>2.15-V</td>
<td>1.1-V</td>
<td>0.9-V</td>
</tr>
<tr>
<td>Peak SNR</td>
<td>77-dB</td>
<td>92-dB</td>
<td>86-dB</td>
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<td>Power consumption</td>
<td>323-μW</td>
<td>190-μW</td>
<td>59.4-μW</td>
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<td>CMOS Technology</td>
<td>0.8-μm</td>
<td>0.6-μm</td>
<td>0.25-μm</td>
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</table>

Conclusion

A novel low-power, energy-efficient analog front-end is proposed and implemented in a 0.25-μm CMOS process for a digital hearing aid chip. To reduce power dissipation and expand its dynamic range, the CGC and the ASNR technique are devised and adopted. The peak SNR is 86-dB and the input referred noise is 3.8-μVrms. The proposed analog front-end consumes a minimum power of 59.4-μW at 0.9V supply.

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References