A Real-Time Feedback Controlled Hearing Aid Chip with Reference Ear Model

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Abstract—A real-time hearing aid chip with the reference ear model (REM) and the comparison processor (COMP) is proposed and implemented. Through the COMP the response differences between the reference ear model and the impaired ear of the patient are achieved and processed to compensate the hearing loss of the patient. By adopting this architecture, the fully internal gain fitting and verification of the hearing aid with only single initial hearing loss test is implemented. To reduce the power dissipation and achieve the high flexibility, the preamplifier which has programmable multi threshold voltages is introduced. The feedback controlled hearing aid chip is implemented in 0.18 µm CMOS technology, consumes less than 110 µW and has a die size of 3.7 mm².

I. INTRODUCTION

Recently, the design paradigms of the biomedical devices get changed from the point of performance to the point of flexibility and user convenience [1, 2]. Especially the traditional hearing aid demands the innovation of design approach to satisfy the various user requirements [3]. The architecture of the conventional digital hearing aid is shown in Fig.1 (a). Because of the open loop gain fitting and verification method it is hard to optimize the performance of the hearing aid according to the each individual user [4]. In addition the only off-chip gain fitting and verification is possible. To enhance the performance optimization and the convenience level the hearing aid chip incorporates the human factors before the chip fabrication by using the pre fitting verification algorithm (PREVA) and the ear modeling circuit (EMC) in Fig.1 (b) [3]. In spite of its fast gain fitting, it still requires multi-external hearing loss test results because of open loop system. To achieve the user optimized design with single hearing loss test result and minimize the internal gain error for high accuracy the hearing aid system should include closed loop system for generating the DSP gain parameters. In addition, the advantages of the closed loop system are well known in control system applications through many articles and designs.

This work implements the hearing aid chip with reference ear model (REM) and the comparison processor (COMP) in Fig.1 (c). To achieve the fully internal gain fitting and verification without multi hearing loss test results, the fabricated chip adopts the closed loop control technique for gain verification. The generated parameter from the comparison of the response between the REM unit and the impaired ear compensates the hearing loss of the patient to the ideal reference ear.

II. SYSTEM OVERVIEW

Fig. 1 shows the fabricated hearing aid chip. It is composed of three major blocks: the REM unit, the COMP unit and the hearing aid (HA) unit.

The COMP enables the gain fitting and verification of the HA by using only internal parameters with the adoption of
the REM unit. The REM generates the ideal human ear response for comparing with the impaired ear response through the COMP. Due to its closed loop architecture the implemented chip requires only single hearing loss test response for initial parameter comparison.

III. BUILDING BLOCKS

A. Comparison processor with reference ear model

The design methodology of the proposed REM is shown in Fig.3 (a). The REM models the normal human external ear to achieve the natural resonance values of the ideal ear for compensating the hearing loss of the impaired ear. By adopting the 2-dimensional figure of the normal ear, the acoustic filter feature of the external ear is represented through the distributed LC filter. In this chip, the REM unit is designed to provide 30 taps and each tap has single L and C components. The 11 bit external control signal, SREM, is used to change the reference ear characteristics of the REM unit according to the different reference level by changing the value of the L or C. It modifies the property of the REM unit due to the various user requirements. Fig. 3 (b) shows the response of the REM unit compared with the natural response of the normal ear. Fig.4. presents the block diagram of the fabricated hearing aid chip with the COMP. Through the envelope detector, the peak gain values of the normal external ear from the REM responses are achieved as a function of frequency from 1 kHz to 8 kHz in steps of 1 kHz and digitized to 5 bit DSP parameters using low power SAADC. The introduced DSP gain parameter, PRem, from the REM unit are stored in the internal register and processed to choose proper resonance value. To reduce the design difficulty and the power consumption of the overall chip, the three frequency channels are selected among the eight channels from the 1 kHz to 8 kHz. Because of its enormous influence to the gain fitting and verification of the HA, the response of the REM unit at the 2 kHz is usually taken into account. The parameter value which has the largest amplitude among the outputs of the SAADC and the parameter value at the 2 kHz are decided to the compensation parameter (PRLT) for the REM in the HA.

For the initial DSP gain fitting of the HA, the 1st parameter computation of the proposed COMP is accomplished by using the parameters both from the single hearing loss test, PRLT, and the REM response, PRem. The values of the PRLT are compared with the PRem as a function of frequency. The differences between the two parameters are recognized by the parameter comparator, PC, and used to generate the new DSP parameter, PTR1, to compensate these differences through the parameter synchronizer, PS.

During the 2nd gain verification of the HA, the newly generated DSP parameter from the 1st parameter computation, PTR1, is compared with the parameter from the REM unit, PRem, again to achieve the parameter differences for determining the verified gain of the HA. The acquired parameter, PTR2, from the 2nd parameter computation achieves the fine gain compensation of the HA to reduce the gain difference between the normal ear and the impaired ear by the multi-internal iterations. The parameter computation through the COMP is continued until the parameter difference between the PRem and the PTRi is minimized enough to satisfy the specific reference value.

B. Low power programmable multi threshold preamplifier

Fig.5 shows the principle of the low power preamplifier with programmable multi threshold voltages. To imitate the ability of the normal human ear which covers the wide dynamic range, the conventional preamplifier adopts the high compression ratio. However the high compression ratio of the dynamic range causes a serious edge distortion at the conversation region. It requires an arduous and laborious training of a patient when he or she wears the hearing aid for the first time. To eliminate these problems and allow a wide linearity in the normal conversation range, the programmable multi threshold preamplifier is designed. It enables the same dynamic range between the normal and the impaired ear in the conversation region. In addition, the dynamic range of the impaired ear mapped to the conversation region can be changed according to the characteristics of the each individual user by controlling the two threshold voltages, VTH1 and VTH2. It enhances the articulation index and flexibility of the hearing aid.

Fig.6. shows the block diagram of the low power programmable multi threshold preamplifier. To reduce the
power dissipation, only two MOS-resistive circuit (MRC) units with the gain amplifier are used instead of the conventional three MRC units to implement the automatic gain control function and exponential gain control function at the same time. The voltage gain of the implemented multi threshold preamplifier is expressed in the form of (1) as

$$A_{\text{PRE}} = \frac{W_F L_F \left( 1 + \frac{V_{\text{DIFF}}}{V_{\text{COM}} - V_{\text{DIFF}}} \right)}{W_F L_F \left( 1 - \frac{V_{\text{DIFF}}}{V_{\text{COM}} + V_{\text{DIFF}}} \right)} = V_F = V_{\text{COM}} - V_{\text{DIFF}} \quad V_B = V_{\text{COM}} + V_{\text{DIFF}}$$

where $V_F$ and $V_B$ are negative and positive resistance control voltages respectively and $V_{\text{COM}}$ is a volume control voltage which determines the common mode level of $V_F$ and $V_B$. $V_{\text{DIFF}}$, the control voltage determined by the preamplifier output, decides the differential mode level of $V_F$ and $V_B$. $V_{\text{TH1}}$ and $V_{\text{TH2}}$ are threshold voltages and $W_F$, $W_B$ and $L_F$, $L_B$ are the widths and the lengths of the transistor $M_F$ and $M_B$ respectively.

When the input signal amplitude is smaller than $V_{\text{TH1}}$ or larger than $V_{\text{TH2}}$, the $V_{\text{DIFF}}$ value is selected as 0 and the $V_F$ and $V_B$ have the same value of $V_{\text{COM}}$. Therefore the voltage gain of the preamplifier is determined from the dimension of the MRC units and the value of the $V_{\text{COM}}$. If the input signal has an amplitude value between the $V_{\text{TH1}}$ and $V_{\text{TH2}}$, the $V_{\text{DIFF}}$ has different values to provide a various gain according to the each individual user. Moreover the threshold gain is changed with the variation of the $V_{\text{VC}}$ to solve the howling problem due to the positive feedback of the input sound. By using this architecture, the preamplifier reduces the power consumption to 33 $\mu$W and area occupation to 0.5 mm$^2$.

IV. IMPLEMENTATION RESULTS

The hearing aid chip with reference ear model has been fabricated in a 0.18 $\mu$m standard CMOS technology. Fig.7 presents a chip microphotograph of the hearing aid chip with comparison processor. The core area is 3.7 mm$^2$ and power consumption is less than 110 $\mu$W from a single 0.9V supply. Fig.8 plots the measured output of the programmable multi threshold preamplifier. The reported output dynamic range is from 0.45 V to 0.8 V. The overall operation of the comparison processor is shown in Fig.9. A hearing loss audiogram of a patient in Fig.9 (a) shows losses at 2 kHz and 4 kHz. In order to compensate such hearing losses, the compensation parameter is selected from the difference between the responses of the impaired ear and of the REM. By adopting this parameter overall gain of the hearing aid is compensation in slide Fig.9 (b). The slide Fig.9 (c) shows the final compensation results by the COMP with multi internal iterations. In this case, the preamplifier gain is selected as 1 to verify the performance of the COMP with REM. Compared with the conventional open loop hearing aid this system enables the fast and accurate on-chip gain fitting and verification by incorporating the fully internal feedback with single hearing loss test.

![Figure 5](image.png)  
**Figure 5.** Operations of the multi threshold preamplifier

![Figure 6](image.png)  
**Figure 6.** Block diagram of the multi threshold preamplifier

![Figure 7](image.png)  
**Figure 7.** Chip microphotograph

![Figure 8](image.png)  
**Figure 8.** Multi threshold preamplifier output
Fig. 9 shows the measurement results of the comparison processor. TABLE I represents the performance comparison with the other works related to the hearing aid chip. The main points in this table are design techniques based on internal verification and power dissipation. As a result, this work newly introduces the REM and the COMP with the lowest power consumption. The performance of the fabricated chip is summarized in TABLE II. The power consumption of the complete digital hearing aid chip is less than 110 $\mu$W from a single 0.9 V supply.

V. CONCLUSIONS

A real-time feedback controlled hearing aid chip with reference ear model is implemented using low power technique. The comparison processor (COMP) and the reference ear model (REM) are adopted to accomplish the fully internal gain fitting and verification with single hearing loss test. To compensate the hearing loss of the impaired ear, the response differences between the reference ear model and the impaired ear of the patient are processed to introduce the DSP parameters. Moreover, the programmable multi threshold preamplifier is designed to reduce the power compensation and achieve high flexibility. The closed loop hearing aid chip is fabricated in a 0.18 $\mu$m CMOS process and consumes less than 110 $\mu$W with a 0.9 V single supply.

REFERENCES