

Energy-Efficient Human Body Communication Receiver Chipset Using Wideband Signaling Scheme

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Abstract—This paper presents an energy-efficient wideband signaling receiver for communication channels using the human body as a data transmission medium. The wideband signaling scheme with the direct-coupled interface provides the energy-efficient transmission of multimedia data around the human body. The wideband signaling receiver incorporates with a receiver AFE exploiting wideband symmetric triggering technique and an all-digital CDR circuit with quadratic sampling technique. The AFE operates at 10-Mb/s data rate with input sensitivity of -27dBm and the operational bandwidth of 200-MHz. The CDR recovers clock and data of 2-Mb/s at a bit error rate of 10^{-7} . The receiver chipset consumes only 5-mW from a 1-V supply, thereby achieving the bit energy of 2.5-nJ/bit.

I. INTRODUCTION

Wearable or implantable biomedical devices can be widely utilized for health monitoring and wearable computing using body area connectivity [1]-[2]. In their applications, such devices, which have been worn around the human body and powered by a very small battery, require a low power receiver employing energy-efficient communication schemes. Moreover, the high data rate operation needs for receiving multimedia data such as audio or video using on-body networks. There are two candidates using a radio frequency (RF)-based communication for on-body networks: Bluetooth and ultra wideband (UWB). Bluetooth technology is not available for the transmission of multimedia data due to huge power consumption and insufficient data rate of 1-Mb/s. Even the Zero-G receiver [3] to achieve significant power savings over the Bluetooth radios consumes still too high power. Alternatively, the UWB receivers have been widely developed to achieve higher data rate operation, but must operate at vast bandwidth inherently leading to increase of power dissipation. For example, according to [4], an UWB receiver based on impulse radio was reported with the power consumption of about 30-mW at 3-to-5GHz bandwidth for wearable and wireless body area networks. In addition, it faces increasing cost for additional RF process, severe interference problem at very short range around the human body, and FCC regulation. To overcome the problems of such RF-based receivers for on-body networks, the novel communication method using a human body as a data transmission medium, called human body communication (HBC), was proposed in [2], [5]-[6]. The HBC receiver firstly

introduced in [5] integrates the tiny current with a single carrier frequency of 330-kHz and has limited data rate of 2.4-kb/s. The recently developed HBC receiver [6] requires a special electrooptic sensor to achieve 10-Mb/s data rate, and also it consumes too high power to apply for human body applications. In order to achieve lower power consumption with high data rate operation, the novel HBC scheme, wideband signaling (WBS), was proposed in [2]. This paper presents a receiver exploiting WBS technique that efficiently recovers binary data from the feeble wideband pulse signals. Realized in standard CMOS technologies, the receiver chipset exhibits overall power consumption of 5-mW from a 1-V supply, while delivering the data rate of 2-Mb/s. Accordingly, the proposed receiver is suitable for the application to energy-efficient transmission of multimedia data around the human body.

II. WIDEBAND SIGNALING RECEIVER

The HBC transmission is based on the WBS scheme that directly transmits binary digital signal through a transmitter into the human body, transfers wideband pulse signals over the HBC channel, and then recovers the binary data at the receiver. Fig. 1 shows the proposed WBS receiver, consisting of a receiver analog front-end (AFE), a clock and data recovery (CDR) circuit and an on-chip bit error detector. The receiver AFE amplifies, triggers, and inverts the received signal. The CDR circuit extracts a clean clock signal from the recovered binary data and latches the data. Fig. 2 illustrates the timing diagrams for the operation of the receiver exploiting wideband symmetric triggering (WST) technique. The channel output for the transmitted binary data is the narrow small pulse signal that comprises positive and negative pulses. The received pulse signal corrupted by the channel is sufficiently amplified for wide bandwidth, and subsequently, the signal is triggered to positive and negative states by using two symmetric thresholds, V_{TH} and V_{TL} , where the symmetric operation provides the duty cycle of 50%. Consequently, the binary data can be recovered by inverting the triggered signal.

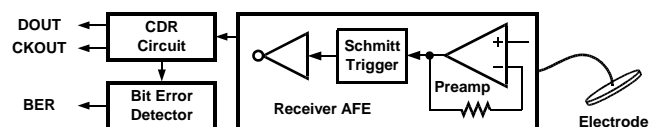


Fig. 1. Block diagram of the proposed wideband signaling receiver.

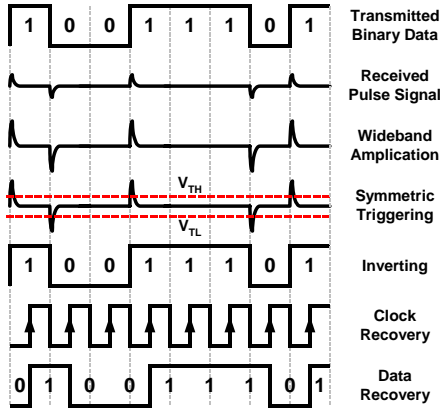


Fig. 2. Timing diagram for the WBS receiver operation.

III. RECEIVER AFE

A. Circuit Description

According to the investigation in [2], the input sensitivity of a receiver AFE needs to be less than 10-mV, which corresponding to -27dBm for the 50- Ω input impedance. In order to recover binary data from the narrow small pulse signals over the human body channel, the WBS receiver AFE in this work exploits WST technique. Fig. 3 shows the block diagram of the proposed receiver AFE consisting of four blocks: an on-chip bias circuit, a wideband preamplifier, a Schmitt trigger, and an inverting buffer. The AC coupling capacitor is connected to the input of the AFE. This capacitor eliminates the conductive current path to the body and provides DC biasing for the input of the preamplifier regardless of the body's potential. The capacitance of C_{IN} with the input impedance of the on-chip bias circuit determines low 3-dB frequency of the AFE. The on-chip bias circuit is designed as a complementary configuration to acquire symmetric impedance of 50- Ω and DC biasing with no external bias circuit. The wideband preamplifier is designed as a non-inverting amplifier where the op amp incorporates the low power wideband configuration. The high 3-dB frequency of the AFE is constrained by the 3-dB bandwidth of the preamplifier. Since the power spectrum of the received signal remains below 200-MHz, the preamplifier requires the 3-dB bandwidth of 200-MHz. the Schmitt trigger consisting of three resistors (R_3 - R_5) and the same op amp as that of the preamplifier produces positive and negative triggering thresholds (V_{TH} and V_{TL}), which can be controlled by varying the resistance of R_5 . With $R_4=R_3$, the sum of two triggering thresholds is equal to the supply voltage. Hence, the minimum input sensitivity of the receiver AFE (V_{RXSEN})_{min} is given by

$$(V_{RXSEN})_{\min} = \frac{V_{TH} - V_{DD} / 2}{A_v} = \frac{R_3}{2(R_3 + 2R_5)} \frac{V_{DD}}{A_v},$$

where V_{DD} is the supply voltage of the AFE and A_v is the voltage gain of the preamplifier, given as $1+R_2/R_1$. As the supply voltage decreases and the voltage gain of the preamplifier increases, the input sensitivity of the AFE can be

minimized. The wide bandwidth operation in the AFE leads to increase of power consumption. Decreasing supply voltage is very attractive to reduce the power consumption. But, the supply voltage, 1-V in this work, is lower than the sum of the threshold voltage of the NMOS and PMOS. This makes it difficult to design a low-voltage and wideband op amp. To alleviate this difficulty, the low-voltage fully complementary folded cascode topology is proposed in this work. Fig. 4 shows the circuit diagram of the proposed topology, consisting of an input stage with the source follower pairs, a gain stage employing fully complementary input pairs with low-voltage folded cascode loads, and a cross-coupled class-AB output stage. All configurations of the op amp are based on complementary structure for symmetric operation. The source follower input pairs need to obtain the sufficient overdrive voltage and to minimize the area overhead at the gain stage. The gain stage employs the fully complementary differential pair and the low-voltage folded cascode loads with each output can further reduce the number of the stacked transistors than the configuration with single output load. A class-AB output stage have been widely chosen to minimize quiescent power consumption leading to a fast operation with high slew rate. The cross-coupled type of the class-AB is adopted in accordance with the fully complementary gain stage. According to the simulations, the op amp exhibits 60-dB DC gain and the gain bandwidth product of 684-MHz while dissipating only 1.5-mA with a 1-V supply. With the help of the cross-coupled class-AB, its slew rate is 880-V/ μ s.

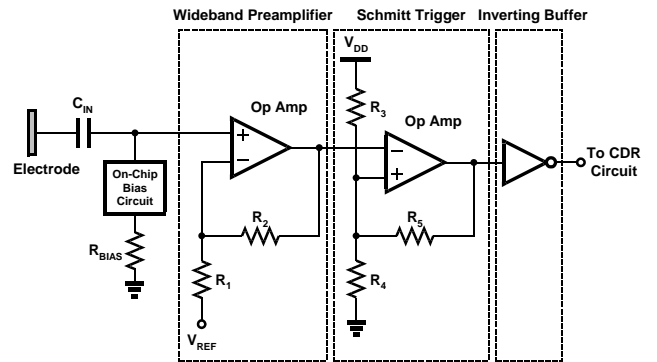


Fig. 3. Receiver AFE architecture.

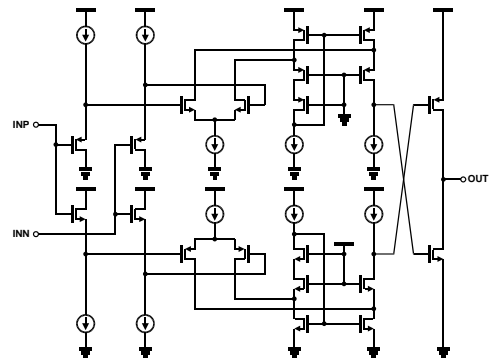


Fig. 4. Circuit diagram of the low power op amp.

B. Measurement Results

The proposed receiver AFE was fabricated with 0.18- μm standard CMOS technology, where the threshold voltage for NMOS and PMOS at saturation region are 0.58V/-0.58V, respectively. Fig. 5 shows the chip microphotograph. Its active area is about 0.04- mm^2 . The test chip was mounted on a FR-4 PC board by using chip-on-board. All measurements were conducted between the wrist and the fingertip that corresponds to the distance of about 25cm. Fig. 6 shows the measured timing diagram of the input and output signals of the AFE exploiting WST technique for 10-Mb/s 2^7 -1 PRBS transmitted data. The received input signal is measured to be about 50-mV amplitude. The preamplifier amplifies the received input signal with the voltage gain of about 30-dB before triggering at the following Schmitt trigger. The recovered output exhibits almost 50% duty cycle due to the symmetric operation. The measured 3-dB frequency spectrum of the AFE is in the range of 1-MHz to 200-MHz. The 0.18- μm CMOS receiver AFE dissipates 4.8-mW at a 1-V supply.

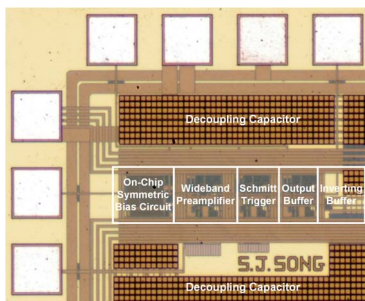


Fig. 5. Microphotograph of the AFE chip.



Fig. 6. Measured timing diagram of the AFE at 10-Mb/s.

IV. CDR CIRCUIT

A. Circuit Description

The WBS receiver employs a CDR circuit that is exploited in areas such as optical communications and high-speed serial links or interconnects. Since the receiver operates at relatively low data rates for the recovered binary data, it is more desirable for the CDR circuit to be focused on low power consumption rather than high speed operation. However, under the condition of $V_{\text{thn}} + |V_{\text{thp}}| > 1\text{-V}$, an analog

CDR circuit faces performance degradation. But, the power dissipation of digital circuitry is proportional to the square of the supply voltage. Therefore, the receiver incorporates all-digital sampling CDR architecture based on a low-voltage DCO. To further reduce power consumption and complexity, a quadratic sampling technique is adopted. The proposed CDR circuit takes all-digital PLL configuration as shown in Fig. 7. It consists of a quadratic sampling phase detector (QSPD), a lock-state controller, a 4-bit UP/DN counter, and a low-voltage DCO with voltage reference. The QSPD samples the incoming data at every rising edge of the clock and detects the transition of the data. The 4-bit FT signals can be generated by averaging and low-pass filtering the sampled values through the lock-state controller and the 4-bit UP/DN counter. When the LC signal goes high, the loop will be locked. The DCO controlled by FT[3:0] is designed to generate 16 multi-phase clock signals for quadratic sampling. In order to further reduce power consumption, the low-voltage DCO and the quadratic sampling technique are exploited. Fig. 8 shows the circuit diagram of a single delay stage of the low-voltage DCO with 8 delay stages. The PMOS differential input pair is used to achieve lower flicker noise and large input capacitance. The delay stage takes a fully differential structure based on the switched NMOS capacitor arrays that are digitally controlled by FT[3:0] for fine tuning. According to the simulations, the tuning range of the DCO shows 800-kHz with the tuning gain of 50-kHz/bit. The power consumption of the single delay stage is only 14- μW . Fig. 9 illustrates the proposed quadratic sampling algorithm and the characteristic curve of the QSPD. The QSPD generates the 3-bit UP, LC, and 3-bit DN signals that are produced by XORing two consecutive bits of the DIN signal with the quadratic interval window. All of them are converted to 4-bit 2's complement values before weighting and averaging functions. To avoid potential loop instability, the averaged values is low-pass filtered by a simple digital filter. Then, the low-pass filtered values are used to generate the UDN and CCK signals. Based on this algorithm, the QSPD provides the quadratic gain over a bit interval window as shown in Fig. 9. With the help of the quadratic gain characteristics, the number of sampling clock signals can be reduced by a factor of two. Therefore, it can further reduce power consumption and the area overhead.

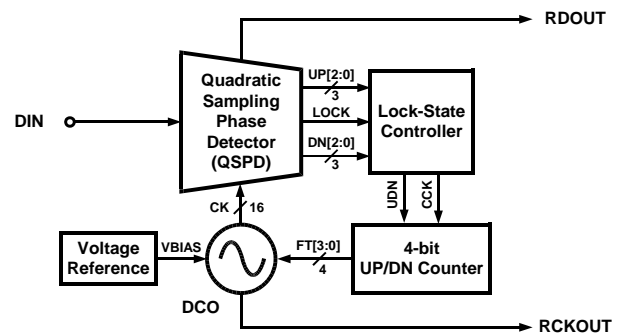


Fig. 7. All-digital CDR Architecture.

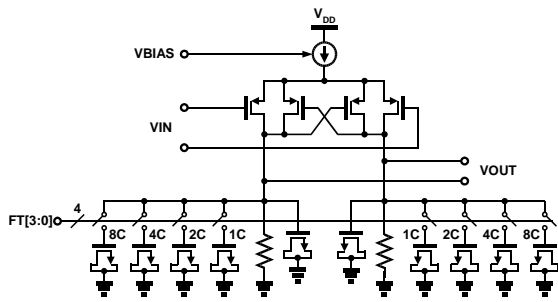


Fig. 8. Circuit diagram of the single delay stage in the low-voltage DCO.

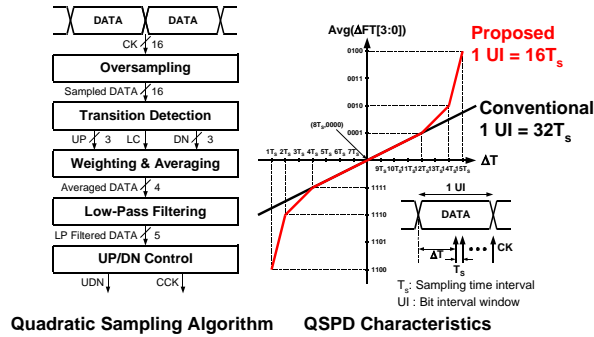


Fig. 9. Quadratic sampling CDR technique.

B. Measurement Results

The proposed CDR circuit is fabricated with a 0.25- μm standard 1P4M CMOS technology, where the threshold voltage for NMOS and PMOS at saturation region are 0.6V and -0.65V, respectively. Fig. 10 shows the microphotograph of the test chip, including the CDR circuit and the bit error detector. Its core area is about 0.2- mm^2 . Fig. 11 shows the measured waveforms of the recovered clock and data of the CDR circuit for 2-Mb/s 2^7 -1 PRBS data, respectively. The recovered clock jitter is measured to be 1.6ns rms. The bit error rate is estimated to be less than 10^{-7} by the on-chip bit error detector by counting error bits for 2^7 -1 PRBS data. The CDR circuit consumes a power of 0.15-mW at 1-V supply. The measured receiver input power as a function of the communication distance from the fingertip to the ear for 2-Mb/s 2^7 -1 PRBS data is shown in Fig. 12, indicating that the receiver input power rapidly decreases to the minimum input sensitivity of -27dBm. The receiver chipset including the AFE consumes the total power of 5-mW from a 1-V supply.

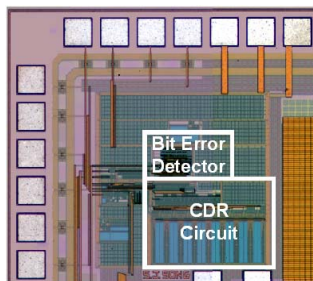


Fig. 10. Microphotograph of the CDR chip.

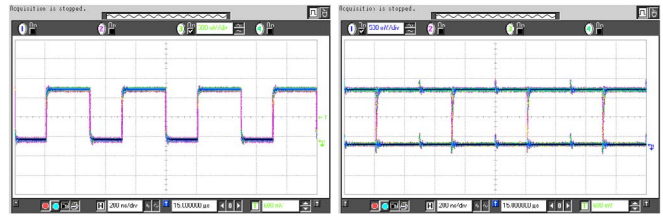


Fig. 11. Measured waveforms of the recovered clock and data at 2-Mb/s.

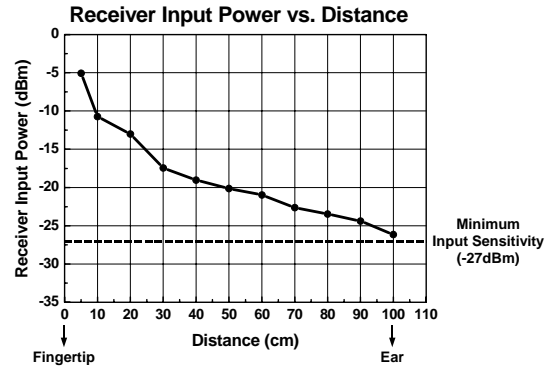


Fig. 12. Measured receiver input power as a function of distance.

V. CONCLUSION

In this paper, an energy-efficient wideband signaling receiver chipset is presented for the human body as a data transmission medium. A receiver AFE exploiting wideband symmetric triggering technique and all-digital CDR circuit are included into the chipset. To reduce power consumption along with wide bandwidth operation, the transceiver incorporates a number of low power techniques such as low-voltage fully complementary folded cascode op amp topology, all-digital CDR architecture, low voltage DCO, and quadratic sampling CDR technique. The transceiver operates at 2-Mb/s data rate with the input sensitivity of -27-dBm at a bit error rate of 10^{-7} . The total power consumption of the chipset comes to only 5-mW from a 1-V supply.

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