An Autonomous SRAM with On-Chip Sensors in an 80nm Double Stacked Cell Technology

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Abstract

An active solution to overcome the uncertainty and fluctuation in nano technology SRAM is introduced. It automatically adapts SRAM's operation optimized for the process variation and operating environments by using on-chip timer, temperature sensor, substrate noise manager and leakage current monitor. A test SRAM chip fabricated with an 80nm SRAM process, shows that average power consumption is reduced by 9%, and the standard deviation decreases by 58%.

Keywords: SRAM, on-chip timer, temperature sensor, substrate noise, leakage current monitor

Introduction

Recently, SRAM is reported to face severe problems which are density limitation, leakage current, static noise margin of cell, and SER, etc [1]. S^3 (Stacked Single-crystal Si) SRAM cell technology was developed to solve the density problem [2]. Its cell size is only $0.16um^2$, 2.9 times of DRAM cell size in the same technology. However, as the density of SRAM becomes higher, leakage current and device parameter fluctuation become more significant. Careful and detailed control of the device features is necessary and more precise data on the conditions under which the device operates are required. In this paper, sensing, analysis and control (SAC) scheme is introduced for the close monitoring and controlling of the device operations in consideration of chip-to-chip difference and operating environments.

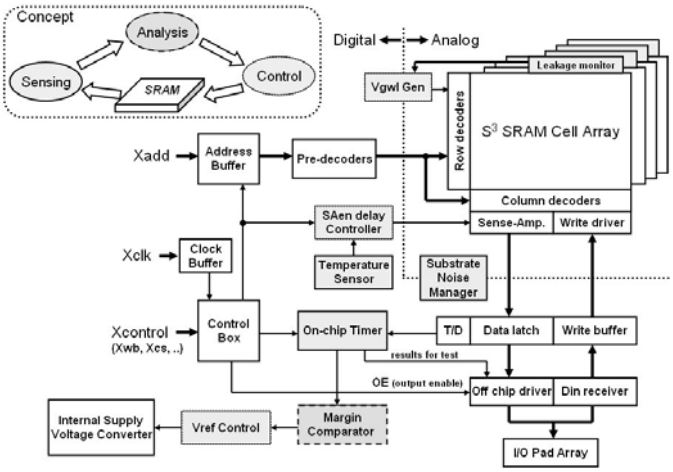

Fig. 1 Block Diagram of the Proposed SRAM

Fig. 1 shows the block diagram of the proposed SRAM. In addition to the conventional SRAM circuits, measurement blocks, diagnostic blocks, and controller blocks are added as described as gray blocks in Fig.1.

Process, voltage, and temperature variations can cause uncertainties like speed degradation and high power consumption including leakage current of SRAM. In this paper, an active approach is introduced to tackle these uncertainties by incorporating multiple sensors on a chip. An on-chip timer is integrated for the diagnosis of speed degradation. And the on-chip timer and a temperature sensor are used for power optimization. A substrate noise manager and a leakage current monitor control substrate noise and leakage current, respectively. Table. 1 shows the summary of the SAC scheme in the proposed SRAM.

Table. 1 The Summary of the SAC scheme

Sensors	Detect and Analysis	Control	Effect
On-chip timer	> Preset margin for stable read op.	Internal supply voltage	Low power & stable operation
Temperature sensor	< 50°C or >100°C	SAen delay	Wide margin
Substrate noise detector	> Preset noise level (V_{p-p}=150mV @20MHz)	Active decoupling	Silent substrate for sense amplifiers
Leakage current monitor	> Preset value (1uA per cell block)	Negative wordline	Low power

Building Blocks

A. On-Chip Timer

Although lowering supply voltage is a very effective way to reduce power consumption, it can cause problems in the cycle time and static noise margin of the SRAM cell. The on-chip timer of Fig. 2 is adopted to check the cycle time margin.

Small-size SRAM cell like S^3 SRAM cell is difficult to generate enough cell current for bitline swing so that read cycle becomes the limitation of the cycle-time. The on-chip timer measures two kinds of delays: from clock rising edge to data transition in data latches, and from the data transition to the next clock rising edge. The former is for checking the internal delay of the read cycle for known good die (KGD) test at wafer level. The latter is for measuring read cycle time margin.

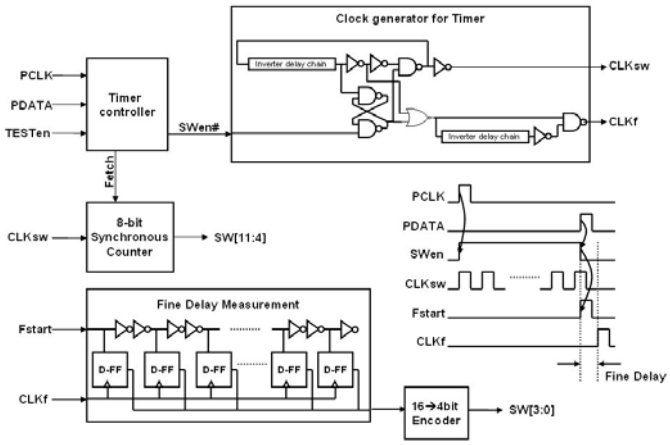

Fig. 2 On-chip Timer

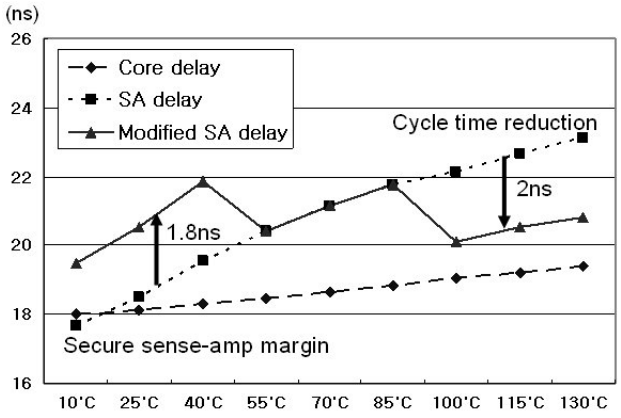

Fig. 3 Core Delay VS Sense-Amp Delay VS Modified SA Delay

The switching between the two operation modes can be set by the test mode selection. PCLK is the rising edge of the external clock and PDATA is the output signal of the transition detector (T/D) of the data latch. The clock generator is triggered by SWen# to generate CLKsw and CLKf. The CLKsw is fed to 8-bit synchronous counter where the higher bits of the timer (SW[11:4]) are output.

In the fine delay measurement block, the delay from the falling edge of SWen# to the rising edge of CLKf is measured and encoded to 4 bit digit (SW[3:0]). As shown in Fig. 2, the unit of the measurement is two inverter-delays of a typical-size MOSFET. To measure delays in real time unit in testing, another test mode is implemented in order to measure the delay from clock to next clock. In case of normal operation, the number of two inverter delays, about 0.2ns at 1.6V, is enough to represent cycle time margin.

According to the values of the on-chip timer, the internal supply voltage level is controlled for low-power consumption and stable operation. When enough margins exist, internal supply voltage is dropped until it reaches the pre-defined voltage determined by data retention voltage of SRAM cell, which is about 0.8V. In addition, the internal voltage is lowered as long as the value of on-chip timer has an operation margin. On the contrary, when the cycle time margin is insufficient, the internal supply voltage is raised for more stable operation.

B. Temperature Sensor

One important factor which affects read cycle time is the sense-amplifier-enable delay (SAen delay) which means an enforced delay from wordline-rising edge to sense-amplifier-enable time. In general, SRAM has an option to modify this delay because the performance of the cell and the core circuit can not be known before fabrication and the final tuning is necessary according to the measured value. Proposed SRAM can adjust the SAen delay with 8 steps. Each step has about 2ns delay. Commonly, the delay circuit for the SAen generation uses relatively large length transistors in order to make long delay and it suffers from the voltage and temperature variations. Especially, the temperature has different effects on core delay and SAen delay.

Core delay means the delay from wordline rising edge to when bitline pair develops enough voltage difference, about 50mV. Core delay is composed of decoding delay and bitline-evaluation time by cell current.

Fig. 3 shows the temperature variation of the core delay, SAen delay and modified SAen delay. This is controlled by the output signals, T50 and T100, of the temperature sensor as shown in Fig. 4. The temperature sensor generates signals T50 and T100 which mean the boundary of 50°C and 100°C, respectively.

For the consideration of process variation, the values of R1 and R2 can be changed by test signals and fixed by fuse. According to the T50 and T100, the SAen delay is adjusted by 1 step. If the temperature is higher than 100°C, SAen delay is reduced to give the SRAM more cycle-time margin. This enables to lower internal supply voltage resulting in low-power consumption. On the contrary, if it is lower than 50°C, SAen delay is increased by 1 step to stabilize the read operation.

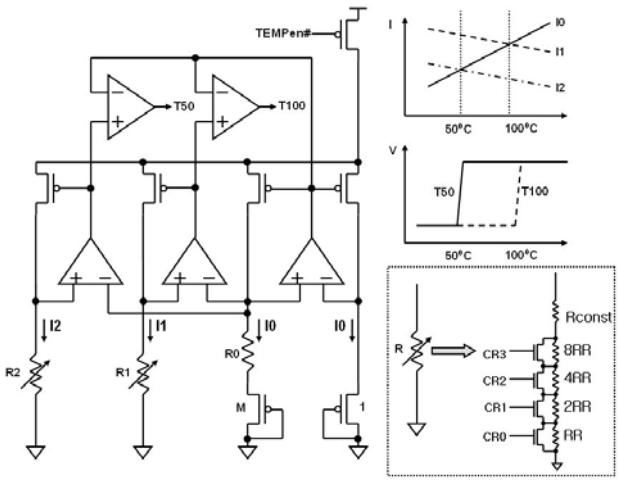

Fig. 4 The Schematic of Temperature Sensor

C. Substrate Noise Manager (SNM)

Recently, the effects of the substrate noise from digital circuits to analog circuits have been studied [3]. Fig. 5 shows the schematic diagram of the substrate noise manager (SNM). It is composed of substrate noise detector (SND) and substrate noise suppressor (SNS). The SND integrates substrate noise in pre-determined period, and asserts the signal NOISY when the integration level (VC5) is under the logic threshold voltage of the inverter V1. Sensitivity of the SND can be controlled by the resistor R5 and the period of signal PRECH#. By controlling substrate noise, the operation of the analog circuits like sense amplifier can be stabilized and it can have shorter SAen delay.

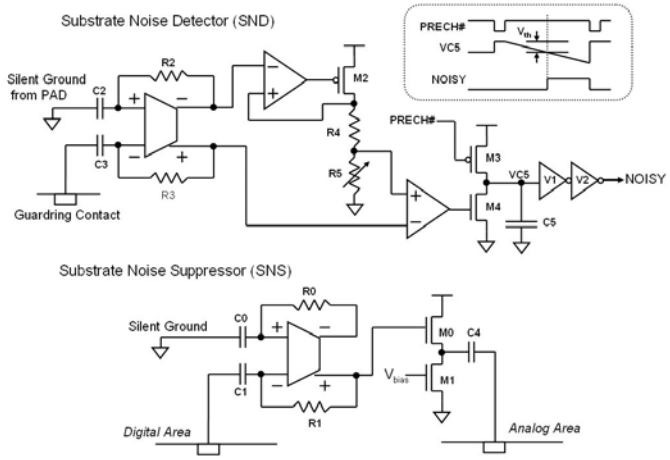

Fig. 5 Substrate Noise Manager (SNM)

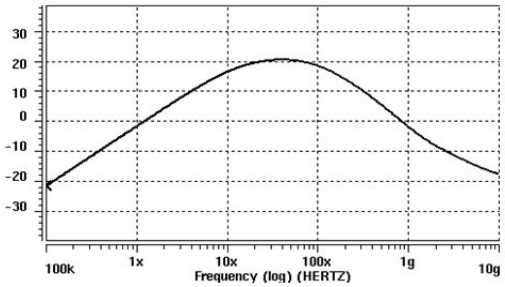

Fig. 6 Frequency Response of Substrate Noise Suppressor

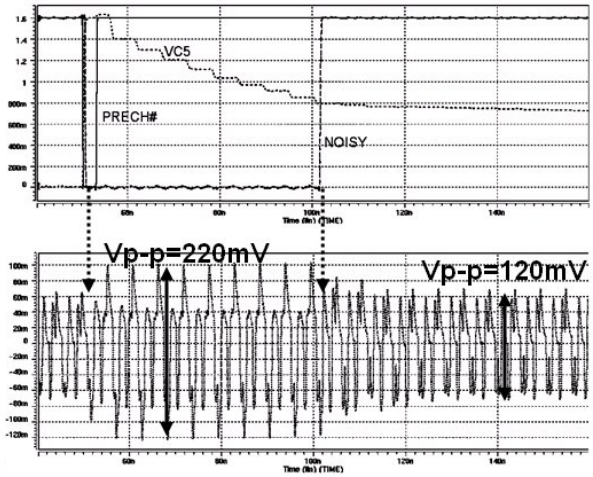

Fig. 7 Simulation Results of Substrate Noise Manager

SRAM can secure more cycle-time margin and lower operating-supply-voltage as well. Fig. 6 shows the frequency response of the SNS. It has 20dB gain and 820MHz gain band width. Low frequency less than 1 MHz is cut off by the capacitors C0 and C1. The SNS suppresses effectively the substrate noise from 10MHz to 500MHz which covers the range of the operating frequency and its harmonics.

Fig. 7 shows the simulation results of SNM. Peak to peak voltage of the substrate noise can decrease about 40%.

D. Leakage Current Monitor (LCM)

Fig. 8 shows the leakage current monitor. In test mode or standby mode, the M4 is turned off to cut off the current path from the main regulator M1. The current of each cell array block is supplied through the M2 in the leakage current monitor. Leakage current I1 is replicated by the M3, converted to the voltage Vsen and compared with Vlkg. When the Vsen is higher than the Vlkg, LKG0 is turned on and is used for controlling the Vgwl generator of Fig. 1. The source and bulk voltage of the pull-down transistor of final row decoders are made to negative voltage by the Vgwl generator. And the low level of wordline falls down to about -0.3V. This reduces leakage current from a bitline precharge transistor to a pull-down transistor through a pass transistor of the SRAM cell.

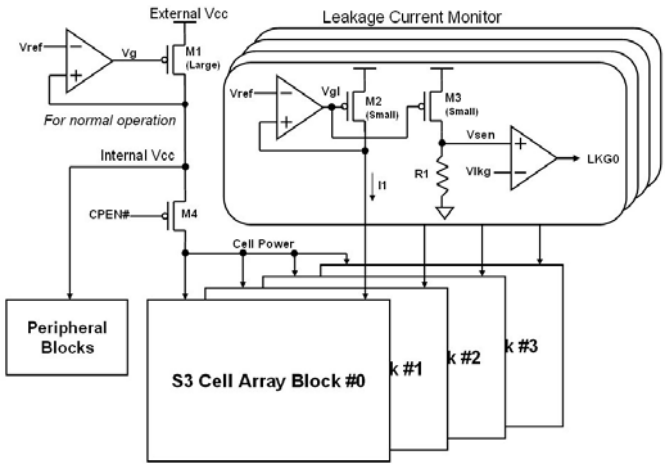

Fig. 8 Leakage Current Monitor (LCM)

Implementation and Testing

Fig. 9 shows 512kb test SRAM chip in an 80nm double stacked S^3 SRAM cell technology with 3.3V external and 1.6V internal supply voltage. The chip area is 1,152um x 1,728um.

Fig. 10 shows the test results of the proposed SRAM with and without SAC at room temperature. 40 samples from different wafers and lots were tested. The average power consumption is reduced by 9% from 15.9mW to 14.4mW. Maximum power consumption is also reduced by 17% from 20.5mW to 17.1mW. More importantly, the standard deviation of power consumption is reduced by 58% from 2.6 to 1.1. From these results, it is clear that the implemented SRAM reduces not only power but also chip-to-chip variation by using the proposed SAC scheme.

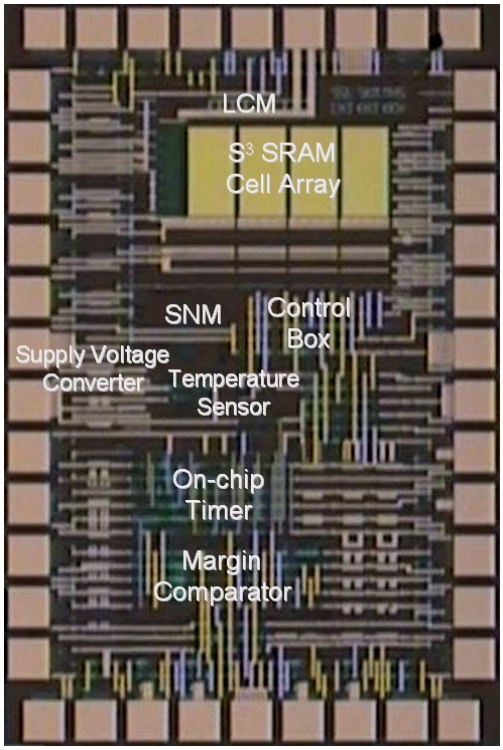

Fig. 9 Test Chip Photo

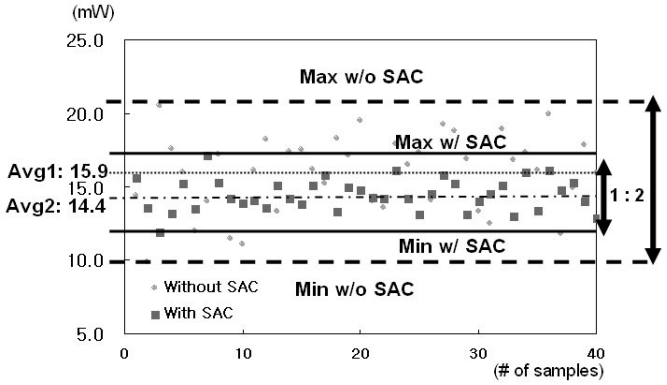

Fig. 10 Measured Power Consumption Without and With SAC

Fig. 11 shows the cycle time shmoo according to a preset read timing margin. The smaller the preset read timing margin becomes, the larger a maximum operation frequency becomes. If the preset margin is set to 100000, the maximum operation frequency is 20.8Mhz. In case of 001000, the maximum operation frequency is changed to 23.2MHz. And, at the same cycle time, if the read timing margin is set to a small value, power consumption is also decreased by lowering internal supply voltage. But, in an extreme case, read operation can not be performed normally. So, determining proper read timing margin is very important and initial tests must be executed in many times.

All components of SAC scheme are made to be turned on and off independently. The effect on the power consumption is the biggest when the on-chip timer is used. Each component can increase or decrease power consumption. Increasing case happens when stable operation is considered first.

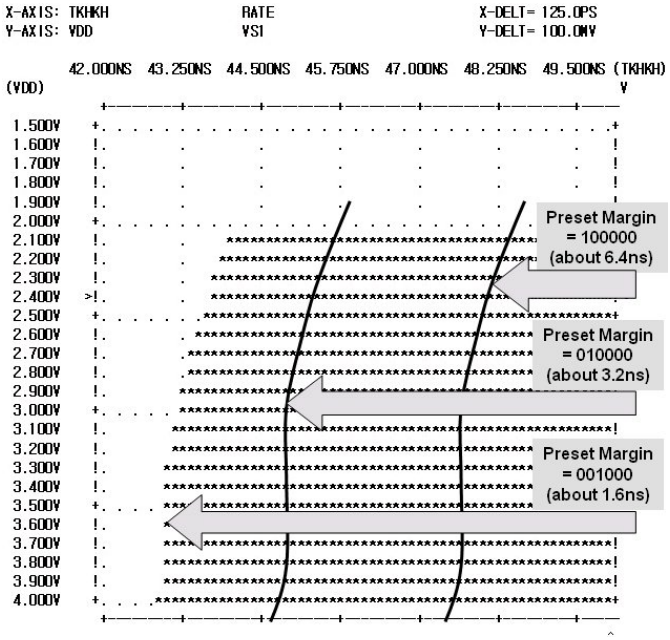

Fig. 11 Cycle Time Shmoo according to the Preset Timing Margin

The power consumption overhead of the SAC scheme is under 8% at test chip. In high-density SRAM product, the overhead of SAC scheme is estimated to be less than 1% of overall power consumption.

Summary

A novel sensing and controlling method for SRAM is proposed and implemented in an 80nm S^3 cell technology to overcome uncertainties. Various blocks like on-chip timer, substrate noise detector, temperature sensor and leakage current monitor are used for sensing internal condition of SRAM. According to the sensed data, internal supply voltage, sense-amplifier margin and substrate noise of SRAM are controlled. By using this SAC scheme, the average power consumption is reduced by 9% from 15.9mW to 14.4mW, and the standard deviation of the power decreases by 58% from 2.6 to 1.1.

References

[1] A. Kotabe, et.al., "A 0.13-um, 0.78-um2 Low-Power Four-Transistor SRAM Cell with a Vertically Stacked Poly-Silicon MOS and a Dual-Word-Voltage Scheme," *Dig. Symp. VLSI Circuits*, pp. 60-63, June 2004.

[2] S. Jung, et.al., "The Revolutionary and Truly 3-Dimensional 25F^2 SRAM Technology with the smallest S^3 (Stacked Single-crystal Si) Cell, 0.16um^2, and SSTFT (Stacked Single-crystal Thin Film Transistor) for Ultra High Density SRAM," *Dig. Symp. VLSI Technology*, pp. 228-229, June 2004.

[3] K. Makie-Fukuda, T. Tsukada, "On-chip active guard band filters to suppress substrate-coupling noise in analog and digital mixed-signal integrated circuits," *Dig. Symp. VLSI Circuits*, pp. 57-60, June 1999.