Networks-on-chip and Networks-in-Package for High-Performance SoC Platforms

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Abstract—A structured packet-switched Networks-on-Chip (NoC) is designed and implemented for high-performance heterogeneous SoC design platform. The chip integrates multiprocessors, multiple memories, and other heterogeneous Intellectual Properties and interconnection with 51mW and 1.6GHz on-chip networks. The NoC adopts a partial activated crossbar, low-energy coding, and low-swing signaling for the power consumption optimization. A Network-in-Package integrating four NoCs is fabricated in a 676-BGA-type package for larger and scalable systems and demonstrates 2D-image-processing and 3D-graphics applications.

I. INTRODUCTION

On-chip wire delays have become more critical than gate delays and recently synchronization problems between Intellectual Properties (IPs) are more apparent. This trend only worsens as the clock frequencies increase and the feature sizes decrease. Moreover the interconnections, including clock distribution over the whole chip area, are readily influenced by process uncertainty or physical disturbance. In this context, the performance of SoCs will be limited by the ability to efficiently interconnect predefined and pre-verified IPs and to accommodate their communication requirements, i.e. it will be communication – rather than computation – dominated. Moreover the power consumption on communications becomes significant portion of overall system power budget.

Recently, Networks-on-Chip (NoC) architectures are emerging as a scalable, reliable, and highly modular on-chip communication infrastructure [1], [2], [3]. The NoC architecture uses layered protocols and packet-switched networks which consist of on-chip routers, links, and network interfaces on a predefined topology, as depicted in Fig. 1. Instead of interconnecting processing modules at the top-level using an ad-hoc routing of dedicated global wires, as is done today, a better approach is to interconnect them by a structured on-chip packet switching network that routes packets between IPs. The advantage of using a NoC platform includes both modularity and performance benefits. There have been lots of architectural and theoretical studies on NoCs such as design methodology, topology exploration [1], QoS guarantee, reliable transmission, and software issues. Only a few were implemented and verified on the silicon but they were not energy-efficient [2]. For large scale NoC implementations, the power consumption on the network infrastructure should be minimized in order for reliable transmission of data with low-cost.

In this work, we designed and implemented a hierarchically star-connected NoC with various low-power techniques. The chip [3] contains heterogeneous IPs such as two RISC processors, multiple memory arrays, FPGA, off-chip network interfaces, and 1.4GHz PLL. The integrated on-chip network provides 89.6-Gb/s aggregate bandwidth and consumes less than 51mW at full traffic condition. In the other hand, the previous work [2] consumes 264mW with 51-Gb/s bandwidth. The ratio of power consumption to providing bandwidth of this work is reduced by ten times from the previous work. This design will present and verify the proposed various low-power techniques for on-chip networks.

Large scale SoCs with huge chip size such as embedded memory logic systems often suffer from their low yield and high cost problems. The NoCs have so modular structure that large system can be divided into several parts or several chips to mitigate such problems. In this work, four NoCs are mounted on a single package for larger system emulation to form a Networks-in-Package (NiP). The chip-to-chip interconnections in a package exploit low resistive LC printed wires for low-latency and low-jitter off-chip communications [6].

II. NOC ARCHITECTURE AND CIRCUITS

For the design of Networks-on-Chip, there are lots of things to be decided such as a communication protocol, a network topology, a switching style, buffer-depth (in router), a clock synchronization method, a signaling scheme and so on. In this section, a brief summary about what is decided and why such decisions are made at each design-stage will be presented based on an important basic idea, low-power consumption.

A. Hierarchical Star Topology

The first phase for NoC architecture design is choosing the most suitable NoC topology. In this work, we compared the most widely used topologies such as bus, star, mesh and hierarchical star (H-star) topologies based on the power consumption, which is our main concern. According to an analytical calculation shown in Fig. 2, Mesh and H-star topologies show the lowest power consumption under not only uniform traffic but also localized traffic D

Figure 1. Networks-on-Chip and Networks-in-Package architecture
condition. We chose the H-star topology for our NoC platform because it has more flexible structure and less switching hops than Mesh topology does.

![Figure 2. Power analysis of various topologies](image)

**B. No global clock synchronization**

A state-of-the-art SoC is a heterogeneous multi-processing system, with multiple timing references, because of the difficulty of global synchronization as well as Processing Unit (PU) independent clock frequency scaling. To cope with multiple clock domains, in this implementation, each processing unit operates with its own clock, CLKPU, but it communicates with a unique clock, CLKNET. Network Interface (NI) changes the timing reference from the CLKPU to the CLKNET and vice versa. The CLKNET is not synchronized over the chip so that the communications become mesochronous condition—same frequency but different skew. For the mesochronous communications, we use a source-synchronous scheme where strobe signal goes along with the packet data. The strobe signal is used as timing reference to latch the packet data at the receiver end.

A proposed NoC protocol supports burst transactions and 2-level of Class-of-Service. A packet consisting of 16bit header, 32bit address and 32bit data fields is serialized into 8bits channel to reduce the network area and power consumption.

**C. Low-Power Techniques**

In this implementation, various low-power techniques are proposed in physical layer, network layer, and transport layer.

1) **Low-swing signaling on global links**

The global link connecting switches are usually several millimeters long. Therefore, it suffers from its longer latency and higher power consumption than a local link does, making cross-chip communication increasingly expensive. Low-swing signaling can alleviate the energy consumption significantly and overdriving signaling improves its delay.

Fig. 3(a) shows the implemented differential low-swing signaling. Global wires are laid out in zigzags to emulate a long link as long as 5.2mm without repeaters. To find out the optimum signaling. Global wires are laid out in zigzags to emulate a long link VSWING. Fig. 3(c) shows energy and delay product. The delay from a power consumption on a transmitter and a receiver according to the capacitance and resistance wire model [3]. Fig. 3(b) shows the signaling improves its delay.

2) **Crossbar Partial Activation Technique [3]**

Crossbar is widely used in the router as the switching fabric. We proposed the Crossbar Partial Activation Technique to reduce the power consumption on the crossbar. The technique removes unnecessary activation by using tri-state buffers and multiplexers. As a result, 22% power saving is obtained on 8x8 crossbar.

3) **Low-Energy Coding on On-chip Serial Link [4]**

On-chip source-synchronous serial communication has many advantages over multi-bit parallel communication in the aspects of skew, crosstalk, area cost, wiring difficulty, and clock synchronization. However, the serial wire tends to dissipate more energy than parallel bus due to the bit multiplexing. In this work, we proposed a novel coding method, SiLENT, to reduce the transmission energy of the serial communication by minimizing the number of transitions on the serial wire. The coding method saves significant amount of the communication energy for multimedia applications. It reduces maximum 77% of energy for instruction memory access, and 40–50% of energy for data memory access in a 3D graphics application.

4) **Operating Frequency Scaling**

PLL generates internal clocks such as a 100MHz clock for main cluster PUs, a 50MHz clock for peripheral cluster units, and a 1.6GHz network clock for switches and network interfaces. The clock frequencies are scalable for power management modes, i.e. 100/50/1600MHz for FAST mode, 50/25/800MHz for NORMAL mode, and 25/12.5/400MHz for SLOW mode.

**III. CHIP IMPLEMENTATION**

**A. Design Flow and Methodology**

The Network-on-chip was designed by semi-custom method. Integrated processors are synthesized, memories are compiled by SRAM compiler, and the on-chip networks are full-custom designed for low-power and high-performance. Processors and memories are obtained from vendors and reused by attaching the network interface and wrappers. Fig. 4 shows the design flow; EDA tools, design stage, and the output deliverables at each stage. It took 6-months from architecture sketch to tape-out with 7 engineers.
The chip integrates two clusters; a main cluster and a peripheral cluster. The main cluster contains two RISC processors, on-chip FPGA, two 64kb SRAM, and an off-chip gateway. Two RISC processors emulate multiprocessor systems. Off-chip gateway (OGW) [2] enables seamless off-chip communications with other NoCs on the same package or boards in order to compose larger scale systems. By using the OGW, a PU on a die can communicate other PUs on the other dies without protocol conversion. The peripheral cluster contains three memories to emulate peripheral circuits. By using the OGW, a PU on a die can communicate other PUs on the other dies without protocol conversion. The peripheral cluster contains three memories to emulate peripheral circuits. The two clusters are interconnected via 5mm global link clocks for PUs and networks. PU clocks are not synchronized each other for the emulation of systems with multiple timing references. Therefore no effort is needed for clock skew minimization. The on-chip network supports 3.2GB/s communication bandwidth for each PU and 11.2GB/s aggregate bandwidth at FAST mode. The chip is implemented using 0.18µm CMOS process with 6-Al metal layers and its die area takes 5x5mm². Fig. 6 shows the die photograph. The on-chip network power dissipates 51mW at FAST mode with full traffic condition. The right figure shows the power break-down and the effectiveness of the proposed low-power techniques. By using the proposed techniques such as low-swing signaling, crossbar-partial activation, and serial-link coding, the overall power consumption is reduced by 43%.

IV. NETWORKS-IN-PACKAGE

Four NoCs are mounted on a single 676-BGA package as shown in Fig 7(c), (d). The Network-in-Package (NiP) needs four isolated supply voltages: 1.8V for digital logic, 1.8V for analog circuits, 3.3V for I/O, and sub-0.5V for low-swing links. The operating frequencies are different for each module: 50MHz for peripheral logic, 100MHz for processors, 800MHz for scheduler, and 1.6GHz for on-chip networks.

The important issue for the package design is the power integrity, i.e. a design of power and ground (P/G) network. No significant resonance should occur on the P/G plane of the package at the operating frequency. Otherwise small noise from signals or external system causes so significant P/G noise that P/G network becomes unstable. In order to analyze the power integrity, we used Transmission Line Matrix (TLM) Method and Simultaneous Switching Noise (SSN) analysis. (See Fig. 7(a), (b)) We integrated decoupling-capacitors for each power voltage at the proper position: 5 for logic power, 2 for I/O power, 1 for analog power. Each capacitor has 10nF capacitance and 600pH Effective Series Inductance properties. Fig. 7(a) shows the self-impedance of the power plane. We targeted the self-impedance of the power plane as 1Ω. The solid-line is for bare P/G plane and the dotted line is for the proposed decouple-capacitors-insertion. The impedance of the P/G plane shows inductance-characteristics and exceeds the target
impedance at 800MHz and 1.6GHz. After the decoupling-capacitance-insertion, the impedance resonance occurs at 272.1MHz that comes from the L of bare plane and C of the inserted-capacitors. As a result, the self-impedance at the target frequency becomes lower than 1Ω.

V. MEASUREMENTS & DEMONSTRATION SYSTEM

A. Measurement Results

The implemented chip is successfully measured. Fig. 8(a) shows the measured packet signals on the network at FAST mode, and Fig. 8(b) shows the measured packets with and without the proposed SiLENT coding, respectively, while a 3D graphics application is running on the system [5]. Transitions on a channel are reduced from 134 to 79 after the coding.

B. Demonstration System

We developed a demonstration system with the implemented Networks-in-Package for multimedia applications. Fig. 9 shows the demonstration system which consists of NiP-board on top, video board on bottom layer, LCD module. The system demonstrates image processing and animation processing on the display through networks on the chip and networks in the package. The Fig. 9 shows packet transactions between two NoCs on the NiP where the two NoCs are running at different clock frequencies, e.g. 400MHz and 274MHz.

VI. CONCLUSION

A low-power packet-switched Networks-on-Chip (NoC) and Networks-in-Package (NiP) with hierarchical star topology is designed and implemented for high-performance SoC platform. The chip contains two RISC processors for multiprocessor emulation, two 64kb SRAMs, on-chip FPGA, off-chip gateway for off-chip network interface, three 4kb SRAM for peripheral logic emulation, 1.6GHz PLL for internal clock generation, and on-chip networks connecting those processing units. On-chip network channel is serialized from 80bits onto 8bits to reduce the network area significantly. Source-synchronous signaling enables plesiochronous communications between processing units running at different clock frequencies. Low-power consumption is achieved by applying various techniques such as a lower swing signaling link, crossbar partial activation, low-energy serial-link coding, and clock frequency scaling. The chip integrates 2.5 million transistors and consumes less than 160mW and the on-chip network consumes less than 51mW delivering 11.2GB/s aggregated network bandwidth. The 5x5mm² chip is fabricated with 0.18µm CMOS process and successfully measured and demonstrated on a Network-in-Package system evaluation board running real-time multimedia applications.

REFERENCES