A 1.2Mpixels/s/mW 3-D Rendering Processor for Portable Multimedia Application

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Outline

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• System Architecture
• High Performance Rendering Processor
• Low Power Techniques
• Implementation Results
• Summary
Introduction

- Mobile Multimedia Evolution
  - 3D Graphics
  - DMB
  - Camera
  - MP3 Play

- Barriers to Portable 3D Graphics
  - Lack of System Resources
    - Processing Power
    - Memory Bandwidth
  - Limited Battery Lifetime

⇒ Low-Power, High Sustained Performance
Dedicated 3D Graphics Accelerator
Portable System : Bus Utilization

- **Bandwidth Bottleneck**
  - 3D Rendering Requires > 360MB/s Memory Bandwidth
  - System Bus Provides < 45MB/s
  - BW Mismatch → Performance Degradation
Separated Bus Architecture

- **Separated Data Bus**
  - Graphics Data Move to Graphics Memory
  - Only Vertex Data Transfer through System I/F < 40MB/s
  - Less Than System Bus Budget (45MB/s)
High Performance Rendering Processor

- **SlimShader**(1)
  - 2 Pixel Pipelines ⇒ 2Pixels/cycle
  - Depth-First Clock Gating ⇒ 25% Power Reduction
  - Address Alignment Logic ⇒ 69% Texture Access Reduction

RSB Mapping

- **Horizontal Order Rasterization**
  - Low Power Consumption
  - High Conflict Miss Rate during Texture Mapping

- **Recursive Sub-Block (RSB) Mapping Method**
  - Change Image Order in Texture Memory
  - Reduce Conflict Miss During Block Change

(a) Conventional 8x8 Block Mapping

(b) 2x2 Recursive Sub Block Mapping
• **15.2% Execution Time Reduction**
  – 1KB Texture Cache / 2-Way Set Associative
  – Bilinear Texture Filtering is Used

⇒ **17% Energy Saving**
Low Power Techniques

(1) Non-Atomic Read-Modify-Write (NARMW) Control
(2) Partial Activated Depth Buffer (PADB)
(3) Logarithmic Texture Unit
Basic of RMW Operation

- **Read-Modify-Write Operation**
  - The Most Frequent Operation in 3D Graphics
  - One Cycle RMW Operation is Needed

- **Previous Solutions**
  - One Cycle RMW e-DRAM
    - KAIST RAMP-IV\(^1\), SONY PSP\(^3\)
    - Technology Dependent Techniques
  - Higher Clock Frequency SRAM
    - 3~4 Times Higher Than 3DRE Clock Frequency
    - High Power Consumption

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(3) Yoshikazu Kurose et, al., “A 90nm embedded DRAM…”, HOTCHIPS 2004
Low Power Techniques(1)

NARMW Memory Timing

- **Pipelined RMW Operation**
  - Inside Rendering Operation
  - Decrease Memory Clock Frequency.
- **Read-After-Write Data Hazard Problem**
  - Pixels Drawing at the Same Position
  - Data-Forwarding Can Solve Data Hazard
Low Power Techniques(1)

NARMW Controller

- NARMW Controller
  - Partial Activation Control / Data Forwarding
- Power Reduction by NARMW
  - 33% of Memory Power Consumption
Embedded Depth Buffer

- Depth Data Consume Most of Bandwidth
  - Depth Comparison for Every Pixels
  - About 40% of Bandwidth Used for Depth Data

- Latency Degrades Rendering Performance
  - Latency Makes Bubbles in RE Pipeline

- Previous Solution
  - Multi-Level Depth Cache
    - High Design Complexity
    - High Power Consumption

⇒ 160KB Embedded Depth Buffer is Used

(2) Steven Morein, “ATI Radeon Hyper-Z Technology”, Graphics H/W 2000
Partial Activated Depth Buffer

- Only Two Memory Requests in Every Rendering Cycle
  - Two Address-Space are Activated
  - Other Address-Spaces Can be in Sleep Mode
- Depth Buffer is Partitioned into 10 Sub Modules
- Power Reduction
  \[ 24.4 \text{mW} \Rightarrow 5.2 \text{mW} \]
Logarithmic Texture Unit

• Perspective Correct Texture Mapping
  – Requires Per Pixel Division
    • OpenGL|ES Requires 32bit Texture Coordinate
    • Two 32bit / 32bit Divisions
  – Low Latency and Low Power Divider is Required

• Logarithmic Divider\(^{(4)}\)
  – One Cycle 32bit by 32bit Division
  – Enhanced Approximation Model
  – Low Power Consumption
    $\Rightarrow$ 1.2mW 3DRE Power Reduction

\(^{(4)}\) Hyejung Kim et al., “A 231MHz, 2.18mW 320bit Logarithmic…”, A-SSCC 2005
Power Consumption

mW

50.5mW
38.3mW
36.6mW
19.1mW
18mW
17.2mW

No NARMW, PADB, LAU, RSB
Non-Atomic RMW Control
Partial Activated Depth Buffer
Non-Atomic RMW Control
Partial Activated Depth Buffer
Logarithmic Texture Unit
Non-Atomic RMW Control
Partial Activated Depth Buffer
Logarithmic Texture Unit
RSB Mapped Texture Cache

Texture Cache
Depth Buffer
Rendering Engine
Rendering Performance Comparison

**Performance Index of Portable 3D Graphics**

- Performance Index = \( \frac{\text{Pixel Fill Rate}}{\text{Power Consumption}} \)
  (Analogous to MIPS/mW)
- Power Consumption is Normalized at 1.8V Supply Voltage
Implementation Results

- 0.18μm CMOS
  - 1-Poly 6Metal
- 25mm²
- Power Supply
  - 1.8V (Logic Core)
  - 3.3V (I/O)
- 10MHz Operation
- Power Consumption
  - Less Than 17.2mW
- Pixel Fill Rate
  - 20Mpixels/sec
- Transistors
  - 350K Logic Gates
  - 164KB SRAM
Summary

- Energy Efficient 3-D Rendering Processor is Designed and Implemented
  - High Sustained Performance
    - Sustained 2 pixels/cycle
  - Low Power Consumption
    - < 17.2mW
      \( \Rightarrow 1.2 \text{Mpixels/s/mW Rendering Performance} \)
  - 25mm\(^2\) in 0.18\(\mu\)m CMOS Technology
  - Successfully Demonstrated on the System Evaluation Board