A Fixed-point Multimedia Co-processor with 50Mvertices/s Programmable SIMD Vertex Shader for Mobile Applications

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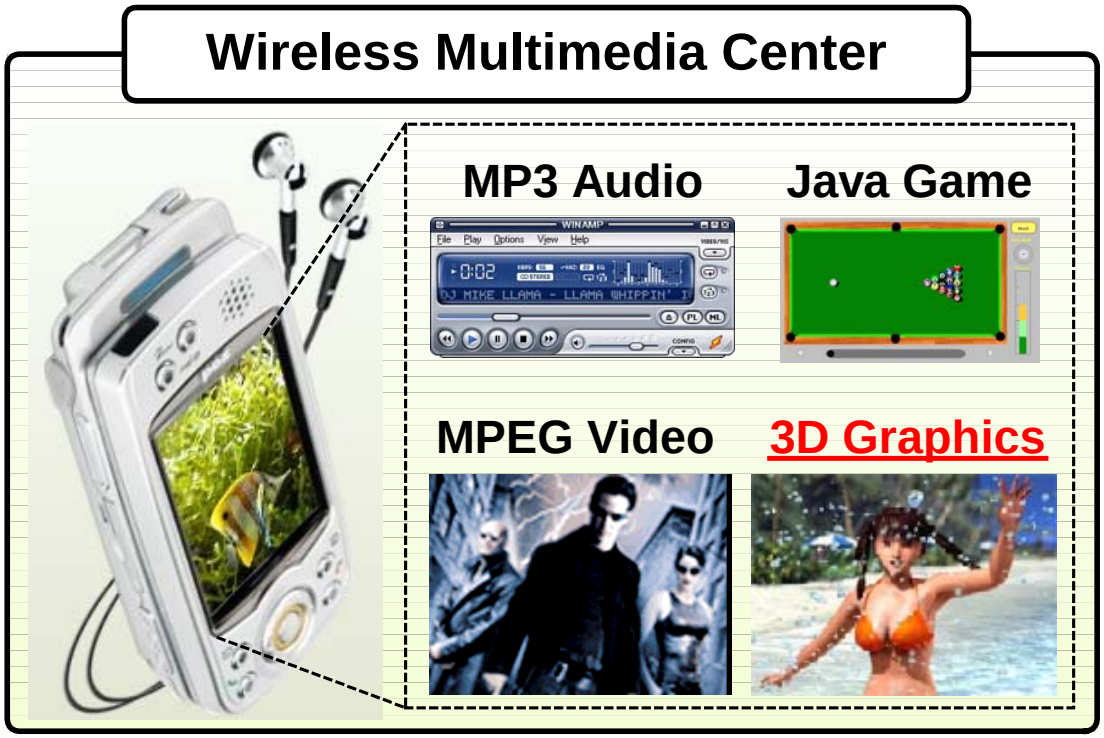
Outline

- **Introduction**
- **System Architecture**
- **Low Power Features**
  - Fixed-point processing
  - Instruction-wise clock gating
- **SIMD Datapath Structure**
  - ALU, Multiply, SFU
- **Implementation Results**
- **Summary**

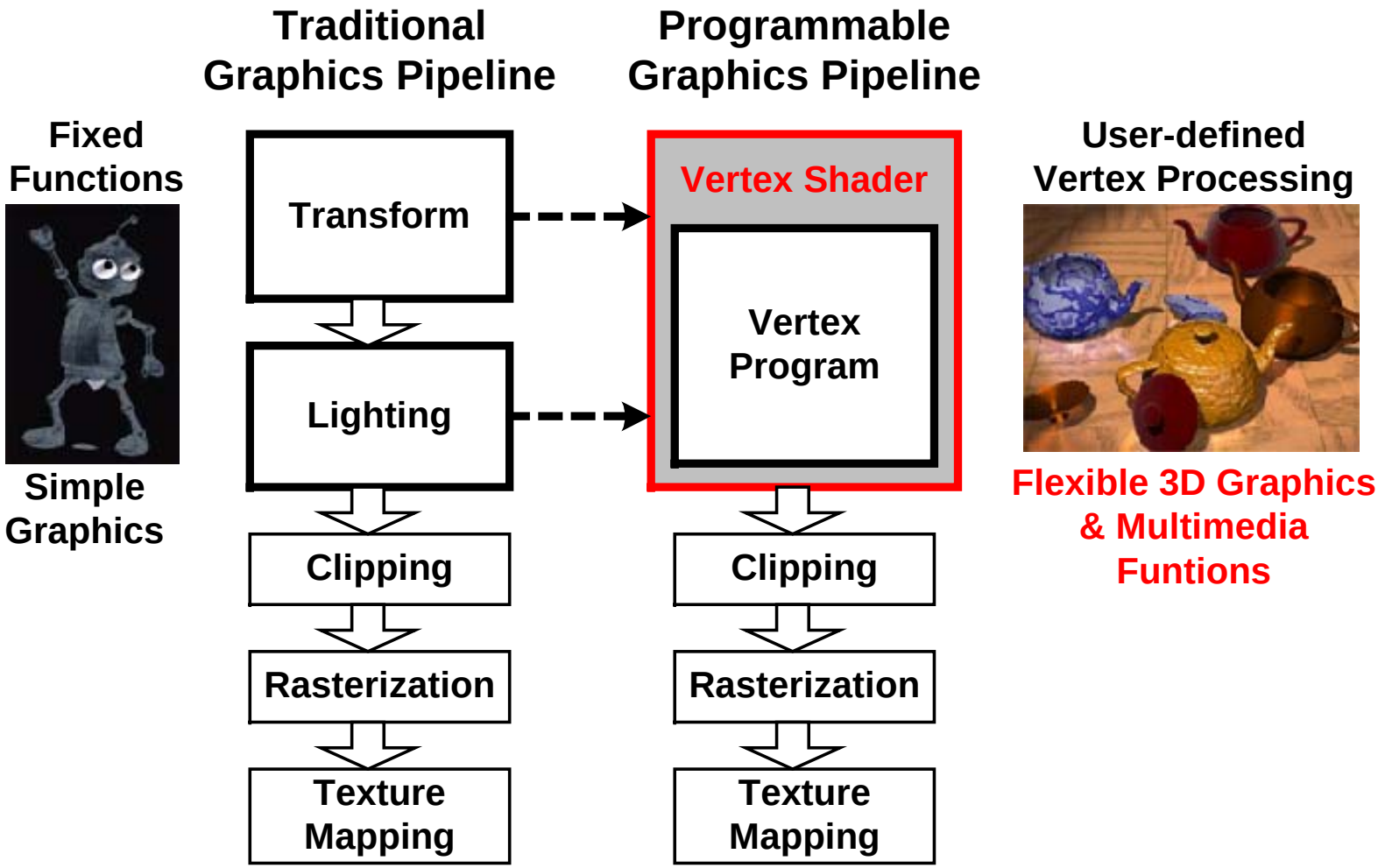
3G Mobile Terminals



- **Requirements**
  - Low power (< 200mW)
  - High performance (>1Mvertices/s)
  - Variable Applications (Programmability)
  - Low cost (<5$)

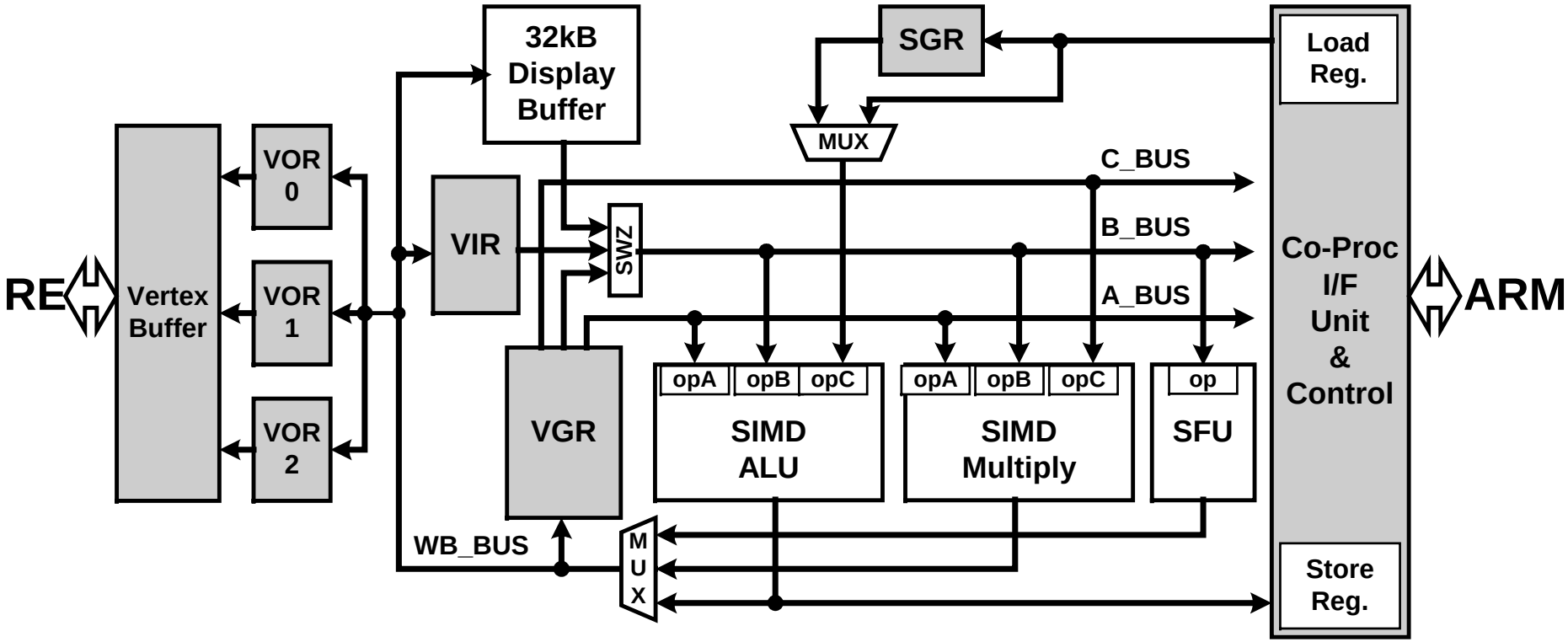
- **Fixed-point multimedia co-processor**
  - Low power consumption in ARM-10 architecture
  - Programmability with SIMD vertex shading

Programmability in Graphics Hardware



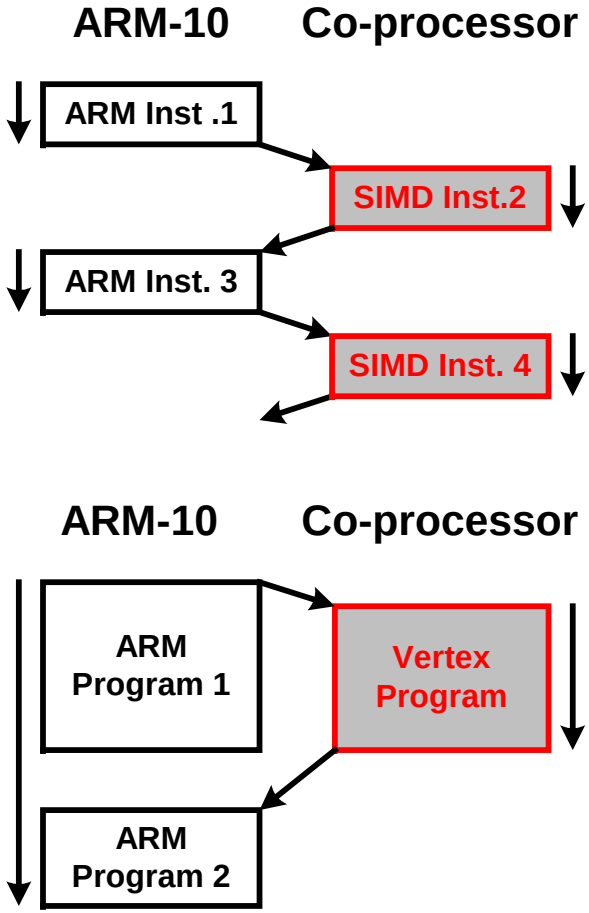
Co-processor Architecture

- **128-bit 4-way SIMD ARM-10 Co-processor**

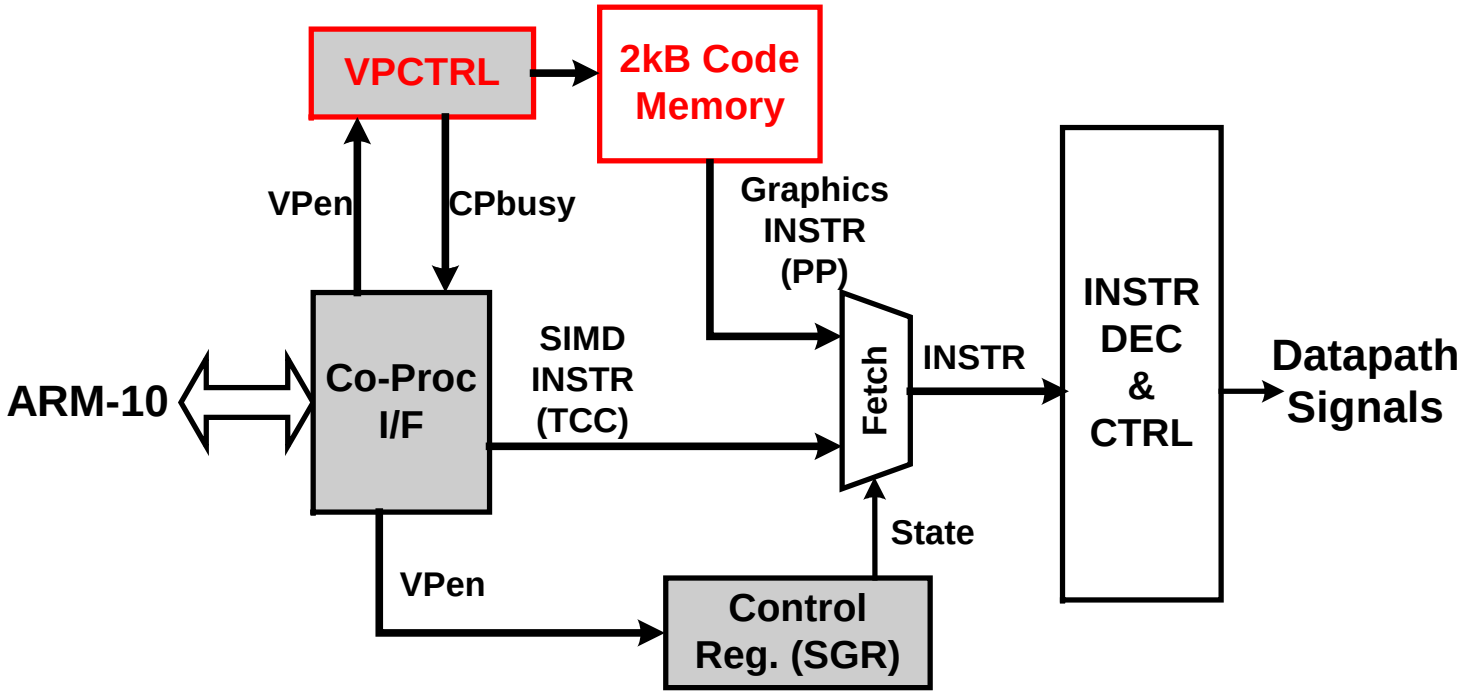


Dual Operations

- **Two operating states**
  - Tightly coupled co-processor (TCC)
    - Normal co-processor
    - General SIMD instructions
    - Handshaking with ARM-10
  - Parallel processor (PP)
    - Independent processor
    - Graphics instructions
    - Parallel operations with ARM-10



Processor State Control



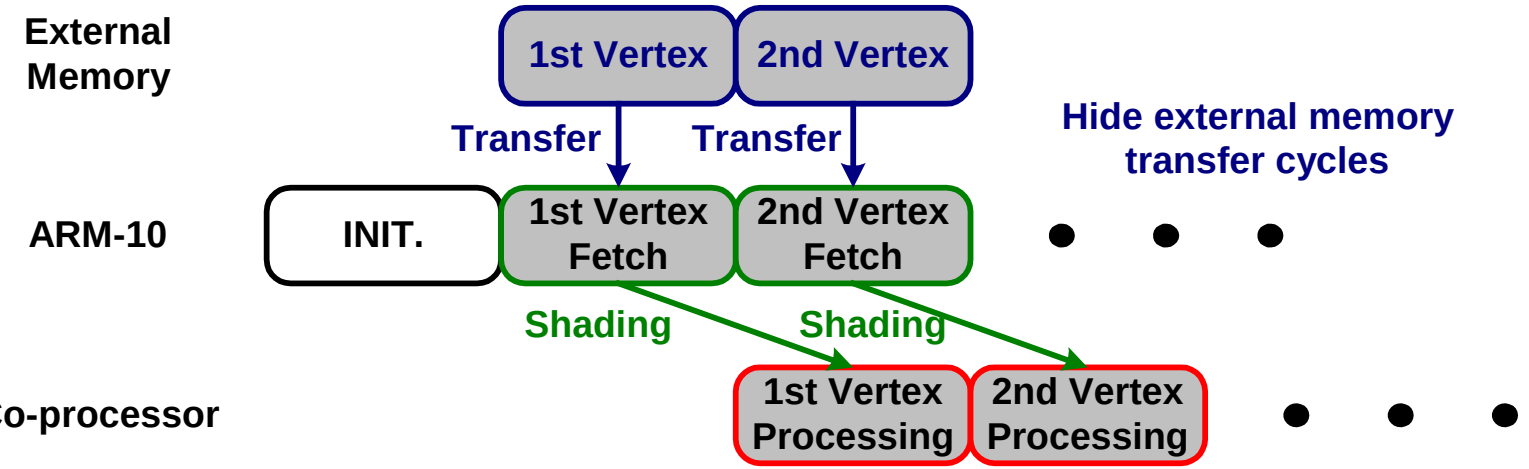
- **Enhanced co-processor I/F for PP state**
  - VPCTRL with 2kB code memory
  - Share all HW blocks with TCC state
  - Drive CPBusy for synchronization

Programmable Vertex Shader

- **Shader instruction extensions in PP state**
  - Source swizzling and write masks

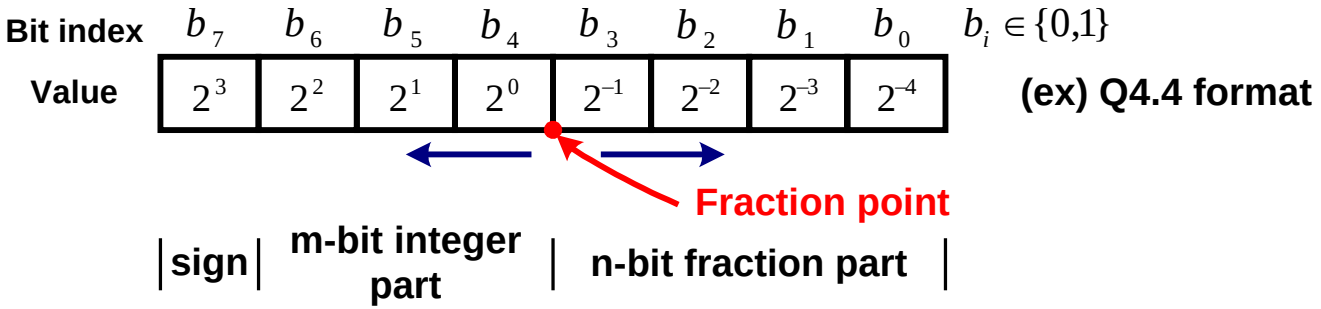
    VGR2 = VGR0 + VGR1 (TCC state) ➡ VGR2.xyzw = VGR0 + VGR.xyzw (PP state)
  - More operands

    VGR2 = VGR0 + VGR1 (TCC state) ➡ VOR2.xyzw = VIR0 + MEM[1] (PP state)
- **Parallelism for streaming graphics data**



Fixed-point Processing
: Low Power Features (1)

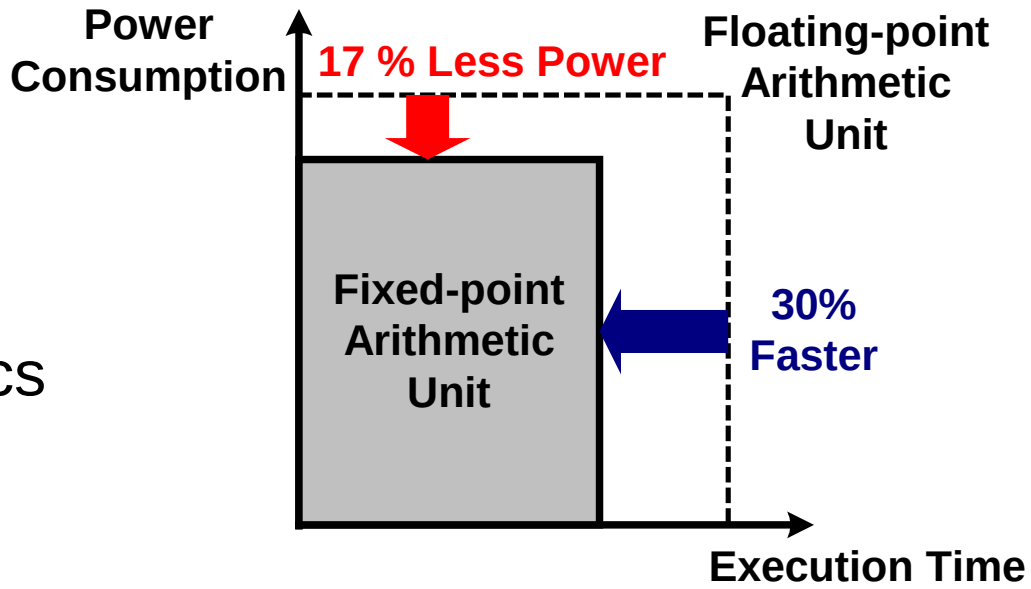
- **Fixed-point number representation**



- **Energy efficiency**
  - 40% less energy

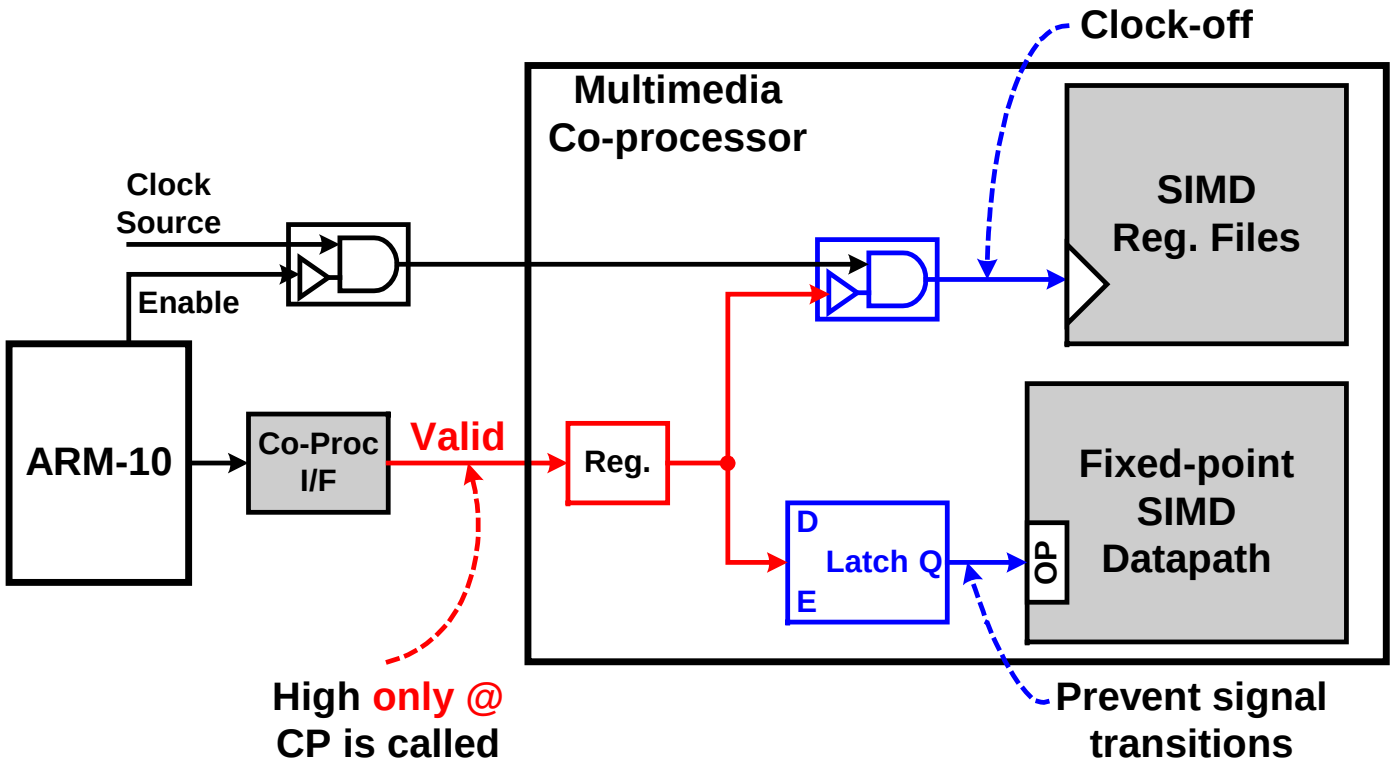
    than floating-point

    on avg. in 3D graphics



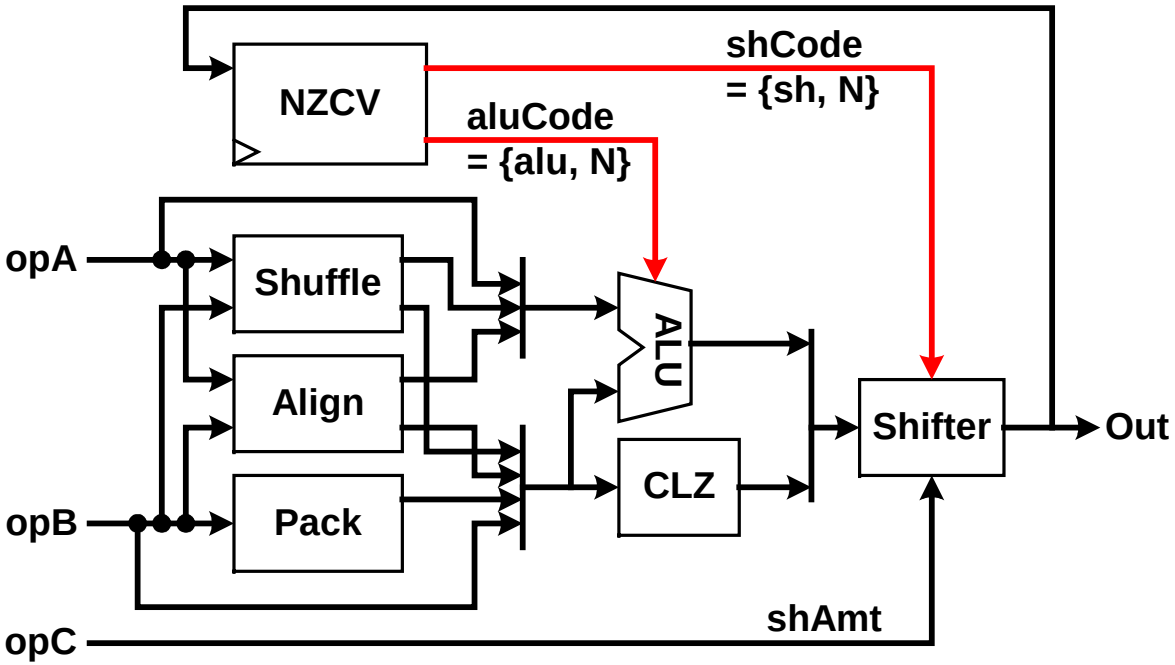
Instruction-wise Clock Gating
: Low Power Features (2)

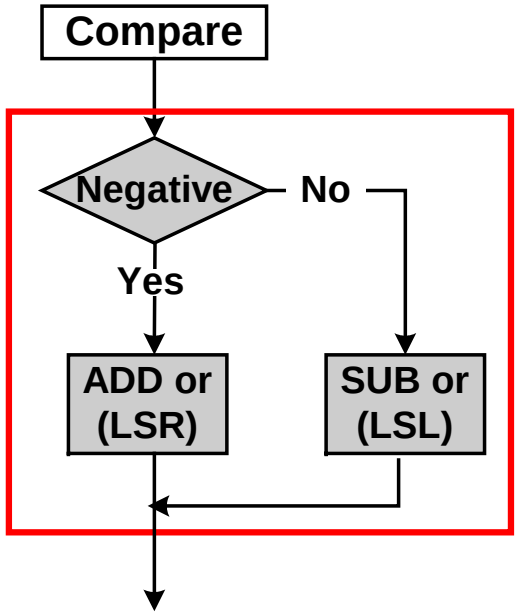
- **SIMD RF and datapath are the most power-consuming parts**
  - Activation in instruction-by-instruction basis



SIMD Datapath : ALU

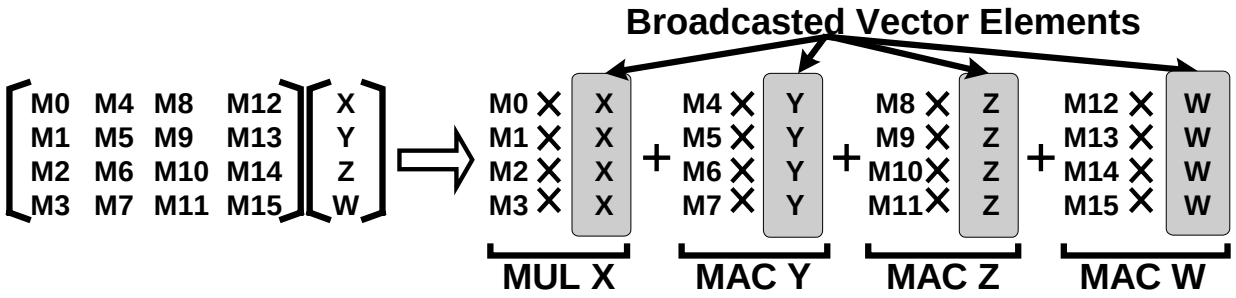
- **Single-cycle integer and fixed-point op.**
  - Arithmetic, logic, shuffle, packing, alignment
  - SW floating-point emulation (80Mflops peak)

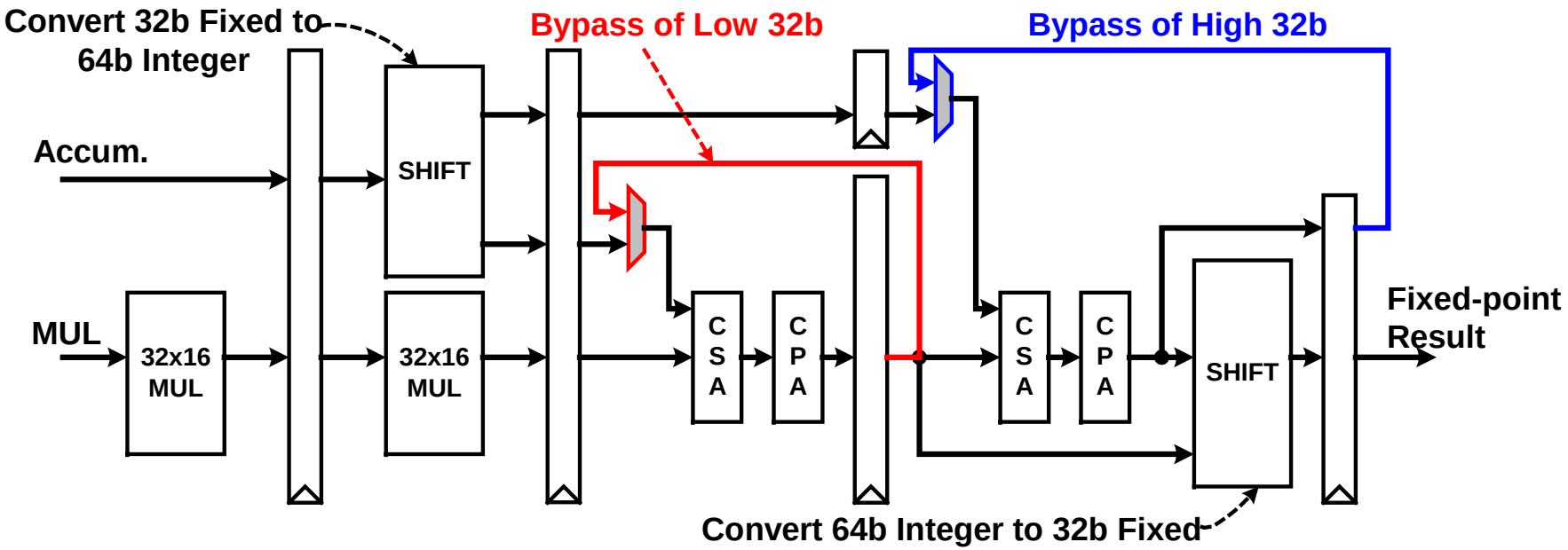




SIMD Datapath: Multiply

- **4-cycle matrix transformation**

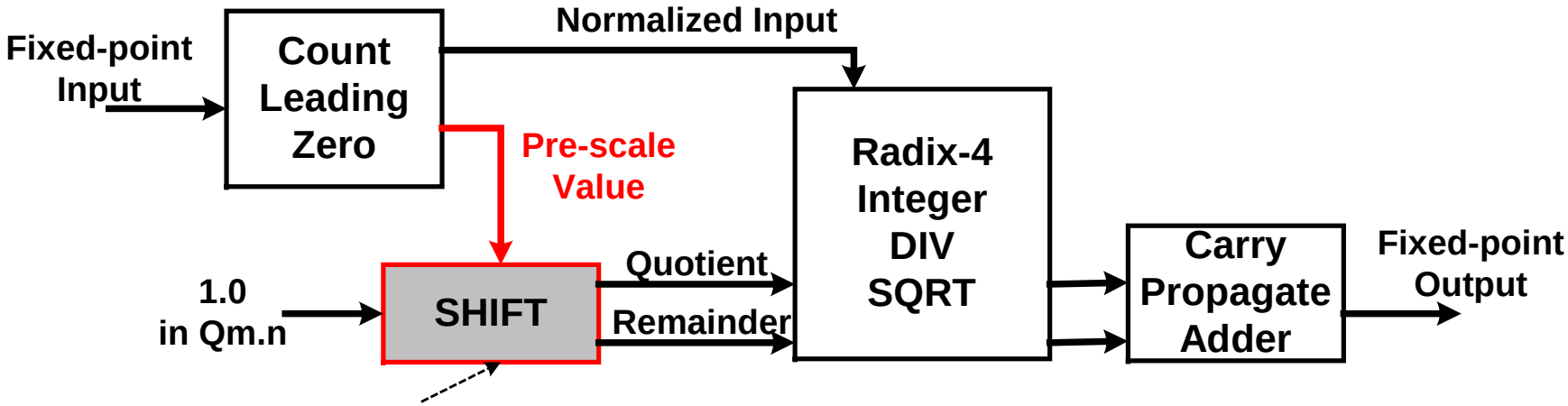




SIMD Datapath: Special Function Unit

- **Calculate RCP (1/x) and RSQ (1/sqrt(x))**
  - Fixed-point input → Fixed-point output
  - No additional data type conversion circuits

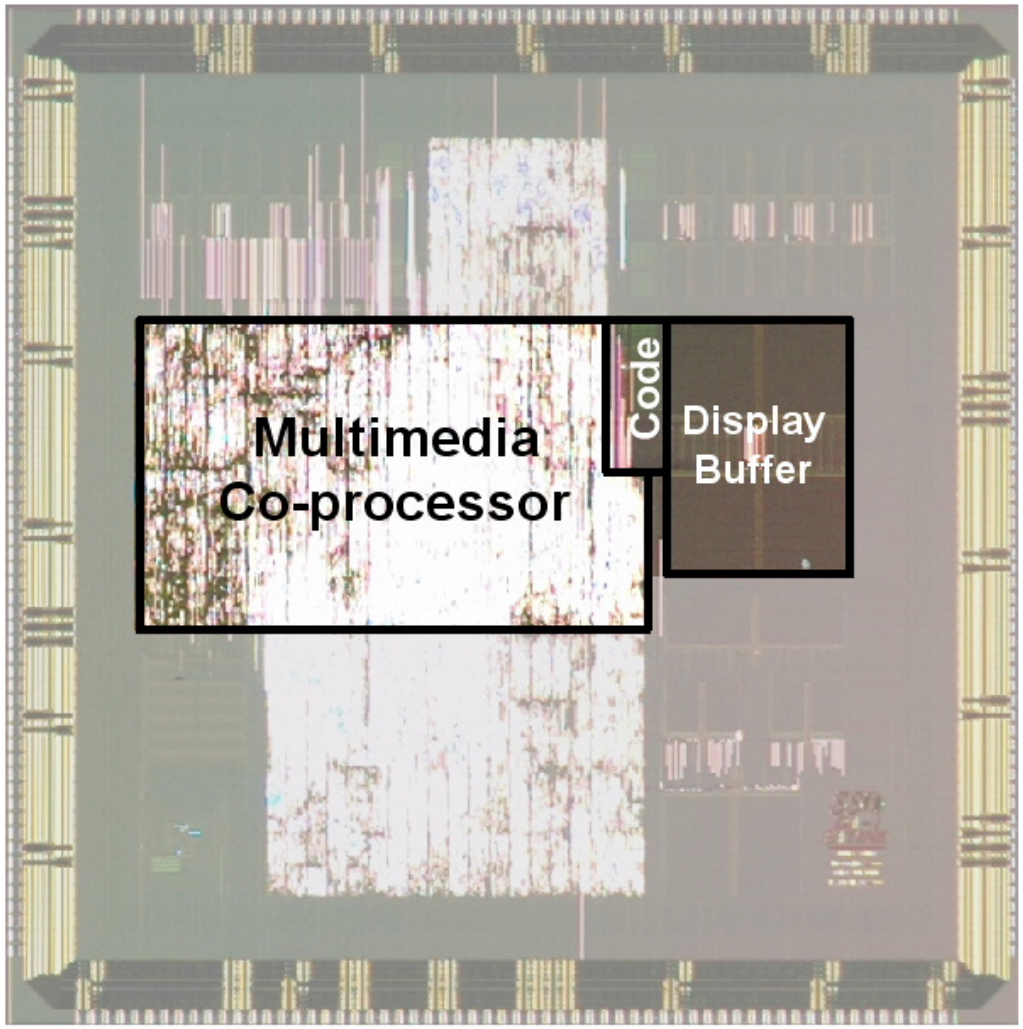
For Qm.n Fixed-point Format



- **Scale up fixed-point dividend to 64b space**

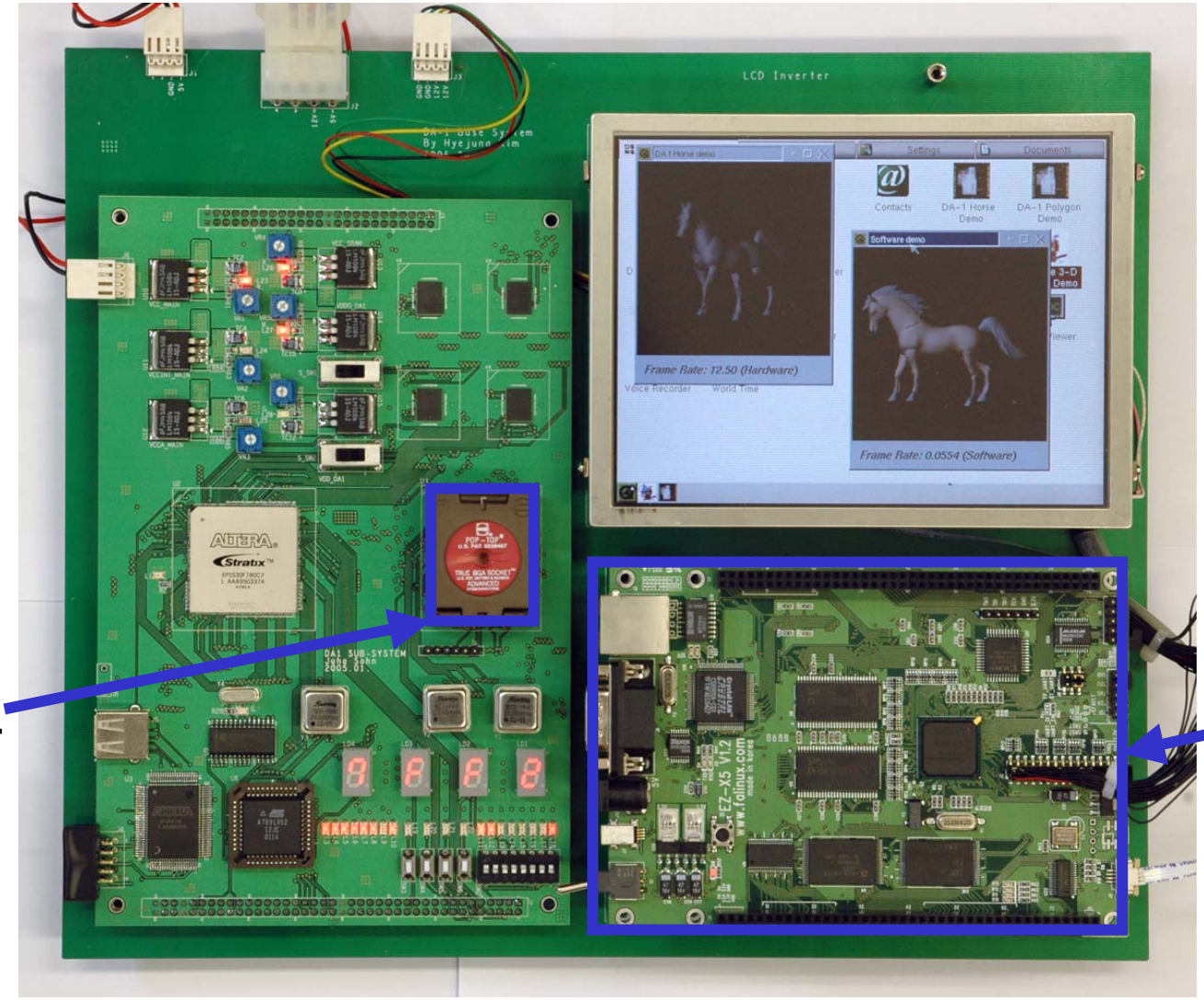
OP	Pre-scale Value
RCP	# of Leading Zero
RSQ	n/2 + # of Leading Zero

Integration into a Mobile Graphics Processor



- **0.18μm CMOS**
  - 1P6M
- **200MHz**
- **10.2 mm²**
  - Full chip (36 mm²)
- **75.4 mW**
  - Full chip (155mW)
- **3D performance**
  - 50Mvertiecs/s (Parallel projection)
  - 3.6Mvertices/s (Full 3-D geometry)

System Evaluation Board



Graphics Processor

Linux Host

Conclusion

- **Low power multimedia co-processor for 3G wireless terminals**
  - Programmable SIMD vertex shader
    - ARM-10 co-processor architecture
    - Flexibility for various multimedia applications
  - Low power features
    - Energy-efficient fixed-point SIMD datapath
    - Instruction-wise clock gating
  - High performance
    - 50Mvertices/s for parallel projection
- **<75.4mW, 10.2 mm^2**
  - Integrated into the mobile graphics processor
  - Successfully demonstrated on evaluation board