A Low Power Compression Processor for Body Sensor Network System

Hyejung Kim, Sungdae Choi, and Hoi-Jun Yoo

Semiconductor System Laboratory
Department of Electrical Engineering and Computer Science, KAIST
Daejeon, Korea

Abstract— **A low power 16-bit RISC is proposed for body sensor network system. The RISC is designed of basic 3 stage pipeline architecture which has 28 instruction sets. Some special instructions are proposed for efficient applications. The lossless compression accelerator is embedded in the RISC to support the low energy data compression. The accelerator consists of 16x16-bit storage array which has vertical and horizontal access path. By using the accelerator the energy consumption of the lossless compression operation is reduced by 95%. The RISC is implemented by 1-poly 6-metal 0.18um CMOS technology with 16k gates. It operates at 4MHz and consumes 24.2uW at 0.6V supply voltage.**

Keywords— **Body Sensor Network, RISC, Lossless Compression**

I. INTRODUCTION

Recently, in according with the interests about the healthcare increase, people desire to check their vital signal or health condition at anytime and anywhere. To solve this request, the wireless sensor network (WSN) system has been studied to apply for the body, which called body sensor network (BSN) system [1]. The BSN system offers health condition monitoring, vital signal collecting, collected data analysis and diagnostics. To provide these various operations, BSN system should consists of lots of sensors, the data processing unit and the efficient network system. Various BSN systems have been proposed to provide the services [1]-[6].

BSN system requires the ultra low energy operation for stable long time operation and the small footprint for wearability. To achieve these requirements, the size of hardware components has to be small. Moreover, they also have limited power supply, bandwidth for communication, processing speed, and memory space. Various researches have been conducted so far focuses on how to achieve the maximum utilization of limited source. The data compression is one of the most effective methods [7]. Since the transmitting power consumption is much more than the data processing power, minimizing data size before transmitting can reduce total system power consumption. Moreover, the low power hardware design and the efficient algorithms are also important for limited resource.

This paper presents a low power RISC for low energy BSN system. The efficient compression algorithms optimized to bio signals is also proposed. We verify low energy consumption of the proposed RISC by implementation of real silicon and test board.

II. 16-BIT RISC ARCHITECTURE

A. Top Architecture of 16-bit RISC

The 16-bit RISC is designed based on a basic 3-stage pipeline which is optimal selection for low power operation [3]. The figure 1 shows the pipeline flow diagram of the proposed 16-bit RISC. The first stage fetches the instruction from code memory, and the second stage decodes the fetched instruction. The last stage executes ALU operations, memory access, and write-back to the register file. Since the both operations of read and write the register file occurs in the same stage, the data hazard is eliminated. The branch is performed with a 2-cycle penalty.

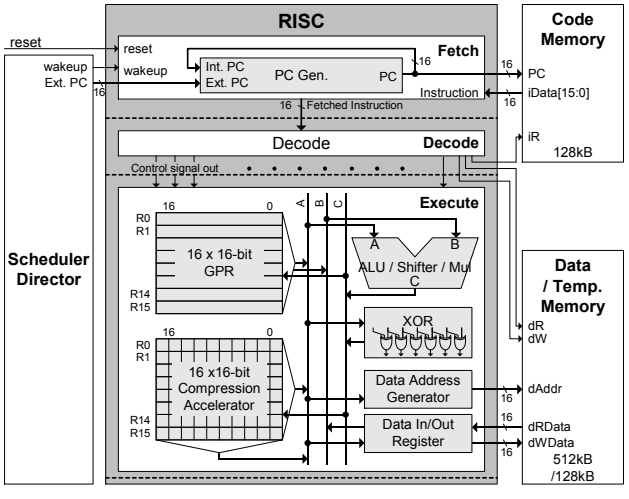


Figure 1. Top Architecture of the Processor

The RISC has 2 kinds of register files which are the 16 general register files and the compression accelerator for the proposed lossless compression algorithm described in next section.

TABLE I. RISC INSTRUCTION SET ARCHITECTURE

ALU Register	MOV, CMP, ADD, SUB, AND, ORR, XOR, BIC, MUL, MVN, NEG
	MGX, MXG, REV, XRC, XRD
ALU Immediate	MOV, ADD, SUB, CMP
Shift	LSR, LSL, ASR, ROR
Memory	LDR, STR, STRX
Conditional Branch	BEQ, BNE, BGT, etc… (16 Conditions)

B. Instruction Set Architecture

The processor implements 16-bit Instruction Set Architecture (ISA). The RISC has 28 instructions, the table I shows the implemented instruction sets. Some special instructions are proposed for the compression algorithm.

XRC, XRD : XRC instruction operates bitwise XOR operation with right next bit. XRD instruction performs reverse operation of XRD. Figure 2 shows the block diagram of the XRC operation, where *Rs* represents the source register and *Rd* represents the destination register.

$$Rd[i] = Rs[i] \oplus Rs[i+1]$$

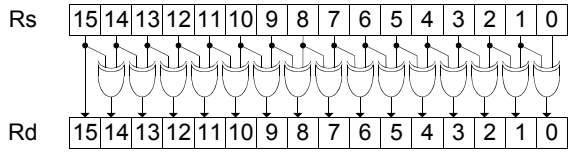


Figure 2. Block Diagram of XRC operation

MGX, MXG : MGX moves the data from general purpose register to special purpose register. MXG moves the data from special purpose register to general purpose register.

REV : REV moves the MSB to LSB, and LSB to MSB. Figure 3 shows the block diagram of the REV operation.

$$Rd[i] = Rs[15\text{-}i]$$

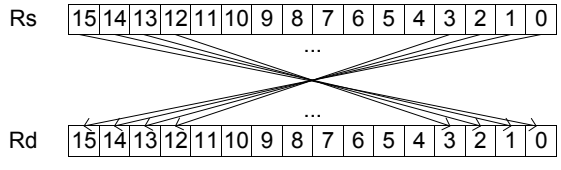


Figure 3. Block Diagram of REV operation

STRX : STRX loads the data from special purpose register, and store them to the data memory if the header bit is one. After store the data, the memory address is increased automatically. It helps to reduce the repeated store operation, when the 256 bit data are stored. *Rm* represents the memory address for data memory.

$$if\ (!head)\ Mem[Rm] = \{Rd\},\ Rm = Rm + 0x01$$

III. PROPOSED LOSSLESS COMPRESSION ALGORITHM

A. Compression for BSN

The sensor nodes gather the bio signal data, process the collected data, and transfer the processed data to base station. If a single sensor node sends n-bit data, the total power consumption (P_{Total}) is derived as following:

$$P_{Total} = n \times \{P_{Comp} + (1-\alpha)(P_{TX} + P_{RX} + P_{DeComp})\}$$

where,
n = *Data bit width*
a = *Compression rate*
P_{Comp} = *power consumption for Data compression*
P_{DeComp} = *power consumption for Data de-compression*
P_{TX} = *power consumption for Data transmission*
P_{RX} = *power consumption for Data receive*

We have quantitative value of P_{TX}=2.5nJ/b, P_{RX}=2.5nJ/b, P_{Comp}=0.003nJ/b and P_{DeComp}=0.003nJ/b from previous work [3-5]. Assuming that the sensor node gathers 1Mb data, the total power consumption would be changed under variable compression rates, the figure 4 shows them. The high compression rate helps greatly to reduce the total power consumption.

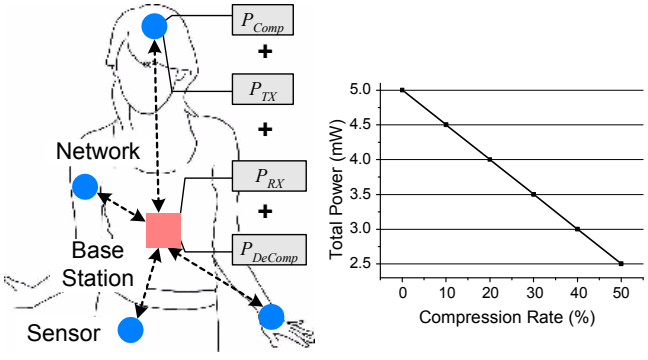
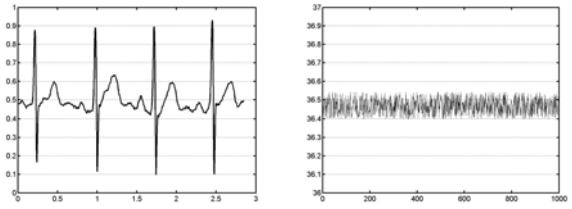


Figure 4. Comparison of Power Consumption

Therefore, it is necessary to employ a data compression algorithm for body sensor network system. There are some limitations to apply the compression algorithm to BSN system. First, since the sensor node currently has limited

resources such as battery energy, CPU performance and the memory capacity, the algorithm size must be as small as possible. The second one is the operating frequency. Usually the processor of sensor node operates only less than 4MHz, therefore it is necessary to design a low complexity algorithm which is enough to operate at low frequency. Because the hardwired accelerator and the special instructions help to reduce the operating cycles and the code size, the proposed compression algorithm is satisfied these requirements.



(a) ECG : 16bit (b) Temperature : 10bit

Figure 5. The Bio Signal with Variable Resolution

The proposed compression algorithm, which name is BiPAC, has three features. First, BiPAC provides the lossless compression. The lossly compression algorithm is efficient to minimize data size, but all loss algorithms have some degree of quantization error, resulting in a possible loss of diagnostic information. Thus, the lossless compression algorithm is studied to preserve all the information of original data. Second, BiPAC is optimized to continuous signal data. Most of bio signals consist of continuous and periodic waveform differ to other randomly media data. The last one is various precision coding. Each kind of sensor data has variable precision. For example, the ECG signal consists of 16 bit resolution, otherwise, the temperature signal consists of only 10 bit resolution. The figure 5 shows that 2 kinds of bio signals. Since the width of the system bus is 16bit, a lot of leading zeros can be generated when the resolution is less than 16 bit. BiPAC eliminates these redundant leading zeros simply so that it is suitable for the all kinds of various precision data compression.

B. BiPAC - Lossless Compression Algorithm

The algorithm1 and figure 6 describes BiPAC which is the proposed lossless compression algorithm. BiPAC represents the Bi-PAth compression.

Algorithm 1 : BiPAC

Input : 16x16b TM data (TM[i], i=0..15)

Output : nx16b compressed DM data (DM[i] , i=0..n, n≤15)

```
1. for i=0 to 15 loop
     d[i] = TM[addr1+i];
   endloop
2. h0=d0; spr[0][*]=0; n=0;
3. for i=1 to 15 loop
     spr[i][*] = d[i] - d[i-1];
4. for i=0 to 15 loop
     for j=0 to 14 loop
          spr[i][j] = spr[i][j] xor spr[i][j+1];
     endloop
   endloop
5. for i=0 to 15 loop
     for j=0 to 15 loop
          h1[i] = h1[i] or spr[j][i];
     endloop
   endloop
6. for i=0 to 15 loop
     if h1[i]!=0
          DM[addr2+j] = spr[i][*];
          n = n +1;
     endif
   endloop
7. return DM[0]..DM[n]
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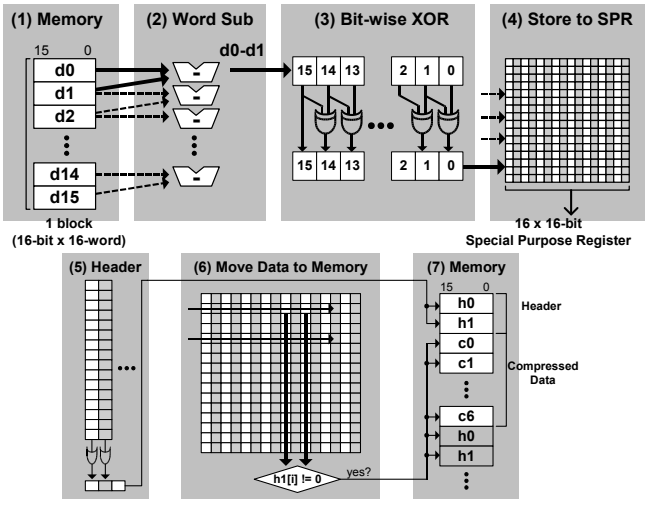

Figure 6. The Lossless Compression Algorithm

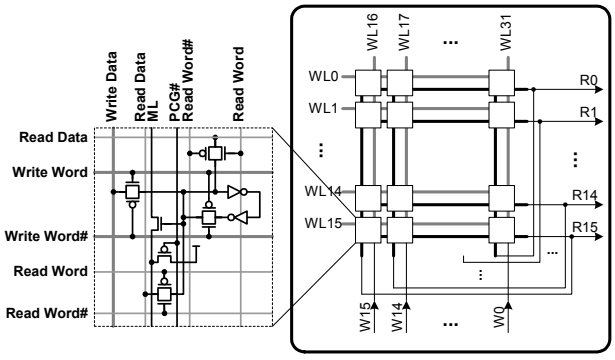

Figure 7. Lossless Compression Accelerator

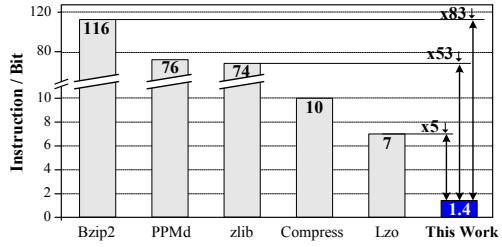

Figure 8. Required Instruction per Removed A Bit

C. Lossless Data Compression Accelerator

The data compression accelerator is embedded in the RISC to support the low energy data compression / decompression operation and it consists of 16x16 storage array shown in figure 7. Its vertical and horizontal accessibility reduces the required execution cycle to 95% compared with conventional RISC operation. The interface of accelerator is same as the register file, so all data transition takes 1 cycle by special instructions. In addition, it can be used as a general purpose registers when the compression program is not executed.

The proposed algorithm compresses the 1 block data (16x16-bit) into 2 headers and the compressed data and it takes up to 114-cycle. It is recalculated to 1.425-instructions/bit. Figure 8 shows comparison result of the number of instruction required by removing a single bit. By using the proposed algorithm with accelerator, the performance is improved by maximum 83 times compare to other conventional algorithms [7].

IV. RESULTS

A. Simulation Results

The ECG records data from the MIT/BIH [9] are used to verify BiPAC. The sampling rate and the resolution are 360 samples/s and 12 bits, respectively. The figure 9(a) shows the ECG record waveform and the figure 9(b) shows the simulation result of compression operation. The data memory write enable signal goes high if the column data are not zero. The compression rate is good if the number of enable signal is small. The compression rate is 25% and 56.3% at steep and slow slop, respectively. The better compression rate is obtained with stable signals. The average compression rate is 38.7% for 10 sec amount data. It consumes only 641us and 0.69nJ to compress 1 sec amount ECG data with 4MHz operation frequency. Table-II shows that the energy consumption of this work is much smaller than that of the conventional low-power processors [4], [5], [6] when 16x16bit data compression is executed. The proposed compression algorithm can operate sufficiently real time lossless compression/decompression with ultra low energy consumption.

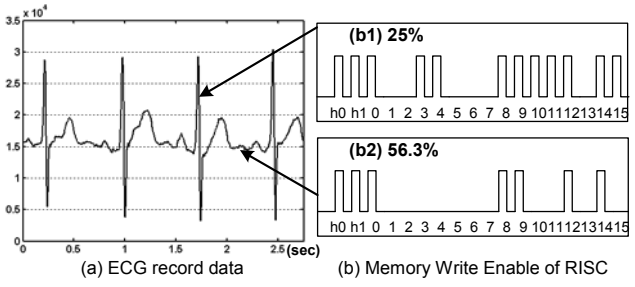

Figure 9. Simulation Result of Proposed Compression Algorithm

TABLE II. ENERGY COMSUMPTION FOR 16X16B DATA COMPRESSION

	[4]	[5]	[6]	Proposed
VDD	1.0V	0.66V	0.23V	0.6V
Clock	500kHz	4MHz	833kHz	4MHz
Energy	32.4nJ	64.8nJ	11.2nJ	0.69nJ

B. Implementation Results

With the proposed architecture, the RISC is implemented into a chip by using 1-poly 6-metal 0.18um CMOS technology. A demonstration board system is also implemented. They are shown in figure 10. The RISC size is 400umx1000um with the compression accelerator. The memory size of code memory, data memory and temporary memory is 128kb, 512kb and 128kb, respectively. The RISC operates maximum frequency of 200MHz with 1.8V and 22MHz with 0.6V. However, the RISC generally operates at 4MHz with 0.6V supply voltage for low energy consumption and reliable operation. The power consumption is 24.2uW with 4MHz at 0.6V supply voltage.

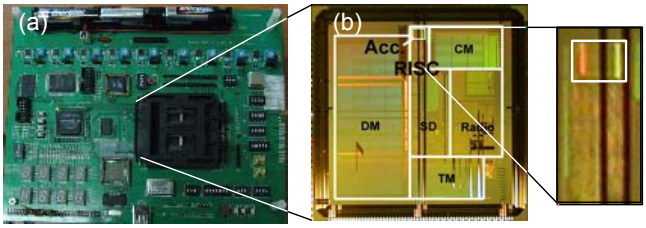

Figure 10. Implementation Result (a) Demonstraion Board (b) Chip Microphotograph

V. Conclusion

A 16-bit RISC of base station is proposed for body sensor network system. The RISC is designed based on basic 3-stage pipeline architecture. The lossless compression accelerator is embedded for low energy data compression. By using accelerator which consists of 16x16-bit storage array with vertical and horizontal access path, the energy consumption of the lossless compression operation is reduced by 83 times. The RISC is implemented by 1-poly 6-metal 0.18um CMOS technology with 16k gates. It operates at 4MHz and consumes 24.2uW at 0.6V supply voltage. The evaluation results clearly indicate the proposed RISC and compression algorithm are suitable for the body sensor network system.

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Address of the corresponding author:

Author: Hyejung Kim
Institute: KAIST
Street: Guseondong 373-1, Yuseonggu
City: Daejeon
Country: KOREA
Email: seeseah@eeinfo.kaist.ac.kr