A Reconfigurable Crossbar Switch with Adaptive Bandwidth Control for Networks-on-Chip

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Outline

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  - Adaptive Bandwidth control scheme
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Introduction

- System-on-Chip (SoC) design
  - Lots of heterogeneous IPs
  - Process scales down (Process variation)
  - Higher clock frequency

- Providing efficient interconnection is difficult
  - Reliable interconnection channel is required
  - Smaller clock domain

- Network-on-Chip (NoC) provides solutions for SoC design
  - Structured Interconnection
  - GALS communication
Motivation

◆ Variations on bandwidth.

<Homogeneous IPs>

<Identical Processing Units
→ Small Bandwidth Variation

Heterogeneous IPs
→ Large Bandwidth Variation

Motivation (Cont’d)

- Conventional crossbar switch is not efficient building block of the NoC.

Performance is degraded due to insufficient bandwidth.

Waste of power or silicon area.
Related Works

- No considerations for NoC traffic conditions.

**FLEXBAR**
- [CICC 2002]
- Improved channel utilization

**NAMOO**
- [CICC 2003]
- Light-weight crossbar switch scheduler

**A 51mW 1.6GHz On-Chip Network...**
- [ISSCC 2004]
- Partial activation → Low power crossbar switch

Improved channel utilization

Light-weight crossbar switch scheduler

Partial activation → Low power crossbar switch
Proposed Switch Structure

- Additional bus accelerates heavily loaded input port.

Bandwidth is temporally doubled

Normal Transfer

Additional Bus
Bandwidth Control Scheme

- Additional bus enables adaptive bandwidth control.

< Low Bandwidth >

- FIFO has unused entry
  → 4 Cycles / Packet

< High Bandwidth >

- FIFO full
  → 2 Cycles / Packet
Buffer status determines use of additional bus.
Order of physical transfer unit is aligned at the output port.
Simulation Setup

- **Traffic generators**

<table>
<thead>
<tr>
<th>Case</th>
<th>Num. of TGslow</th>
<th>Num. of TGfast</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>6</td>
</tr>
<tr>
<td>4</td>
<td>TGslow ~ TGfast (8 steps)</td>
<td></td>
</tr>
</tbody>
</table>

- **3 Crossbar switches**

- Conventional 1X speed
- Conventional 2X speed
- Proposed 1X speed

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Throughput Comparison

Maximum 27% improvement

Case 1

Case 2

Case 3

Case 4

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Latency Comparison

Case 1

Case 2

Case 3

Case 4

Maximum 41% improvement
MPEG 4 Example

- MPEG 4 system is modeled on a mesh NoC.

1) E.B. Van der Tol. et. al.
“Mapping of MPEG-4 Decoding on a Flexible Architecture Platform”
# Implementation Result

## Synthesis result and power comparison

<table>
<thead>
<tr>
<th></th>
<th>Conventional</th>
<th>Proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Estimated Area (unit inverters)</td>
<td>70524</td>
<td>85401</td>
</tr>
<tr>
<td>Maximum Operating Frequency</td>
<td>418 MHz</td>
<td>406 MHz</td>
</tr>
<tr>
<td>Power Consumption (at 400MHz)</td>
<td>66.8 mW</td>
<td>76.7 mW</td>
</tr>
</tbody>
</table>

## Energy consumption

<table>
<thead>
<tr>
<th></th>
<th>Conventional</th>
<th>Proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy Consumption</td>
<td>0.99 mJ / MB</td>
<td>0.92 mJ / MB</td>
</tr>
</tbody>
</table>

*7% improvement in energy consumption!*
FPGA Implementation

- Proposed Crossbar switch is verified with various IPs.
Conclusion

- A Crossbar switch with adaptive bandwidth control is designed and verified.
  - Additional bus enables adaptive bandwidth control.

- Maximum 27% and 41% improvements in throughput and latency are achieved.

- With Adaptive bandwidth control scheme, efficient integration of heterogeneous IPs in NoC design is enabled.