Design and Implementation of Read-Compare-Write Circuits for Low Power Multi-Gigabit DRAM

Sungdae Choi, Yong-Ha Park and Hoi-Jun Yoo

Semiconductor System Laboratory

Department of Electrical Engineering

Koread Advanced Institute of Science and Technology (KAIST)

Outline

- Introduction
- Read-Compare-Write (RCW)
- Adaptive Column Control (ACC)
- Simulation Results
- Conclusions

Introduction

- Low Power Memory for Mobile Multimedia Application

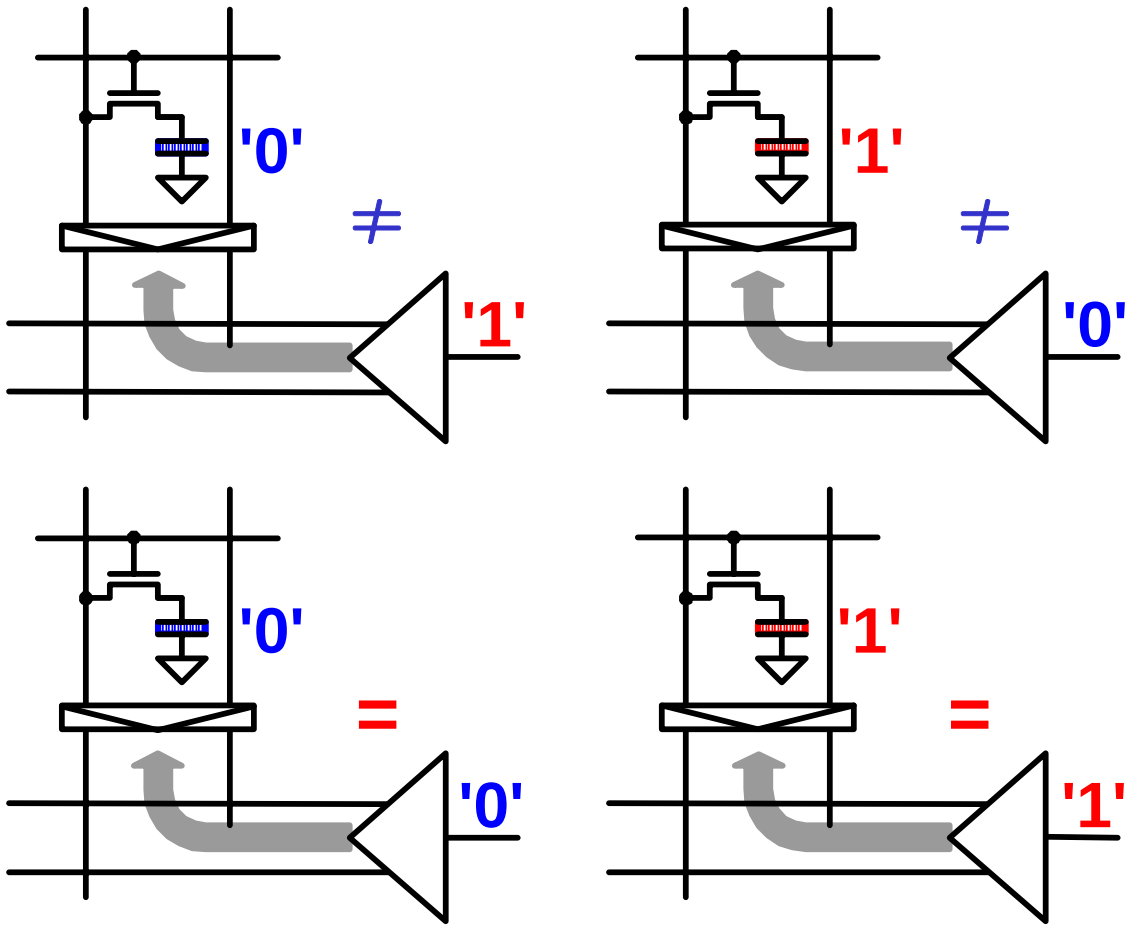
Limited Battery Lifetime

3D Graphics

Portable Video

Frequent Memory Write Operations

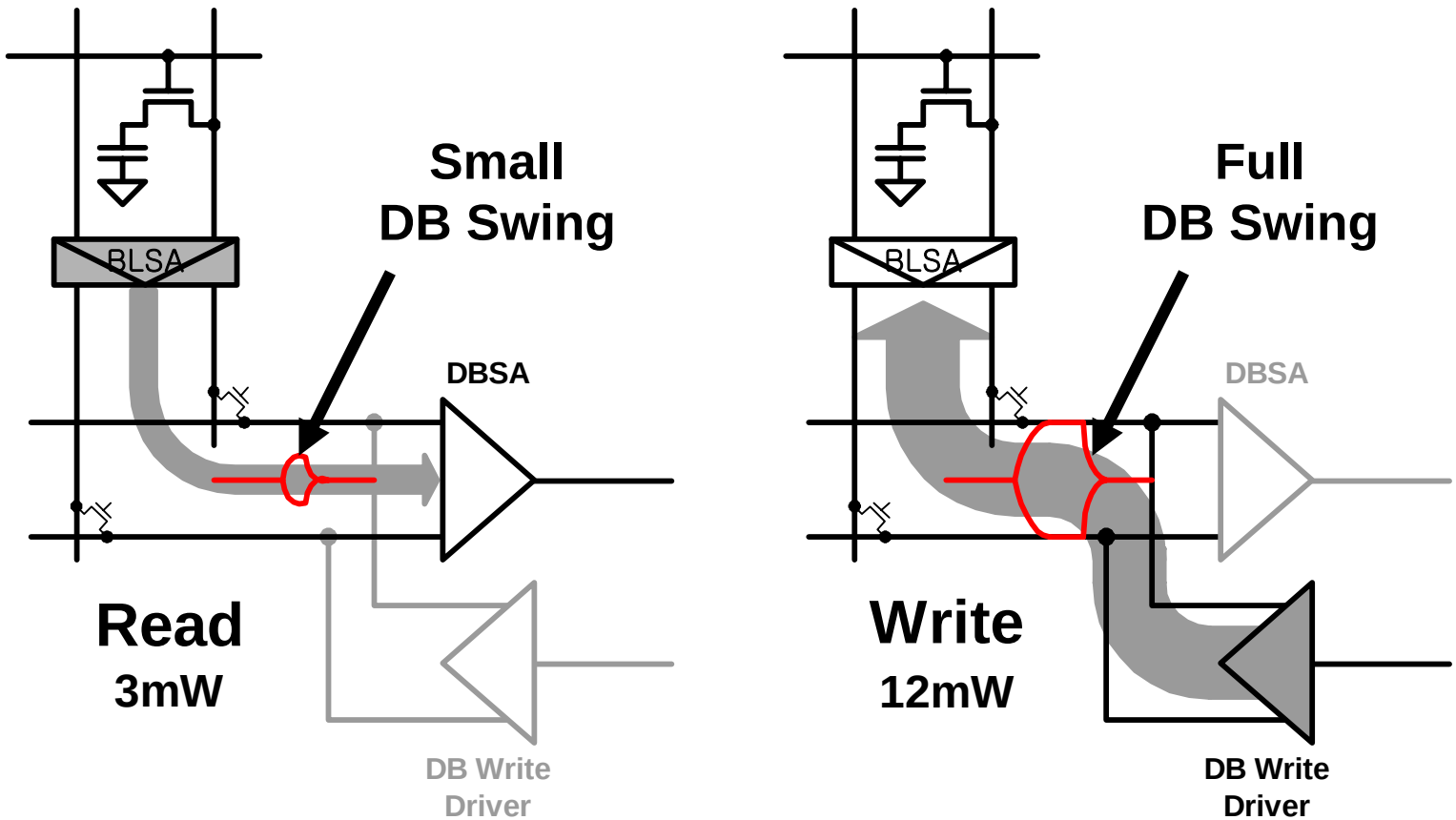
Conventional Write Operation



Case 1
Write operation is necessary

Case 2
Write operation is redundant

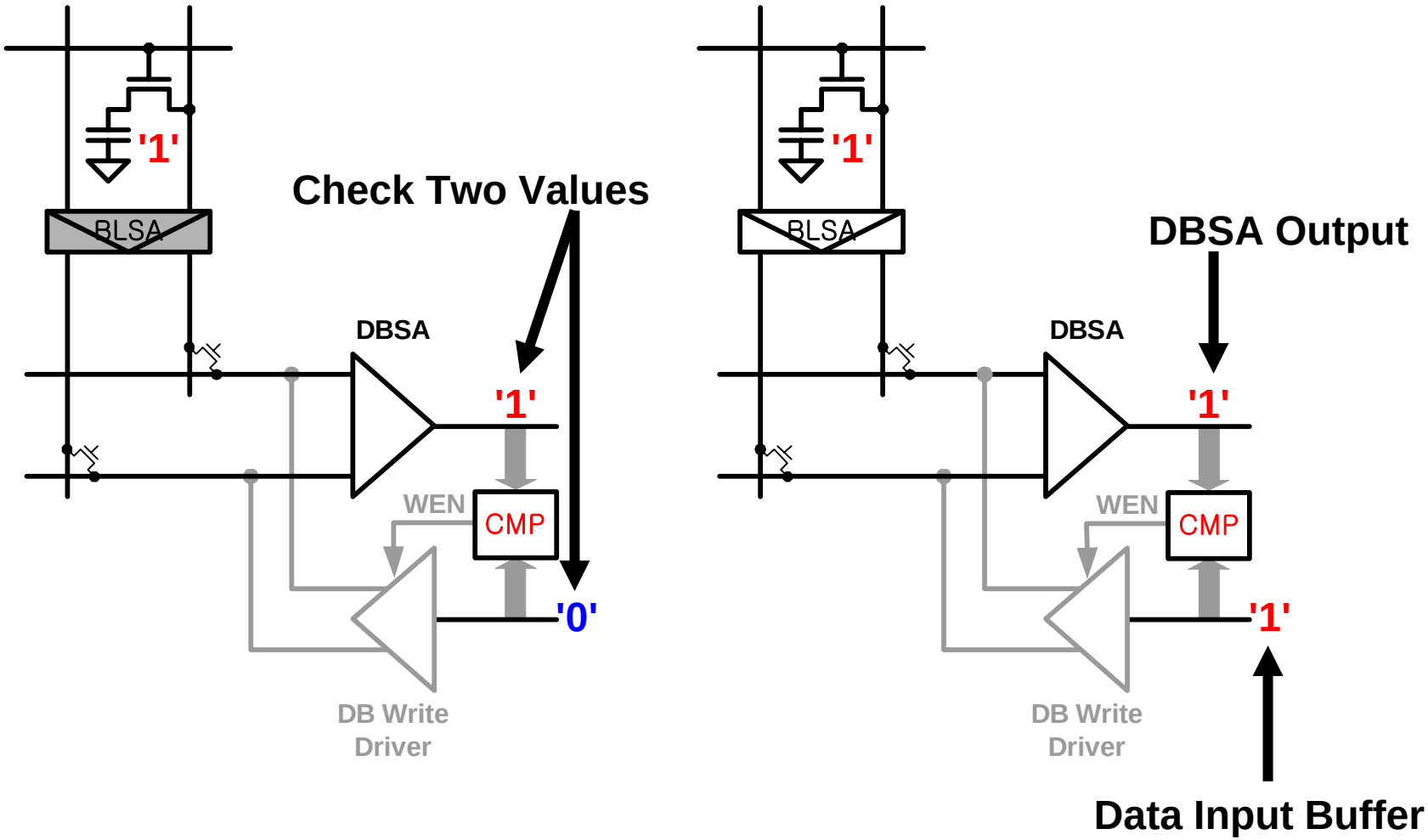
DB Line Swing in Memory R/W



$4 \times P_{READ} = P_{WRITE}$

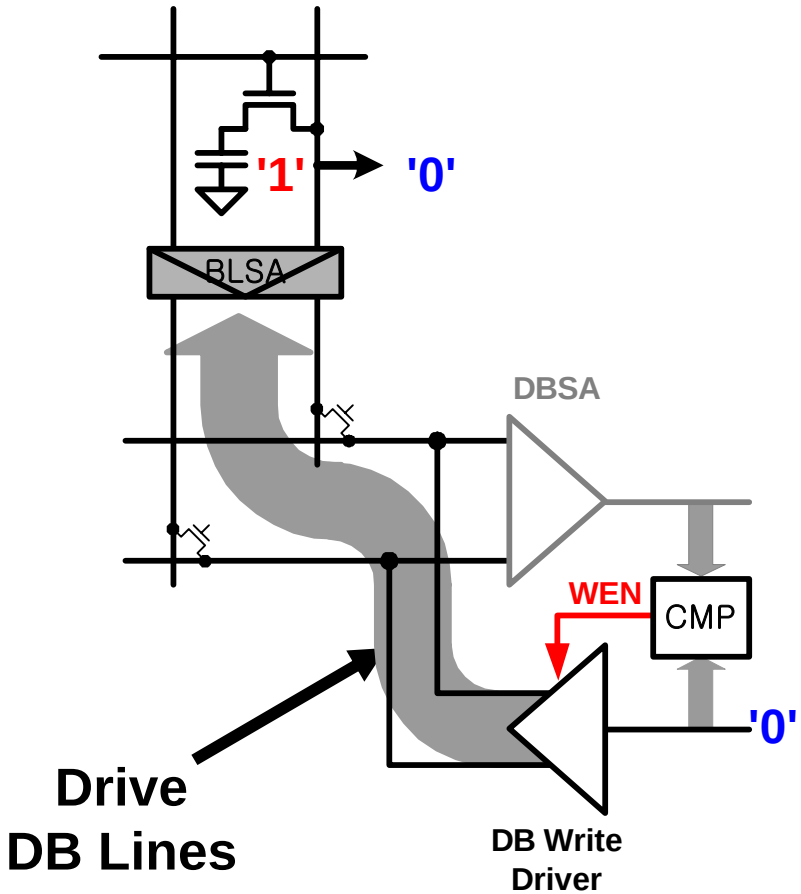
Eliminate Unnecessary Write Operation!!!

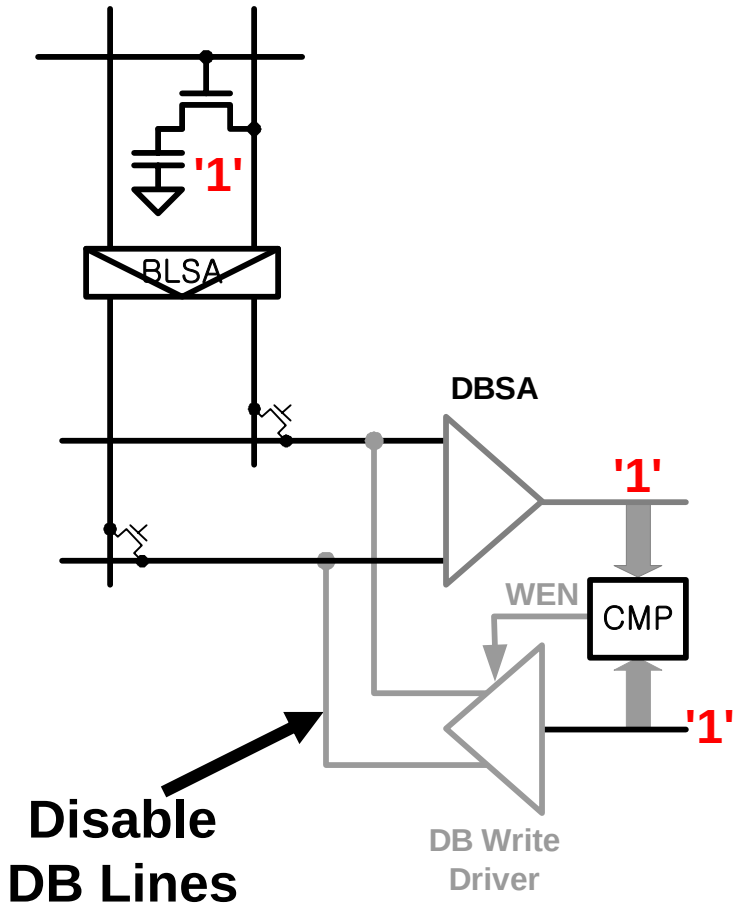
Read-Compare-Write (1/2)



Compare before DB Swing

Read-Compare-Write (2/2)

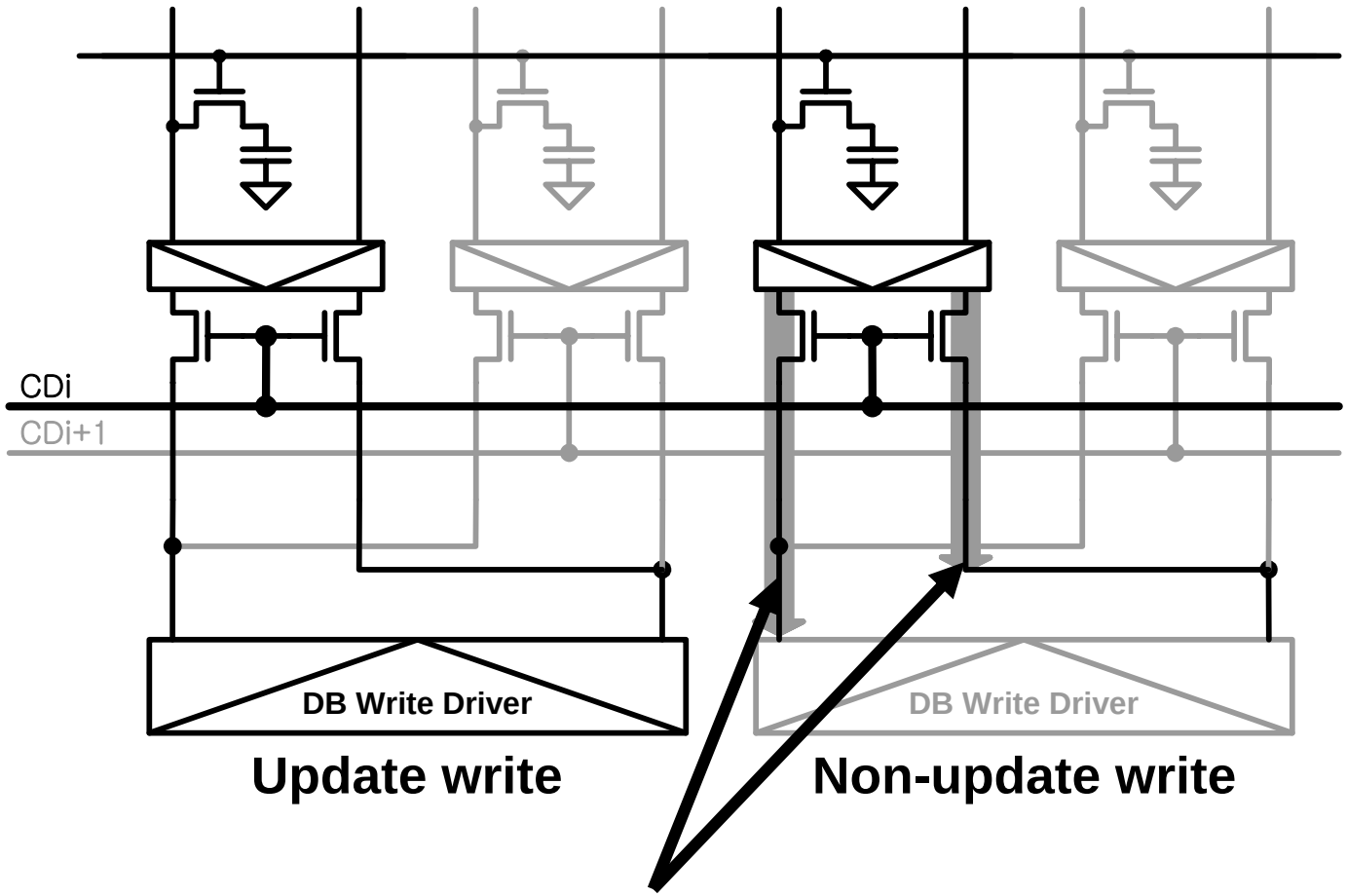




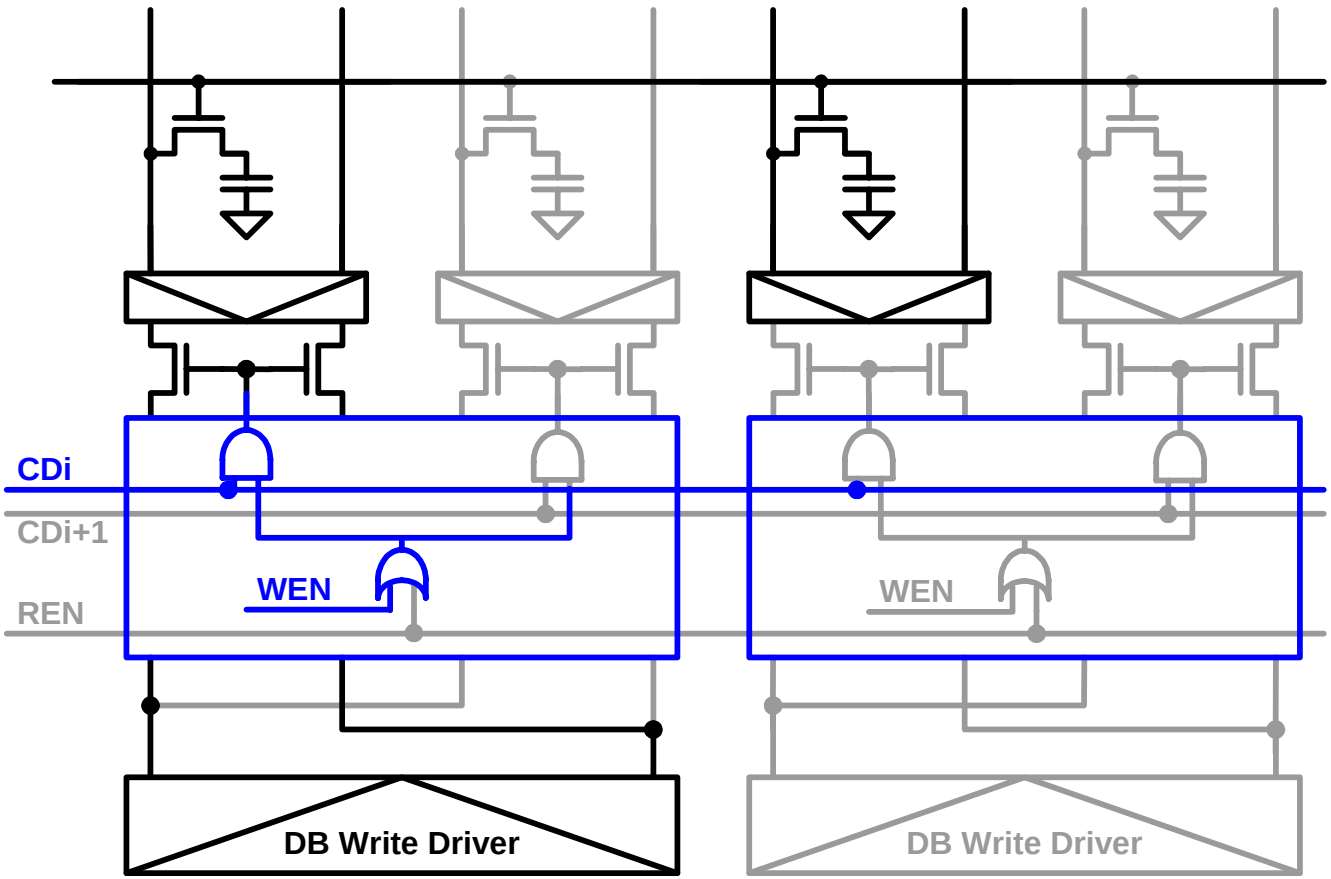
Update Write

Non-update Write

Conventional Column Control



Adaptive Column Control

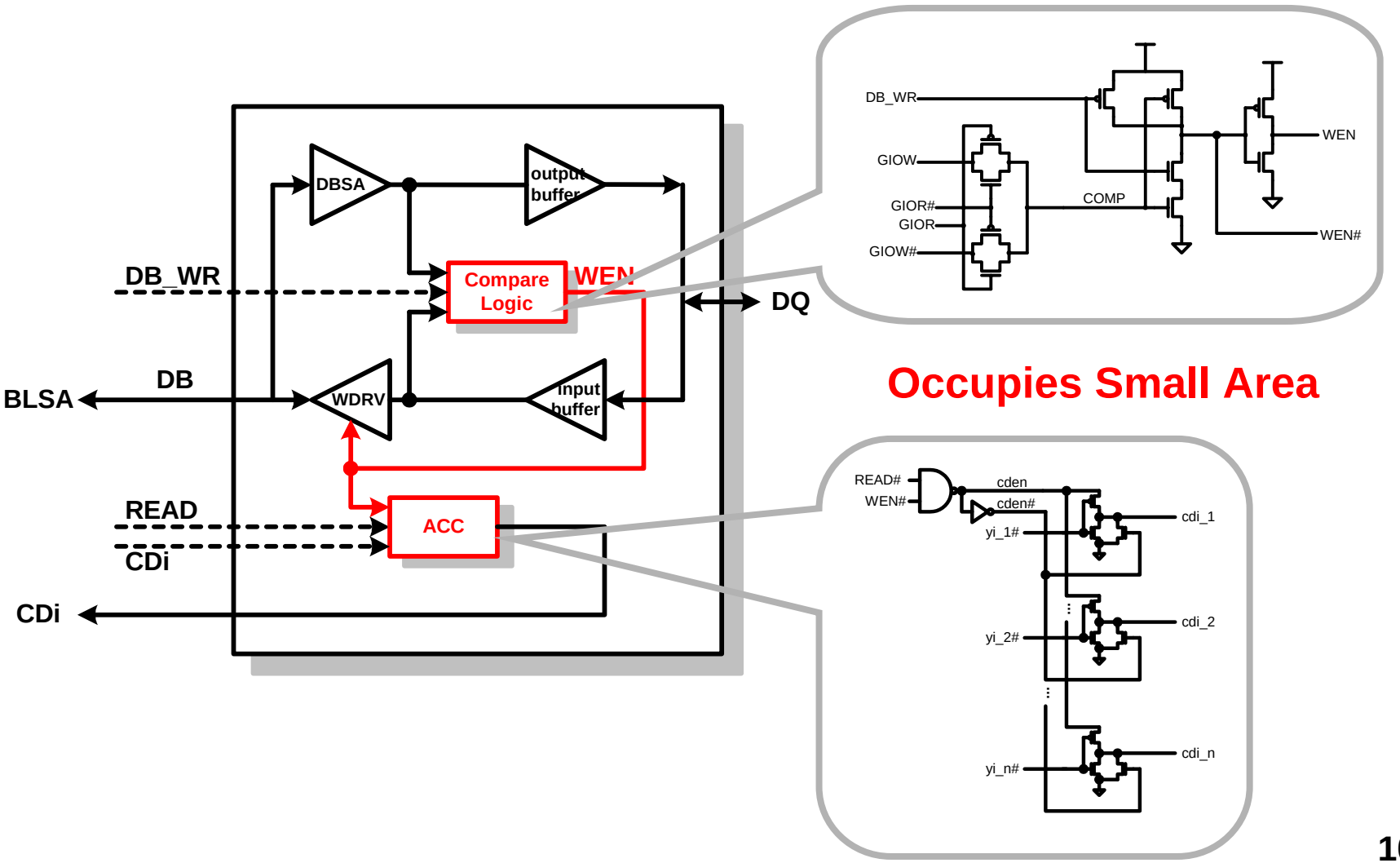


Update write

Non-update write

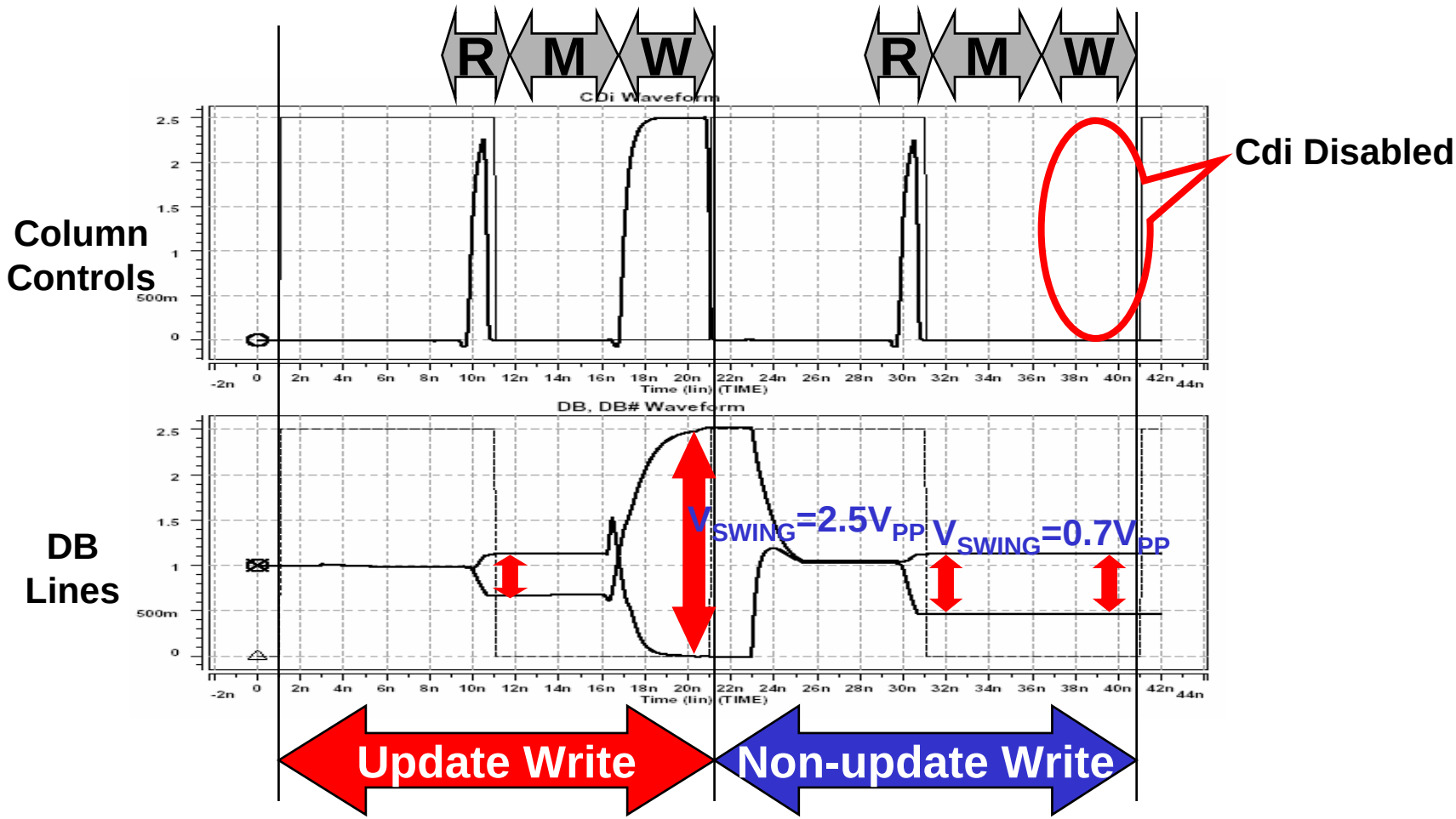
$CDi_{NEW} = CDi \bullet (WEN+REN)$

Circuit Schematic

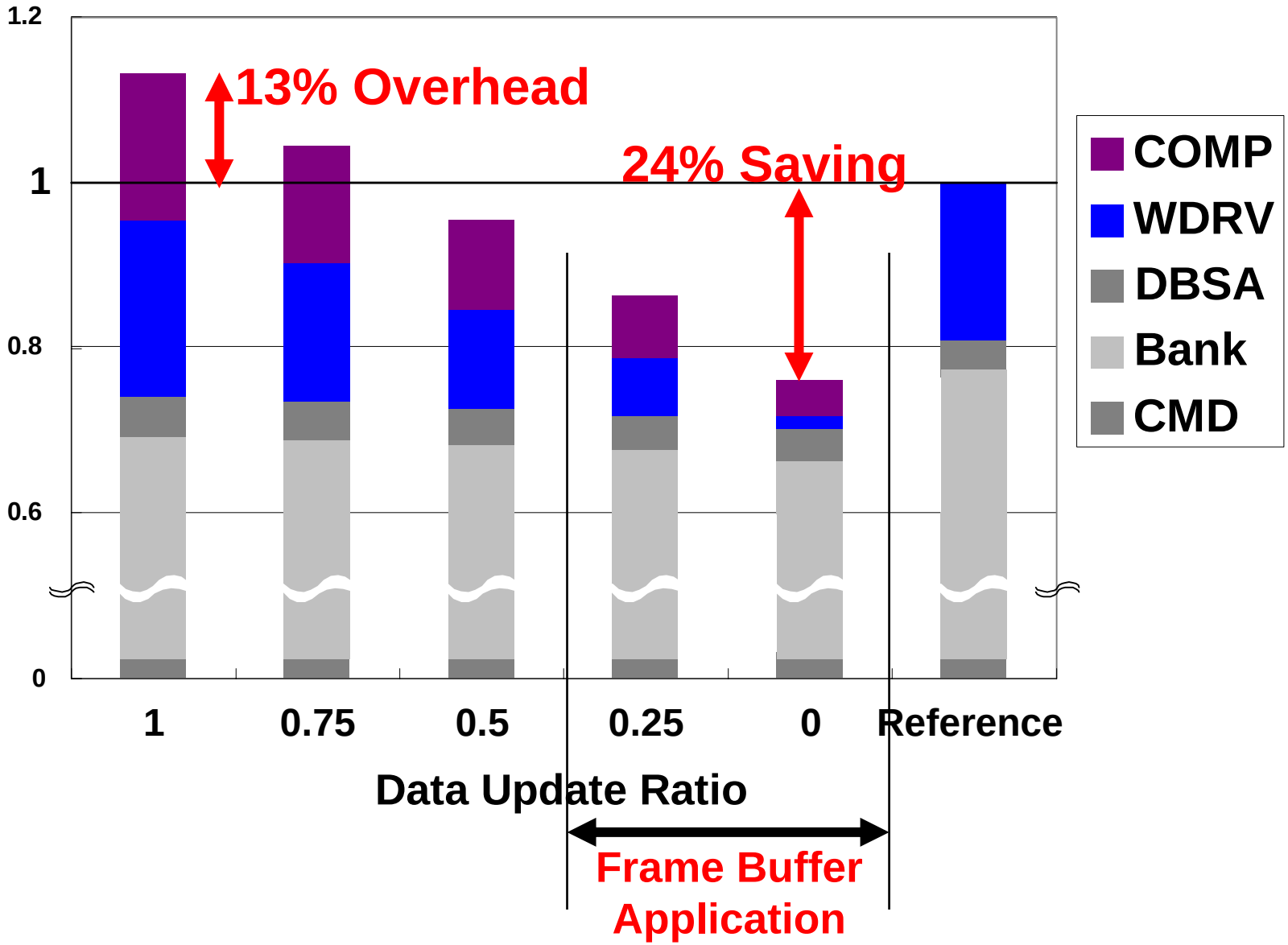


Occupies Small Area

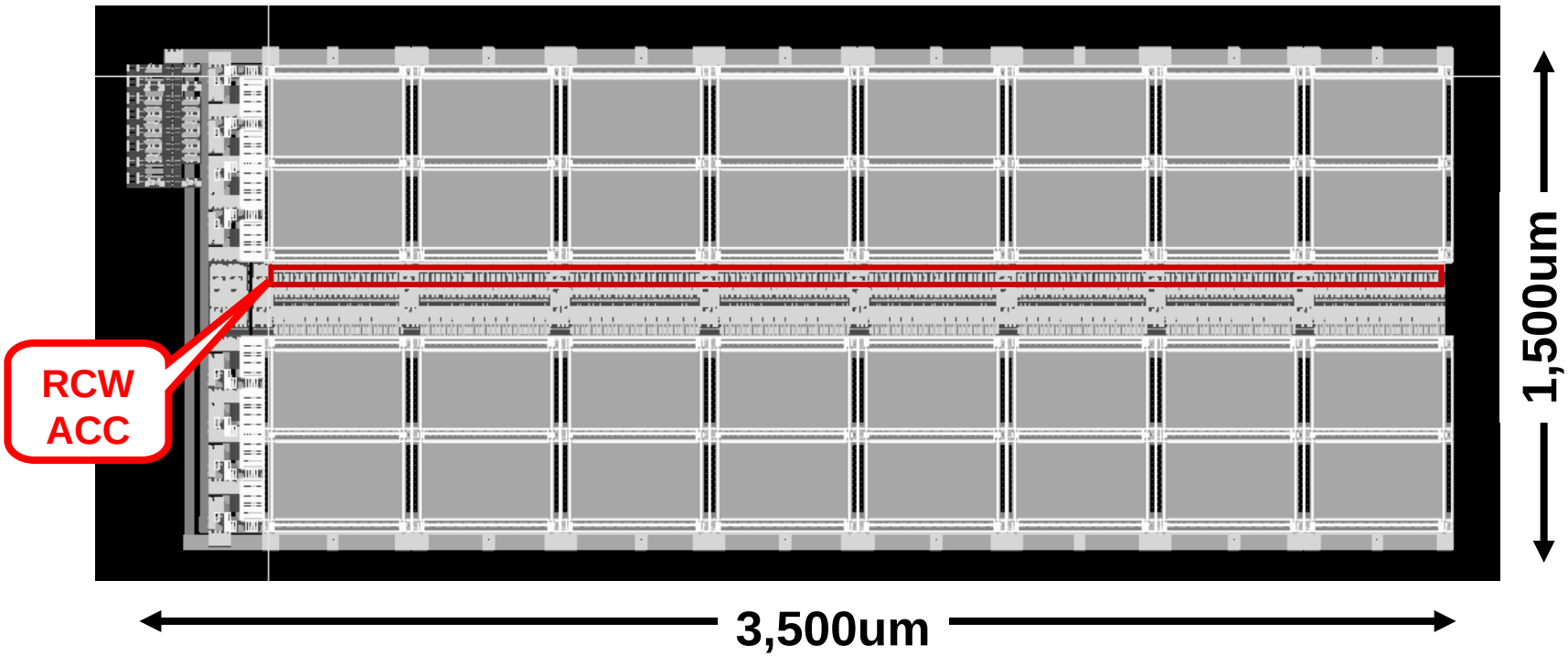
Simulation Waveform



Power Distribution Result



Die Micrograph



Capacity	6Mb
Technology	0.16um DRAM with 1-W 3-Al Metal Layers
Power	47mW (Data Update Ratio=0.0) 70mW (Data Update Ratio=1.0)

Conclusions

- **RCW and ACC scheme are proposed to reduce the power consumption of memory write operations**
- **RCW and ACC reduce the power consumption up to 24% during the write operation**
- **Less than 5% Area Overhead**
- **Applicable to the Mobile Multimedia System**