17.3 A 5.2mW Self-Configured Wearable Body Sensor Network Controller and a 12μW 54.9% Efficiency Wirelessly Powered Sensor for Continuous Health Monitoring System

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Recently, several attempts have been made to continuously monitor chronic diseases in everyday life, but their large form factors or battery power limitations still remain to be solved. Security and/or requirements of interference resilience are stringent for health monitoring, and therefore, using an open-air wireless ISM band [1] is not suitable for a health monitoring body sensor network (BSN). This paper presents a self-configured wearable BSN system with high efficiency wirelessly powered sensors that continuously monitor ECG and other vital signals at the selected locations on the body with low power consumption.

Figure 17.3.1 shows the proposed wearable BSN system. The health monitoring chest band with integrated inductor array is worn over the chest where the sensors are put on at arbitrary locations. The chest band finds the positions and types of sensors, and provides power wirelessly only to the selected sensors. The sensor chip is integrated as an adhesive bandage type Planar-Fashionable Circuit Board (P-FCB) patch [2,3]. The inductor, stacked in the sensor and on the inductor array, is also implemented by P-FCB technology (Q=10.2 and L=0.98μH). The sensor chip adopts a CMOS only adaptive-threshold rectifier (ATR) to harvest power at 13.56MHz and 400MHz. The controller chip activates only the selected inductors and transacts data with the selected sensors automatically for health monitoring, so careful alignment between reader and sensor is not necessary.

Figure 17.3.2 shows the sensor architecture and the P-FCB adhesive bandage with an inductor and a sensor chip integrated on. The sensor, consuming <12μW, is composed of an ATR, an ASK modulator (15% or 100% ASK), a signal level detector, a nested chopper ECG AFE, a 10b SAR ADC, a linear regulator and a ring oscillator (1MHz). Since the vital signal level at the P-FCB electrode is 10 to 500μV, the sensor chip should have a preamp gain ~1000, and 10b ADC with at least 800μV resolution. Its input-referred noise level should be less than 0.8μV, and hence the nested chopper scheme [4] is used to achieve 0.3μV residual offset. The signal level detector stores the information, such as received signal strength and VDD level, in its data packet transmitted to network controller by the ASK modulator.

Figure 17.3.3 shows the schematic diagram of the adaptive threshold rectifier (ATR) in the sensor chip. Maximizing the rectification efficiency is of primary importance in implementing wirelessly powered rectifiers, and in this study, sensitivity is not a major problem due to the short distance (<cm) between sensor and reader coil. In ATR, the V_t drop of diode-connected transistor is minimized to improve the rectification efficiency. M1–M4 transistors form a CMOS bridge rectifier. At startup, SW1–SW4 are connected to the drain of each transistor (ATR off). As the incoming signal is applied to ANT+ and ANT- nodes, the VP node voltage gradually increases. When the generated VOUT goes above V_t, the power-on-reset (POR) signal triggers SW1–SW4. Then the diode-connected devices M5–M8, which have a voltage difference of V_t between drain and source, are attached to the gate of M1–M4 (ATR on). Since M5–M8 are matched to M1–M4, the V_t drop of M1–M4 are cancelled out, making the dead zone virtually zero. 4 ATR blocks are cascaded to generate 1.8V at high frequency (HF, 13.56MHz) band or 1.6V at MICS (402 to 405MHz) band.

Figure 17.3.4 shows the measurement results of the sensor chip. Its rectifier peak efficiencies are measured as 54.9% and 45.2% for HF and MICS bands, respectively. The ATR makes the rectification efficiency better by 18.1% at -6dBm input power than that using expensive ferroelectric capacitors [5], or that using a battery at the sensor node [6]. The generated VDD is ~1.8V up to 200MHz before dropping sharply to 1.0V at 1GHz. At 0dBm input, VDD increases up by 0.75V when ATR is on. VDD ripple after regulation is suppressed to below 30mV (1.6% of generated VDD) while the chip is in operation. The measured ECG waveform by the differential P-FCB electrodes, recovered at the network controller, is also shown in Fig. 17.3.4.

Figure 17.3.5 shows the architecture of the network controller with a 12×4 inductor array. It is composed of an inductor array controller, a dual-band power transmitter with an 8-step adaptive power controller, an ASK demodulator, a MCU, a compression block, an AES-128 accelerator, SRAM, and an I²C interface. It can communicate with up to 48 sensors. In every programmed period (0.2 to 24h), the array controller scans the inductor array for self-configuration. According to the signals from the sensors, the network controller automatically selects the HF (for patch-type sensors such as ECG, temperature, skin conductivity, etc) or MICS (for implantable sensors) band. The data rate can be varied from 10kb/s to 120kb/s, depending on the sensor types. The adaptive power controller can control the transmitting power signal strength to compensate for the fluctuation in received power at the sensors, based on signal strength information previously programmed into the data packet by the sensor nodes. Sensor signal and the configuration information (time, position, type of sensors) are compressed by a quadratic level compression algorithm with an average compression ratio of 8.4:1 to reduce the data memory size [7]. To protect the privacy of personal health information, the sensor data are encrypted by an AES-128 accelerator [2] before being stored into a 10KB data memory. Through a high-speed mode I²C diagnosis interface, a healthcare expert can access the collected data for healthcare assistance.

Figure 17.3.6 shows the self-configuration procedure and the measured waveforms. On system reset, the inductor array controller generates X-address, X0, and increases the Y-address from Y0 to Y3. It is repeated to X11, turning on the inductor from (X0, Y0) up to (X11, Y3) (Figs. 17.3.1 and 17.3.5). If the sensor exists, the sensor replies with an acknowledgment (ACK) packet, including the sensor information, within 50ms and contains the type of sensors and the frequency band to be used (HF or MICS). Otherwise, no sensor exists and the network controller waits for 168ms before moving on to the next address. In case multiple inductors detect a sensor at the same time, or *vice versa*, the first inductor that detects the sensor takes control of the sensor, considering the response time and backscattered signal level. The entire configuration setup takes a maximum of 7.8s for a 12×4 inductor array. Measurement results of Fig. 17.3.6 show that the network controller scans (X2, Y3), (X3, Y0), (X3, Y1) and (X3, Y2) positions sequentially. In this case, (X3, Y0) and (X3, Y2) do not reply until timeout (168ms), whereas (X2, Y3) and (X3, Y1) respond, and are successfully configured.

Figure 17.3.7 shows the chip micrograph and the performance summary of the system. Average power consumption is 5.2mW for the network controller chip with 12×4 inductor array, and 12μW for the sensor chip when the sensor interfaces, the ECG AFE and the ADC are in operation. The network controller chip and the sensor chip are fabricated in 0.18μm 1P6M standard CMOS and occupy 15.0mm² and 4.8mm², respectively, including pads.

References:

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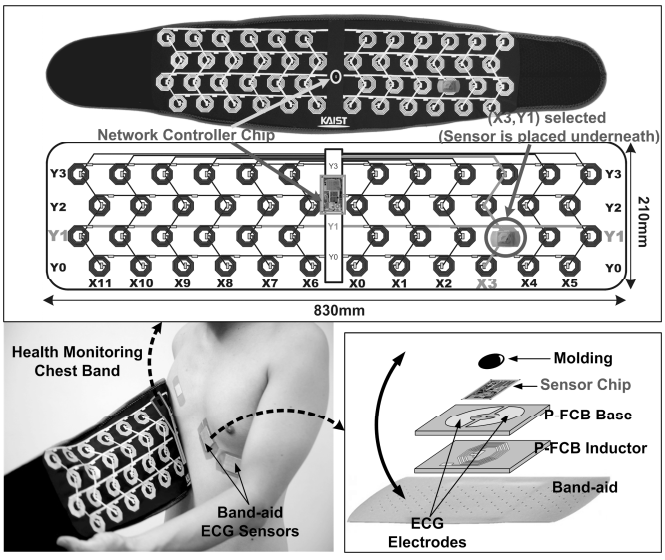


Figure 17.3.1: Proposed wearable body sensor network system.

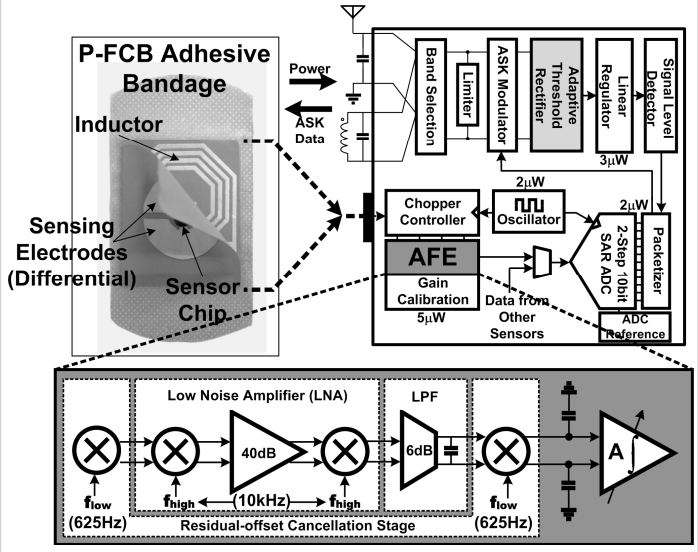


Figure 17.3.2: Sensor architecture and the P-FCB adhesive bandage type ECG AFE.

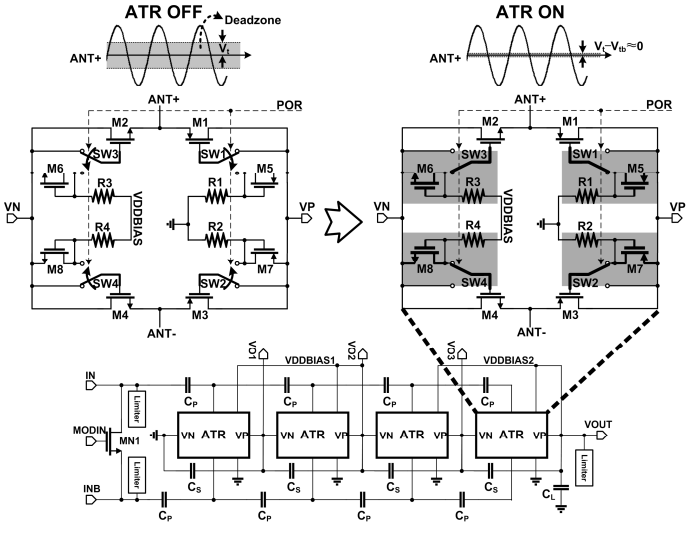


Figure 17.3.3: Adaptive threshold rectifier (ATR).

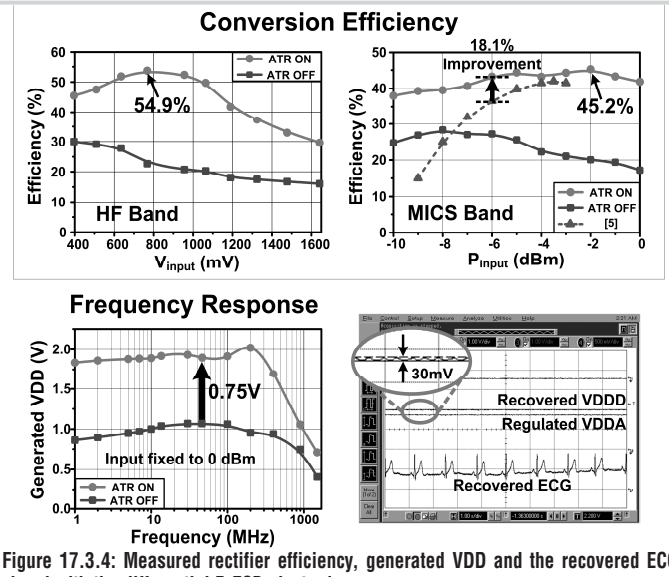


Figure 17.3.4: Measured rectifier efficiency, generated VDD and the recovered ECG signal with the differential P-FCB electrodes.

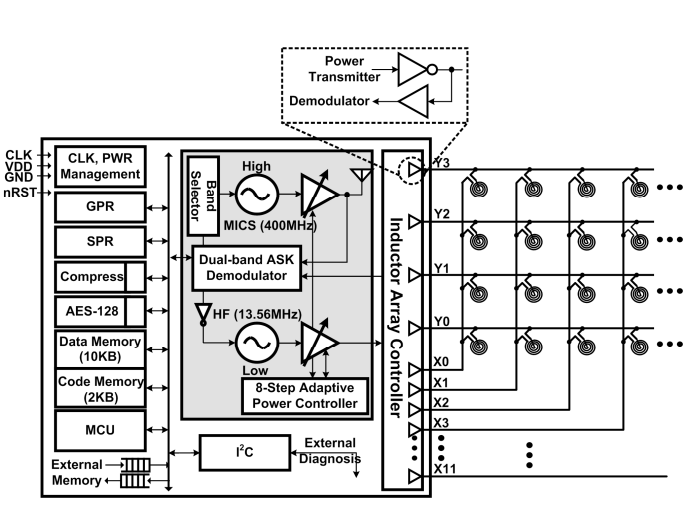


Figure 17.3.5: Network controller architecture.

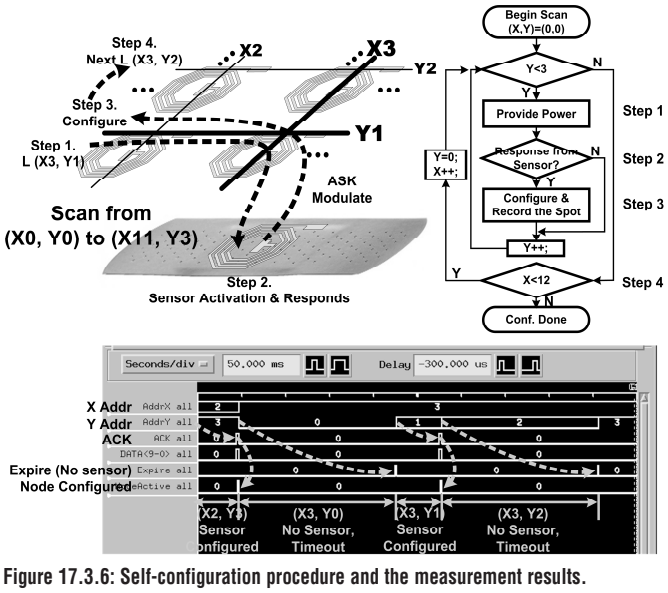
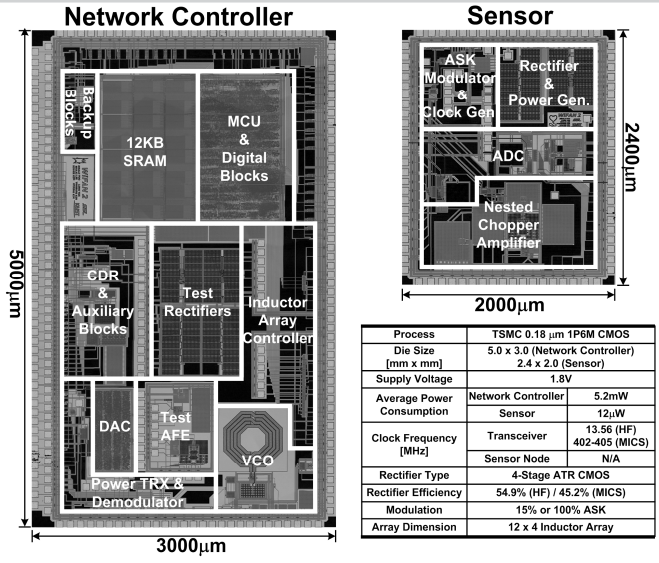


Figure 17.3.6: Self-configuration procedure and the measurement results.



Process	TSMC 0.18 μm 1P6M CMOS	
Die Size [mm x mm]	5.0 x 3.0 (Network Controller) 2.4 x 2.0 (Sensor)	
Supply Voltage	1.8V	
Average Power Consumption	Network Controller	5.2mW
	Sensor	12μW
Clock Frequency [MHz]	Transceiver	13.56 (HF) 402-405 (MICS)
	Sensor Node	N/A
Rectifier Type	4-Stage ATR CMOS	
Rectifier Efficiency	54.9% (HF) / 45.2% (MICS)	
Modulation	15% or 100% ASK	
Array Dimension	12 x 4 Inductor Array	

Figure 17.3.7: Chip micrograph and performance summary.

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