# An Energy-Efficient Dual Sampling SAR ADC with Reduced Capacitive DAC

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*Abstract*— **This paper presents an energy-efficient SAR ADC which adopts reduced MSB cycling step with dual sampling of the analog signal. By sampling and holding the analog signal asymmetrically at both input sides of comparator, the MSB cycling step can be hidden by hold mode. Benefits from this technique, not only the total capacitance of DAC is reduced by half, but also the average switching energy is reduced by 68% compared with conventional SAR ADC. Moreover, switching energy distribution is more uniform over entire output code compared with previous works.**

## I. INTRODUCTION

Recently, low power ADCs have been developed for many energy-constrained applications, such as wireless sensor networks and bio-medical applications [1],[2]. Among many types of ADC, slope ADC, sigma-delta ADC and successive approximation register (SAR) ADC are good candidates for low power applications. Especially, SAR ADC is the most widely used for low energy application [3] due to its minimum analog blocks. Many applications require relatively high resolution while maintaining low energy consumption [4]. However, the size of capacitor array in SAR ADC increases exponentially as resolution increases. Under such circumstances, saving the energy consumption in bit cycling becomes a key design issue. A lot of works focusing on saving the switching energy of capacitor array have been reported [5]-[7]. They use special capacitor array switching method such as capacitor splitting [5],[6] or junction-splitting [7] to reduce their energy consumption. Although the energy consumption is dramatically minimized in [7], the charge sharing between the isolation switches and capacitor array may result in miscalculation of LSB range. Capacitor splitting [6] proposes an energy efficient switching methodology by charge recycling. However, it still suffers from MSB calculation overhead, which consumes most of the energy.

We propose Dual-Sampling method which reduces the switching energy by 49%, and reduces total capacitance by a half, compared with previous method [5],[6]. Also, proposed method demonstrates the energy consumption is uniformly distributed over entire output code.

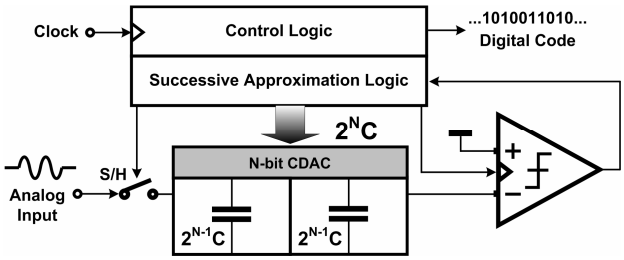



Fig. 1. Conventional SAR ADC

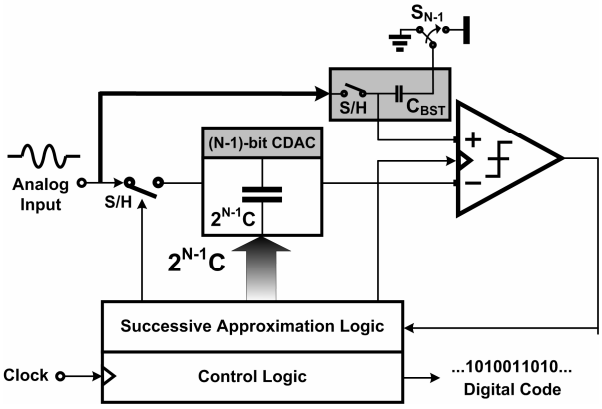



Fig. 2. Proposed Dual-Sampling SAR ADC

The rest of this paper is organized as follows. Section II introduces the proposed SAR architecture. Operation principle of this method is introduced in Section III. In section IV, the proposed method is compared in terms of energy efficiency with the previous works. This paper is concluded in Section V.

## II. THE PROPOSED SAR ARCHITECTURE

A conventional SAR ADC is composed of a binary-weighted capacitive DAC (CDAC), a comparator, SAR Control unit and switches as shown in Fig. 1. In a SAR

algorithm, operation is composed of three operation modes: sample mode, hold mode, redistribution mode.

In sample mode, CDAC samples the analog input value. In hold mode, one side of all capacitors is connected to ground and all capacitors hold analog input. And in redistribution mode, successive approximation process starts. One bit is determined at each cycle and n-cycles are needed for the n-bit digital code conversion.

In conventional n-bit SAR ADC, total capacitance of the CDAC is $2^n C_0$ , where $C_0$ is the unit capacitance. Approximated voltage is generated by CDAC and connected to one input side of comparator while the other input side is biased by reference voltage.

Fig. 2 shows block diagram of the proposed Dual-Sampling SAR ADC. In this case, total capacitance is $2^{n-1}C_0 + C_{BST}$ where $2^{n-1}C_0$ is a capacitance of CDAC and $C_{BST}$ is a capacitance of bootstrapping capacitor. Since $C_{BST}$ is just used for bootstrapping, its size is negligible in

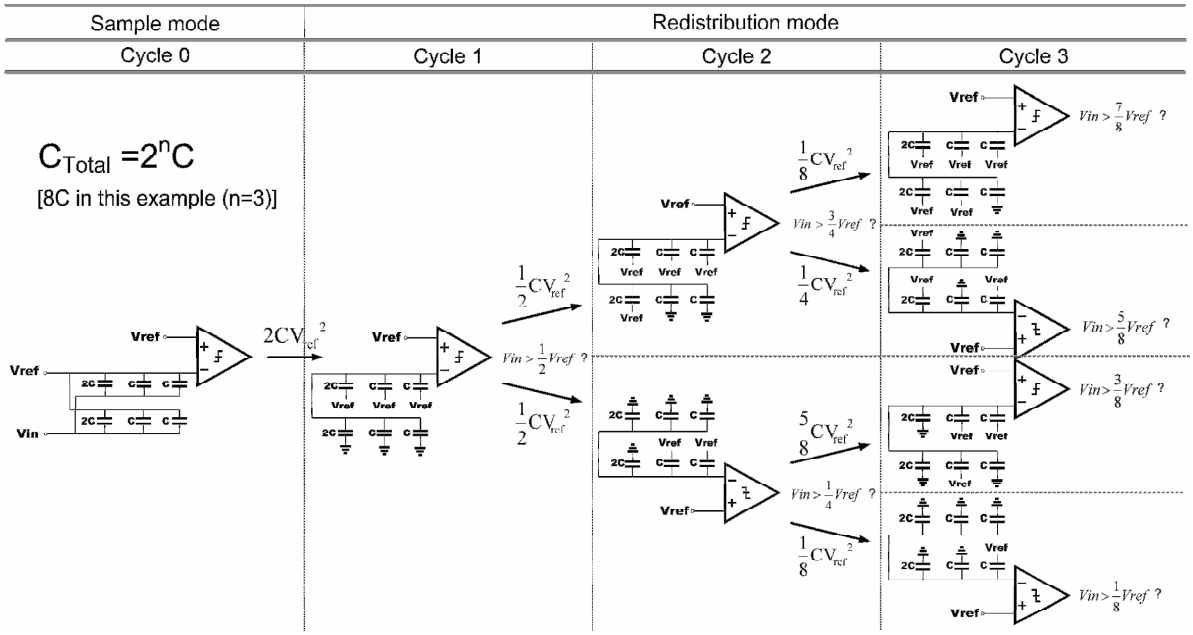



Fig. 3. Switching Sequence of Previous Method [5],[6]

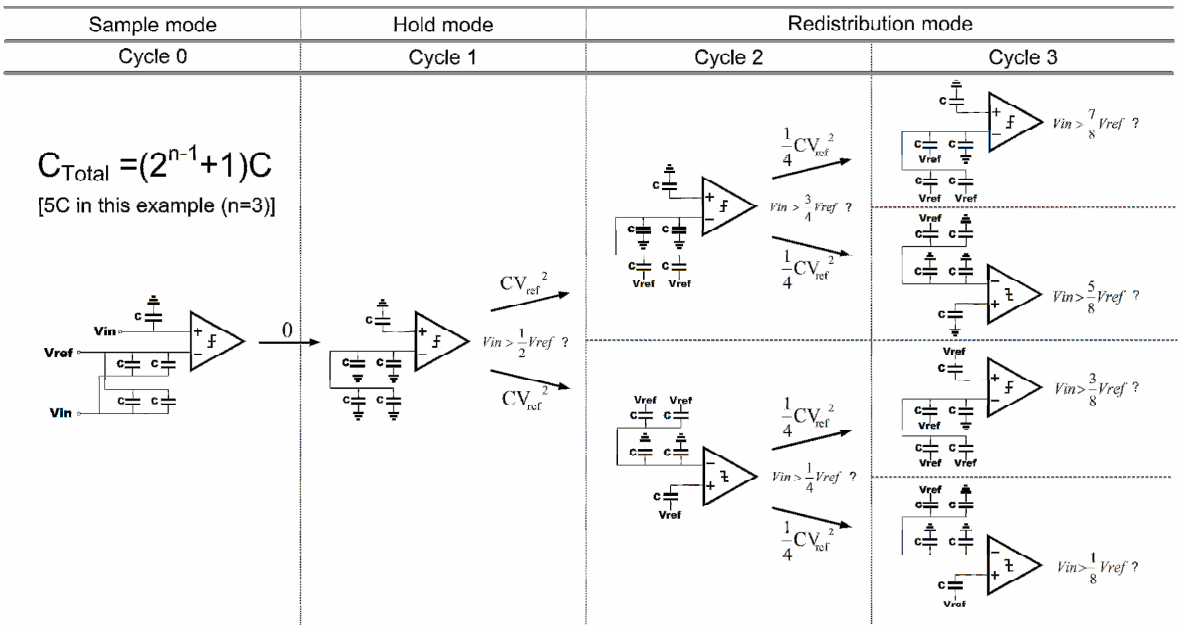



Fig. 4. Switching Sequence of Dual-Sampling method

total capacitance. In this paper, its capacitance is assumed as unit capacitance. Therefore overall capacitance used in the proposed method is about a half of conventional one.

Unlike the conventional one, both input sides of comparator in proposed method take analog signal asymmetrically in sample mode. Detailed operational sequence of the proposed architecture is described in next section.

## III. Operation of the Proposed SAR ADC

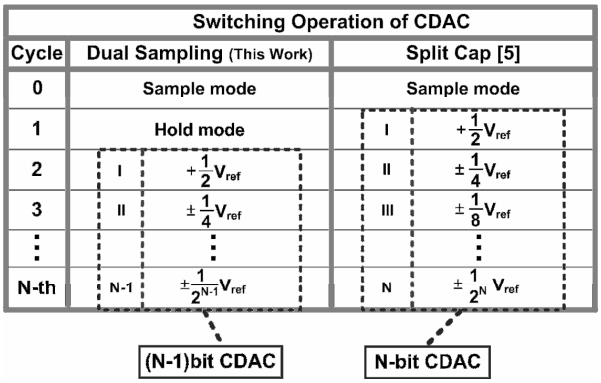
Fig. 3 shows operation and consumed energy of SAR architecture reported in [5],[6]. A 3-bit CDAC is taken as an example. First of all, one input side of comparator is connected to the reference voltage, and the other side of comparator is connected to the output of CDAC, of which the total capacitance is $8C_0$. In sample mode, CDAC samples $V_{ref}$ -$V_{in}$. During the first cycle, $4C_0$ capacitor is connected to the reference voltage for MSB calculation which consumes $2C_0V_{ref}^2$ Joules. Considering the overall switching energy consumption is $89/32C_0V_{ref}^2$ Joules in this case, this cycle consumes 71% of the total switching energy.

Fig. 4 shows operation of the proposed SAR architecture. Total capacitance is $5C_0$. In the proposed SAR architecture, analog signals are sampled and held asymmetrically at each input side of comparator; thus it is called the Dual-Sampling method. By using this method, one input side of comparator is connected to the CDAC, of which the capacitance is $4C_0$. The other input side of comparator is connected to the $C_{BST}$, of which the capacitance value is $C_0$. In sample mode, CDAC samples $V_{ref}$ -$V_{in}$, and $C_{BST}$ samples $V_{in}$. In hold mode, the MSB is decided differentially by comparator; therefore no energy is consumed during the MSB calculation. From the second cycle, the successive approximation process is conducted differentially. Table I summarizes the state of comparator input which represents the voltage of CDAC and $C_{BST}$ at each cycle. Bootstrapping by $C_{BST}$ is decided by the MSB at the first cycle. The succeeding CDAC operation is independent of the MSB value.

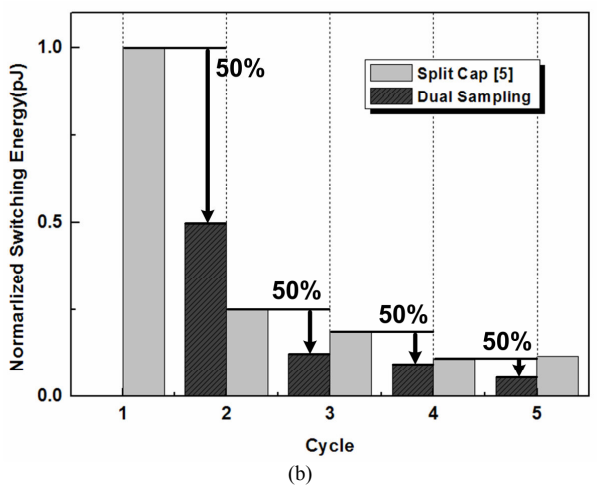
Fig. 5. (a) shows comparisons of switching operation between Split Cap [5],[6] and Dual-Sampling method.

TABLE I. State of Comparator Input by Each Cycle

| Output code | | Cycle 1 | Cycle 2 | Cycle 3 |
|---|---|---|---|---|
| **CDAC** | 11X | $V_{ref}-V_{in}$ | $V_{ref}-V_{in}+1/2\ V_{ref}$ | $V_{ref}-V_{in}+3/4\ V_{ref}$ |
| | 10X | | | $V_{ref}-V_{in}+1/4\ V_{ref}$ |
| | 01X | | $V_{ref}-V_{in}+1/2\ V_{ref}$ | $V_{ref}-V_{in}+3/4\ V_{ref}$ |
| | 00X | | | $V_{ref}-V_{in}+1/4\ V_{ref}$ |
| **$C_{BST}$** | 1XX | $V_{in}$ | $V_{in}$ | |
| | 0XX | | $V_{ref}+V_{in}$ | |




(a)




(b)

Fig. 5. Comparisons of (a) switching operation between Split Cap [5],[6] and Dual Sampling. (b)switching energy at each cycle. Dual Sampling method saves energy with (N-1)bit CDAC by hiding the MSB calculation in hold mode.

Analog input value is sampled at the cycle 0 in both methods. In Split Cap method [5],[6] , $V_{ref}-V_{in}$ is sampled in $2^nC_o$. In Dual-Sampling method, $V_{ref}-V_{in}$ is sampled in $2^{n-1}C_o$, and $V_{in}$ is sampled in $C_{BST}$. Consequently, the total input capacitance of Dual-Sampling method is half compared with Split Cap method. As a result, it requires only half energy consumption for sampling analog input. In Dual-Sampling method, the MSB calculation is hidden by hold mode. A (N-1) bit DAC is used and same operation is performed regardless to the value of the MSB. Because the capacitance of (N-1) bit DAC is a half of N-bit CDAC, CDAC I Operation in Dual Sampling consumes half energy of that in Split Cap [5],[6]. In the same way, CDAC II Operation in Dual Sampling dissipates half the energy of that in [5],[6]. This is represented in Fig. 5. (b). Energy consumption of cycle 1 is zero in the Dual-Sampling method. From the second cycle, the switching energy in this method consumes half of previous cycle in [5],[6]. If all the energy consumption at each step is accumulated, the total switching energy in the Dual-Sampling method is a half of that in [5],[6].

TABLE II. COMPARISON OF TOTAL CAPACITANCE , SWITCHING ENERGY AND STANDARD DEVIATION

| Method | Total Capacitance | Norm. $E_{ramp}$ | Standard Deviation | Normalized Sampling Energy |
|---|---|---|---|---|
| Conventional | $2^n C_0$ | 1 | 1 | 1 |
| Split Cap | $2^n C_0$ | 0.623 | 0.262 | 1 |
| **Dual Sampling** | $2^{n-1} C_0 + C_0$ | **0.320** | **0.132** | **0.5** |

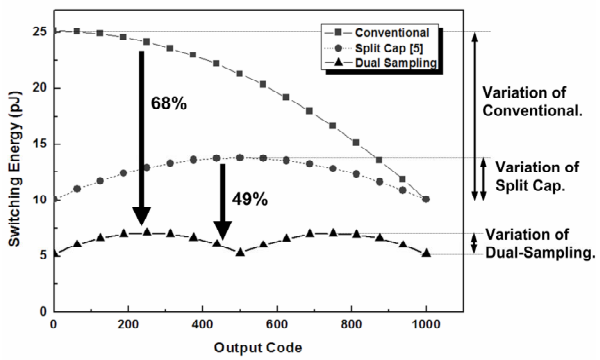



Fig. 6. Comparison of Switching Energy

## IV. SIMULATIONS AND COMPARISONS

A 10bit SAR ADC is simulated with three models: Conventional model, Split Cap model [5],[6], and the proposed Dual-Sampling model. Simulation is performed with 10b CDAC in a 0.18 $\mu$m CMOS process. Switching energy is calculated with 17 samples of output code. These models are analyzed with rigorous SPICE simulations. Fig. 6 shows performance comparison of switching energy among three models by simulation. It shows that the Dual-Sampling method saves 68% and 49% of switching energy compared with conventional method and Split cap method [5],[6], respectively.

Another benefit from Dual Sampling method, switching energy is uniformly distributed over the entire output code. If the distribution of switching energy is not uniform, linearity of ADC may be suffered from irregular energy consumption. In Fig. 6, Split capacitor method [5],[6] draws a parabolic shape. On the other hand, graph of Dual-Sampling method draws a pair of parabolic shapes. Because of these features, the standard deviation of Dual-Sampling is smaller than that of [5],[6] and conventional method. This phenomenon originated from symmetric operation of CDAC, regardless to the value of MSB, which is described in Table I.

Table II compares the three models in terms of total capacitance, switching energy and standard deviation of average energy consumption. A half of total capacitor is used in the Dual-Sampling method compared with that in Split-Cap method [5],[6]. All simulation is conducted by ramp input, the unit capacitance is 20fF and reference voltage is 800mV in 10-bit resolution. The Dual Sampling method reduces energy consumption by 68% and 49% compared with conventional method and Split Cap [5],[6], respectively. Standard deviation of switching energy is only 13% and 50% compared with conventional method and Split Cap [5],[6] , respectively.

## V. CONCLUSIONS

We present a new SAR ADC architecture that reduces energy consumption and total capacitor size significantly. The Dual-Sampling method holds the analog signal at each comparator input asymmetrically in sample mode. This operation makes the MSB to be calculated without consuming any switching energy. As a result, the proposed SAR ADC reduces the total capacitance by 50% and switching energy by 68% compared with the conventional method. Also, standard deviation of switching energy is reduced by 87% compared with conventional method.

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